PCI EXPRESS GEN 3 - COMPLIANCE AND DEBUG TESTING

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ROHDE&SCHWARZ

Make ideas real

AGENDA

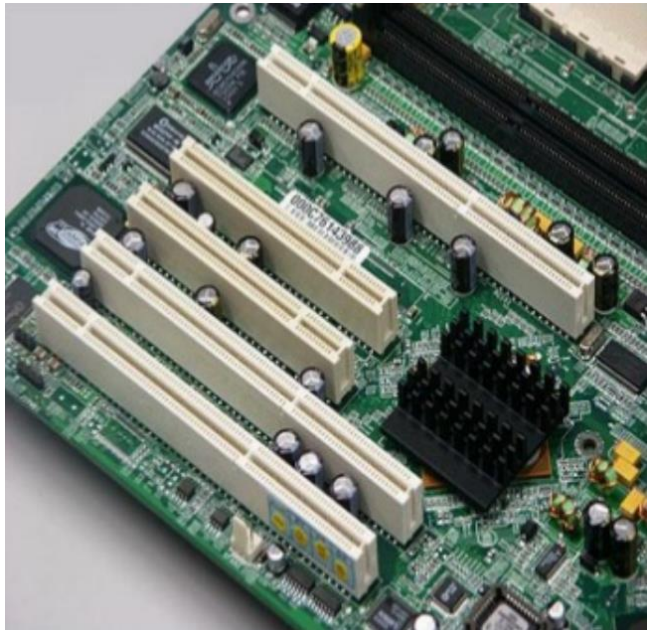
- Overview of PCIe
  - Introduction
  - Architecture
  - Form factors
- R&S solutions for PCIe
  - Compliance testing
  - Protocol Trigger and Decode
  - Signal Integrity Debug

PCI EXPRESS (PCIe)

- Introduced in 2004
- Peripheral Component Interconnect Express is the de facto standard to connect high performance IO devices to the rest of the system. Eg. NICs, NVMe, graphics, TPUs
- Computer to Peripheral Communication
- Overseen by PCI-SIG
- Full-duplex bidirectional

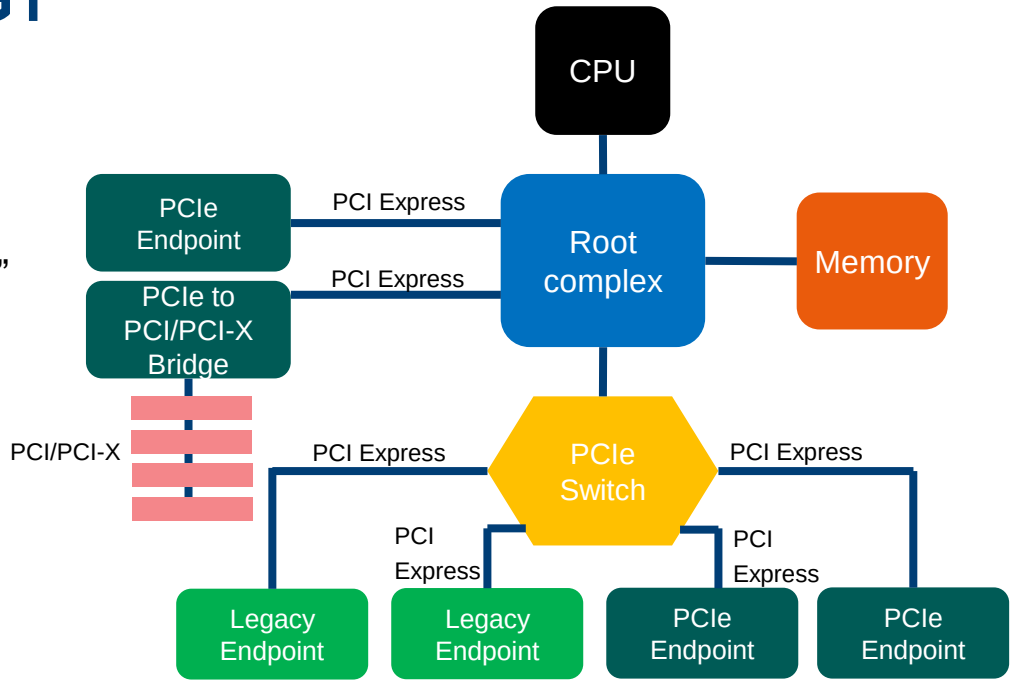
	Transfer Rate	Link BW	Total x16 BW	Coding
PCIe 1.x	2.5 GT/s	2 Gbit/s	8 GB/s	8b/10b
PCIe 2.x	5.0 GT/s	4 Gbit/s	16 GB/s	8b/10b
PCIe 3.x	8.0 GT/s	8 Gbit/s	~32 GB/s	128b/130b
PCIe 4.x	16.0 GT/s	16 Gbit/s	~32 GB/s	128b/130b
PCIe 5.x	32.0 GT/s	32 Gbit/s	~128 GB/s	128b/130b **(PAM)**

- Backwards compatibility
- Still evolving….”first draft” of PCIe Gen6 was released in Feb. 2020



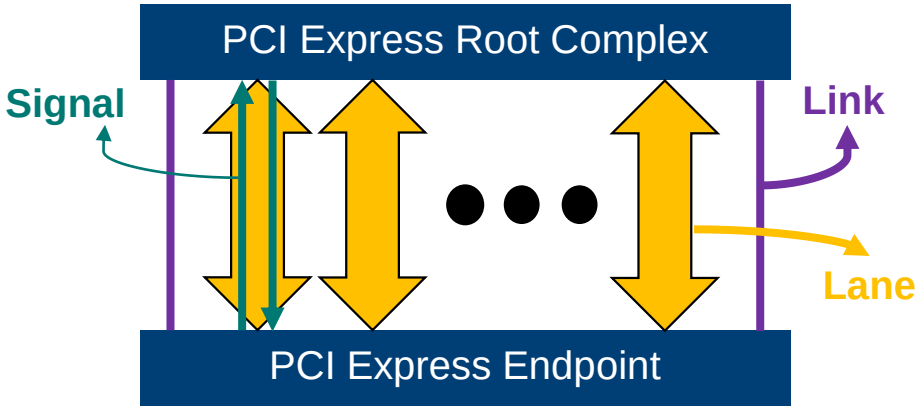
PCI EXPRESS ARCHITECTURE - TOPOLOGY

- Shared topology - only single root system
- Data Integrity and Error Handling
  - Link-level “LCRC” & End-to-end “ECRC”
- Credit-based Flow Control
  - MSI/MSI-X style interrupt handling
- Advanced power management
  - Active State PM
- OS independent!
- Enumeration is performed at boot up



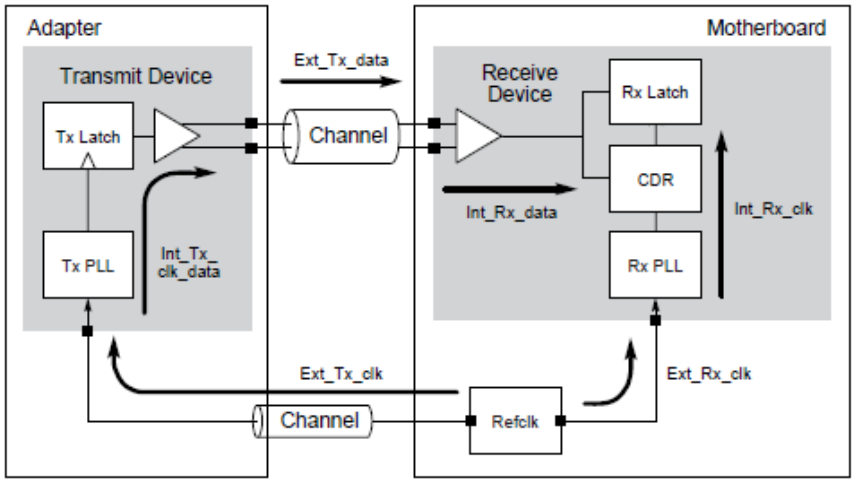
PCI EXPRESS ARCHITECTURE

- Dual Simplex point-to-point serial connection
  - Independent transmit and receive sides
- Interconnect / Link
  - Logical connection between PCIe devices
- Scalable Link Widths
  - x1, x2, x4, x8, x12, x16, x32
  - CPU support this by bifurcation
  - Dual differential signal pair (one pair for receive, one pair for transmit), 4 wires per Lane
- Scalable Link Speeds
  - 2.5…up to 16.0GT/s per Lane
- Packet based transaction protocol



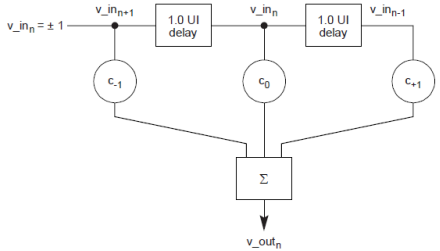
PCI EXPRESS ARCHITECTURE - SIGNALING

- Terminations
  - Up to PCIe Gen 3 on-die to 100 ohms differential (+/- 15%)
  - From Gen 4 this moves to 85 ohms differential
- AC Coupled Differential Pairs (LVDS)
  - Voltage max. 1,200 mV, typically 800 mV
  - Reference Clock (not mandatory to be sperate)
- Clock is embedded



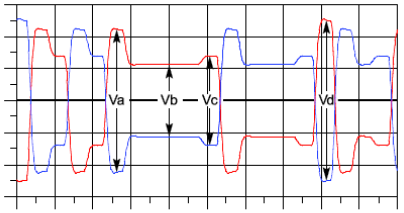
PCI EXPRESS ARCHITECTURE - EQUALIZATION

- PCIe 3.0 promotes equalisation at the Tx and/or Rx
  - Mitigate ISI and improve BER
- Transmitter (TxEQ)
  - Avoid overdriving
  - Simple 3-tap FIR filter
  - Results in De-emphasis, Flat level, Pre-shoot
- Receiver (RxEQ)
  - Improves data eye via behavioural algorithm
  - 1st order CTLE and DFE (taps) filters

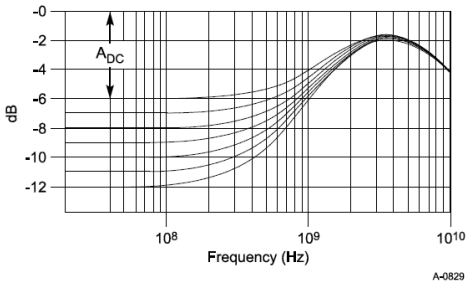


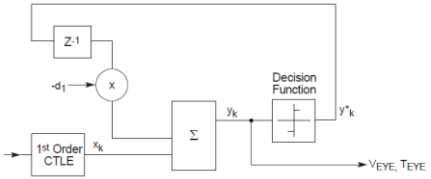
$v\_out_n = (v\_in_{n+1} * c_{-1}) + (v\_in_n * c_0) + (v\_in_{n-1} * c_{+1})$

$|c_{-1}| + |c_0| + |c_{+1}| = 1 \quad c_{+1} \le 0 \quad c_{-1} \le 0$



De-emphasis = $20\log_{10}$ Vb/Va
Preshoot = $20\log_{10}$ Vc/Vb
Boost = $20\log_{10}$ Vd/Vb



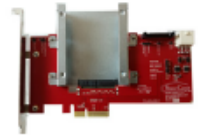


$y_k = x_k - d_1 \mathrm{sgn}(y_{k-1})$
y_k = DFE summer differential output voltage.
y^*_k = decision function output voltage. $|y^*_k| = 1$
x_k = DFE differential input voltage
d_1 = feedback coefficient
k = sample index in UI

PCI EXPRESS
EVOLUTION OF FORM FACTORS – ENDPOINT

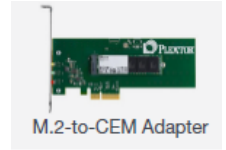
- **CEM Add-in Cards**
  - CEM Add-in Cards is the most commonly used form factor.

- **U.2 (SFF-8639)**
  - U.2 is a newer and smaller form factor for connecting SSDs to computers.
  - Uses 4 x PCIe lanes and 2 x SATA lanes



U.2-to-CEM Adapter

- **M.2 (NGFF)**
  - M.2 form factor is upcoming and even smaller than U.2
  - Replaces the mSATA standard (which used mPCIe)
  - Application : Ultrabooks, tablets



M.2-to-CEM Adapter

PCI EXPRESS
EVOLUTION OF FORM FACTORS – ROOT COMPLEX

- Motherboards
  - Various different form factors
  - Depending on the size, each will have different pinouts and environments
  - Different set of CEM connectors
    - x1, x4, x8, x16
  - A lower adapter card can fit a higher slot. However, a larger card cannot fit a lower slot.

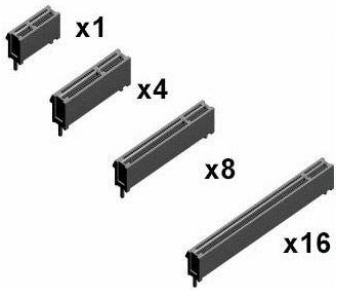
Standard-ATX

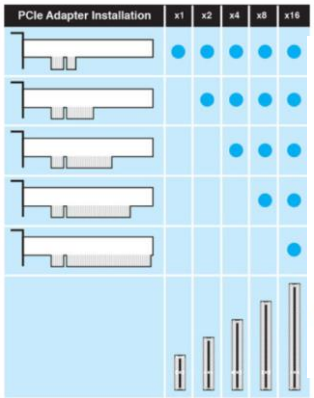
Micro-ATX

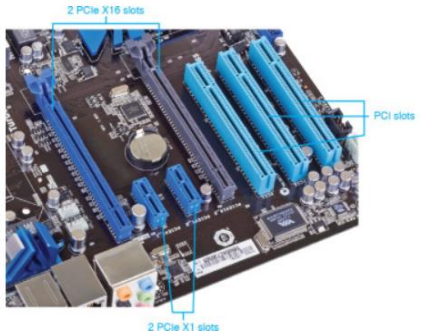
Mini-ITX

Nano-ITX

Pico-ITX



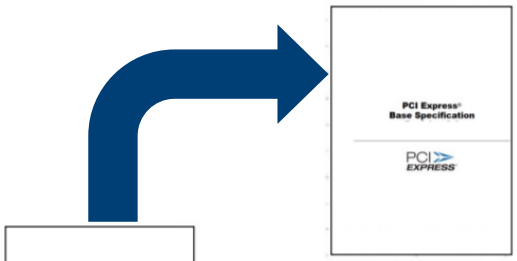




R&S SOLUTIONS

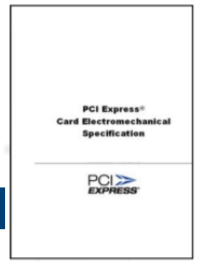
PCI EXPRESS STANDARDS

► Select the specification that relate to your needs



Base specification
- Contains all the system knowledge
- Can directly be applied to Chip test

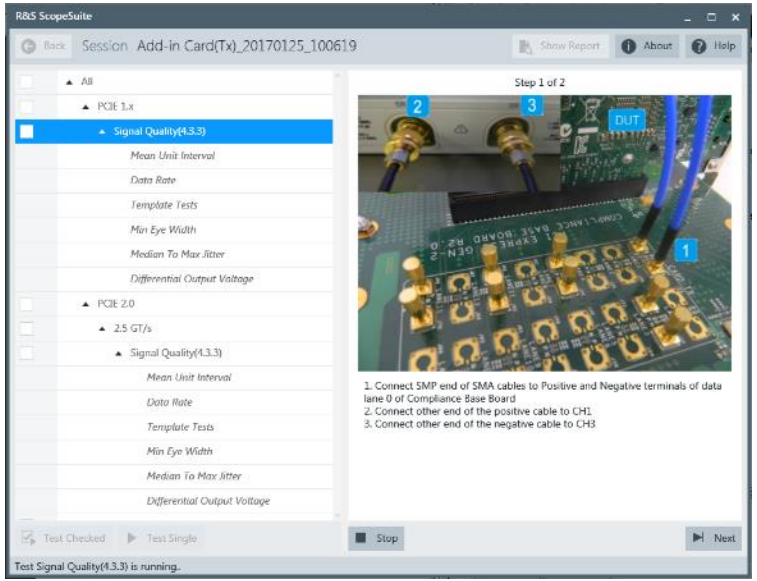
PHY Test Specification
- Defines compliance tests of CEM spec in detail



Card Electromechanical (**CEM**) Sepc
- Applies to Add-In Cards and Mother Boards
- Mitigates card manufacturer's need to study the base spec
- Increases reproducibility through PCI-SIG supplied test tools CBB and CLB

PCI EXPRESS AUTOMATED SOLUTION

- R&S®RTO/P-K81 and R&S®RTP-K83
- PCI Express 1.1/2.0/3.0 with data rate up to 8 Gbit/s
- Support of Add-in Card and System Motherboard
- Based on PCI-SIG Standard post-processing analysis software SigTest tool and test fixtures (CBB, CLB)
- Test of Signal Quality and Reference Clock
- Embedded in R&S®ScopeSuite Compliance Test application
- Step-by-step wizard for user guidance
- Clear and comprehensive test documentation

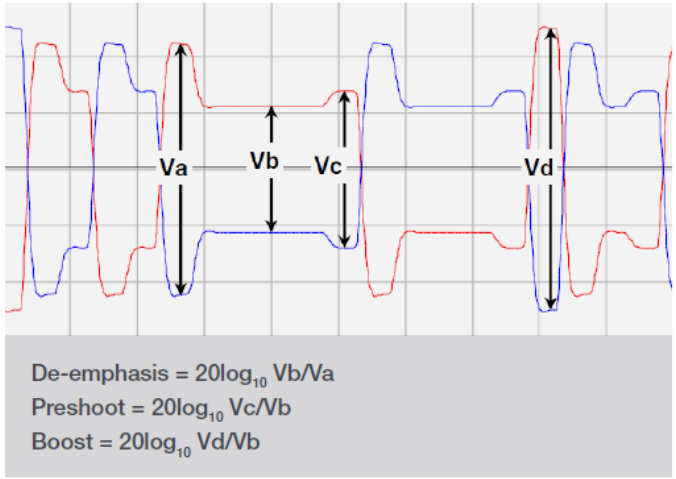


Base Board (Add-in Card testing)

Load Board (System testing)

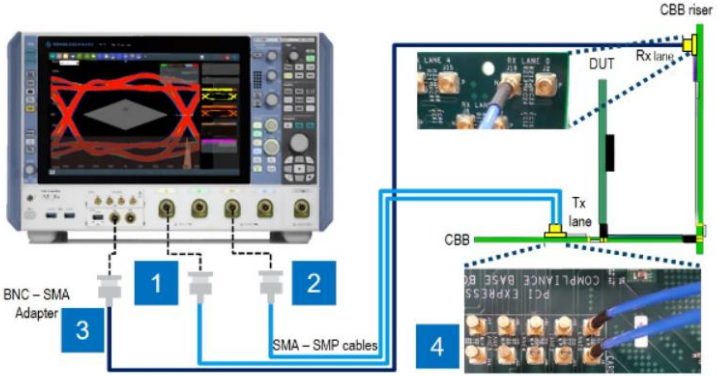
PCI EXPRESS
COMPLIANCE PATTERNS

- Compliance Presets for all speeds
- These are used to equalise channel loss and optimise SI on the link
- Combination of pre-shoot and de-emphasis applied by the host system to the endpoint
- 100MHz clock burst to toggle through these presets



Generation	Preset #	Preshoot (dB)	De-emphasis
Gen 1	P0	-	-3.5 ± 1dB
Gen 2	P0	-	-3.5 ± 1dB
	P1	-	-6 ± 1.5dB
Gen 3	P0	0	-6 ± 1.5dB
	P1	0	-3.5 ± 1dB
	P2	0	-4.4 ± 1.5dB
	P3	0	-2.5 ± 1dB
	P4	0	0
	P5	1.9 ± 1dB	0
	P6	2.5 ± 1dB	0
	P7	3.5 ± 1dB	-6 ± 1.5dB
	P8	3.5 ± 1dB	-3.5 ± 1dB
	P9	3.5 ± 1dB	0
	P10	0	Variable

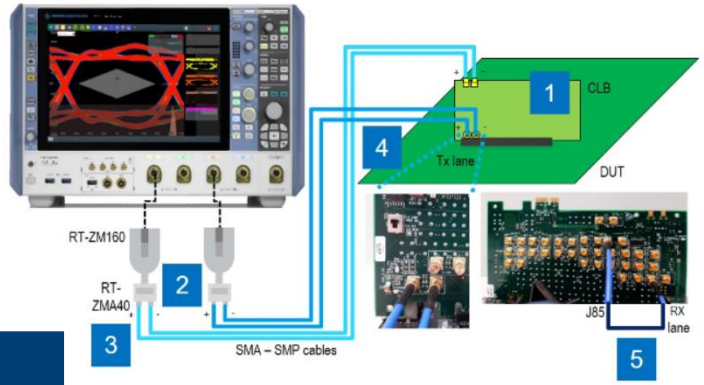
PCI EXPRESS TEST EQUIPMENT



PCIe Gen 3 – Add-In Cards

Type	Recommended model	Description
Oscilloscope	R&S®RTP134	13 GHz bandwidth oscilloscope
Generator	R&S®RTP-B6	Built-in AWG for automated switching of compliance patterns
Pulse source	R&S®RTP-B7	Channel de-skew calibration
Cables and adapters	R&S®RT-ZA17	Pair of matched 50 Ohm SMA-SMA cables
	R&S®RT-ZA16	BNC-SMA adapters
Software	R&S®ScopeSuite	Compliance automation software

PCI EXPRESS TEST EQUIPMENT



PCIe Gen 3 - System

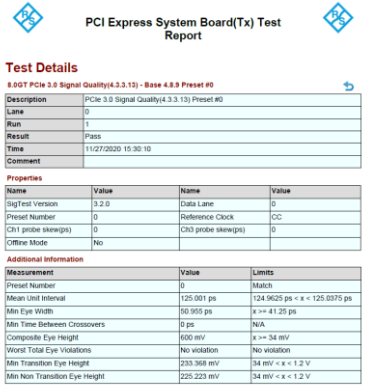
Type	Recommended model	Description
Oscilloscope	R&S®RTP134	13 GHz bandwidth oscilloscope
Generator	R&S®RTP-B6	Built-in AWG for automated switching of compliance patterns
Pulse source	R&S®RTP-B7	Channel de-skew calibration
Cables and adapters	2 x R&S®RT-ZM130	13 GHz Modular probe amplifier system
	2 x R&S®RT-ZMA40	SMA module for Modular probe system
	2 x R&S®RT-ZA17	Pair of matched 50 Ohm SMA-SMA cables
Software	R&S®ScopeSuite	Compliance automation software

PCI Express

DEMO – GEN 3 ADD-IN CARD

PCI EXPRESS SUMMARY

- ScopeSuite Software
- Easy to use test wizard → No need to be an expert
- High level of automation for fast results
- Individual test selection
- Limit editor
- Possibility to repeat tests
- Result windows with pass/fail indication
- Reporting includes all details
  - Screenshots
  - Measurement results
  - Limits, pass-fail indication
  - Test summary


PCI Express System Board(Tx) Test Report

Test Details

8.0GT PCIe 3.0 Signal Quality(4.3.3.13) - Base 4.8.9 Preset #0

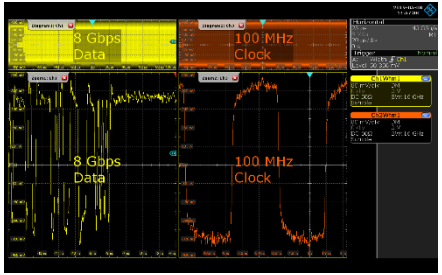
Description	PCIe 3.0 Signal Quality(4.3.3.13) Preset #0
Lane	0
Run	1
Result	Pass
Time	11/27/2020 15:30:10
Comment	

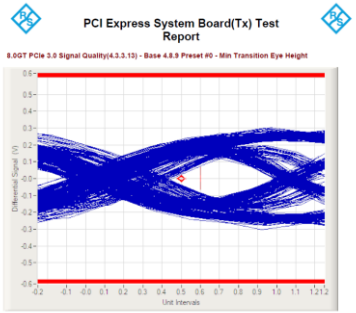
Properties

Name	Value	Name	Value
SigTest Version	3.2.0	Data Lane	0
Preset Number	0	Reference Clock	CC
Ch1 probe skew(ps)	0	Ch3 probe skew(ps)	0
Offline Mode	No		

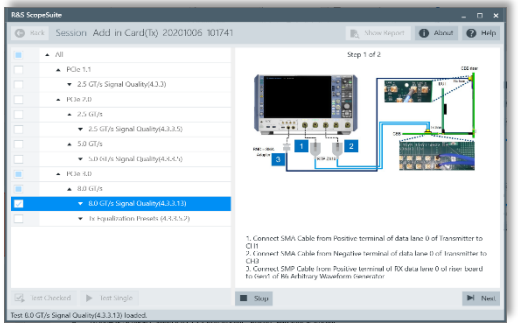
Additional Information

Measurement	Value	Limits
Preset Number	0	Match
Mean Unit Interval	125.001 ps	124.9625 ps < x < 125.0375 ps
Min Eye Width	50.955 ps	x >= 41.25 ps
Min Time Between Crossovers	0 ps	N/A
Composite Eye Height	600 mV	x >= 34 mV
Worst Total Eye Violations	No violation	No violation
Min Transition Eye Height	233.368 mV	34 mV < x < 1.2 V
Min Non Transition Eye Height	225.223 mV	34 mV < x < 1.2 V




PCI Express System Board(Tx) Test Report

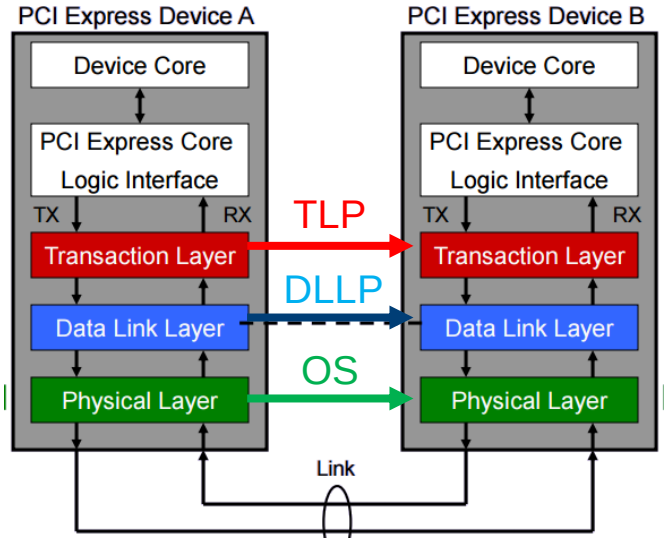
8.0GT PCIe 3.0 Signal Quality(4.3.3.13) - Base 4.8.9 Preset #0 - Min Transition Eye Height



PCI Express

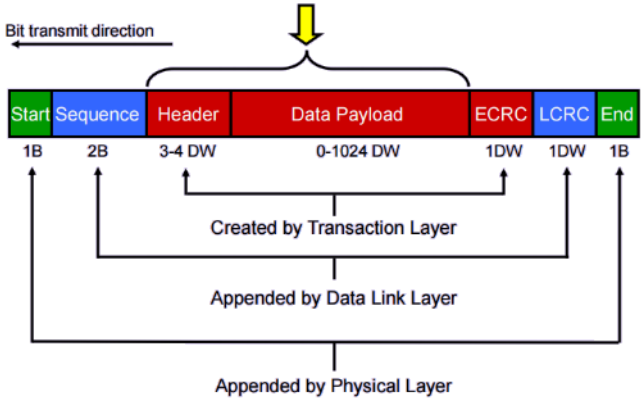
PROTOCOL TRIGGER & DECODE

PCI EXPRESS PROTOCOL LAYERS

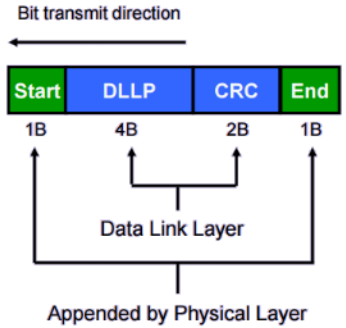


- OS – Ordered Set
- DLLP – Data Link Layer Packet
- TLP – Transaction Layer Packet

TLP

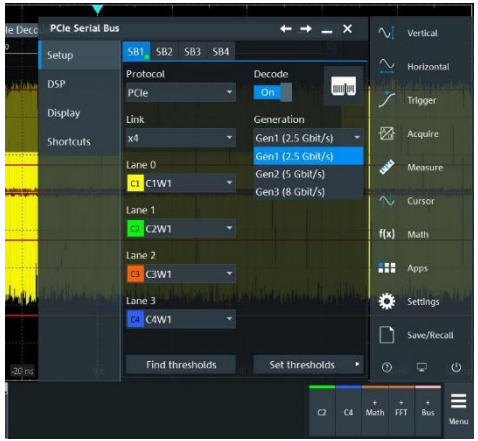


DLLP

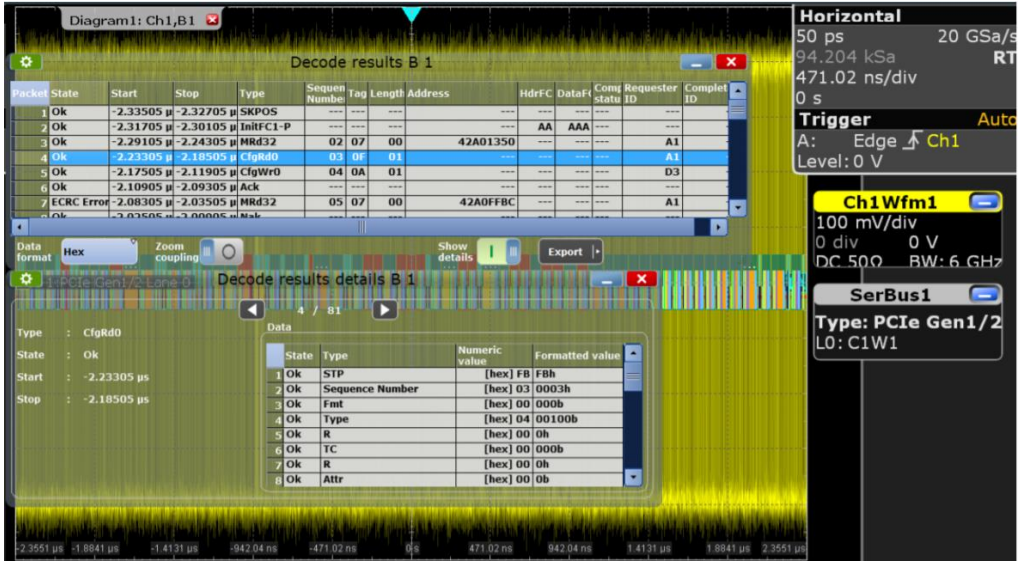


OS

PCI EXPRESS
PROTOCOL TRIGGER & DECODE SOLUTION

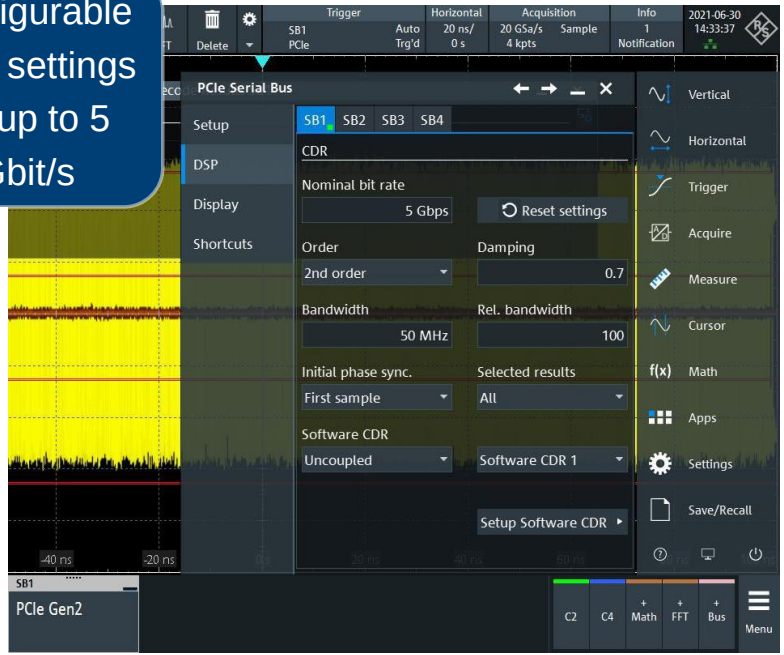


- R&S®RTO/P-K72 and R&S®RTP-K73
- Full support up to 8 Gbit/s and x4 link size
- Predefined or user selectable bit rates
- Configurable DSP settings
- Reliable triggering on protocol detail
  - Transaction Layer Packets (TLP)
  - Data Layer Packets (DLLP)
  - Ordered Sets
  - Errors
- Selectable decoding layer: bits, Scrambled or Descrambled 8b10b word, final protocol layer
- Powerful search capabilities



PCI EXPRESS
RELIABLE DECODE

Configurable CDR settings for up to 5 Gbit/s



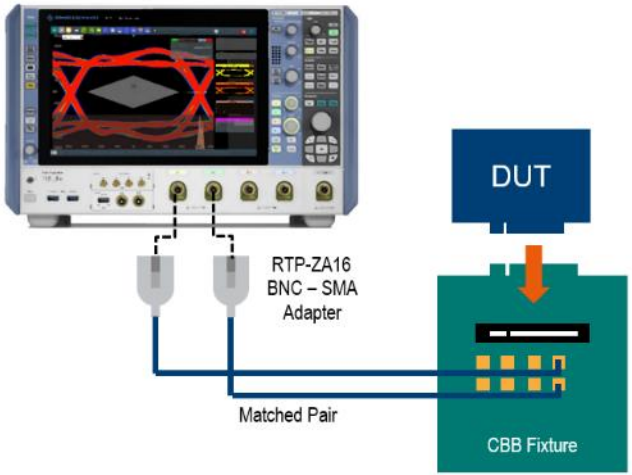
Configurable Equalization settings for 8 Gbit/s

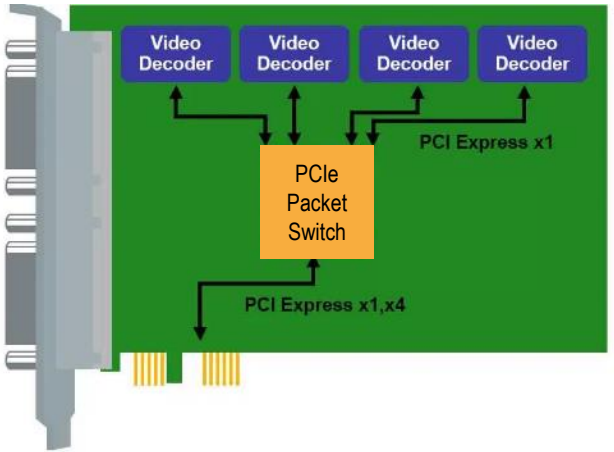
PCI Express

SIGNAL INTEGRITY DEBUG

PCI EXPRESS DESIGN AND DEBUGGING

- In standard design with socket interface, fixtures are designed to test interoperability
- Usually done in final phase I/O design
- PCIe link especially inter-chip will not be able to be tested with standard fixtures
- Quantifying design quality will be an on-going process to validate performance





THE R&S PROBE PORTFOLIO

High voltage

Single ended compact

Differential modular

EMC near field

Power rail

Standard

Broadband

Differential High voltage

Differential compact

Precise V&I Multichannel

Current

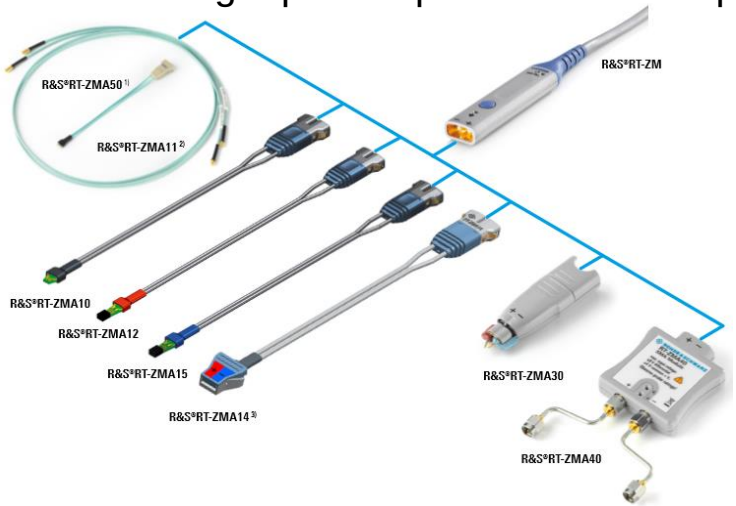
PASSIVE

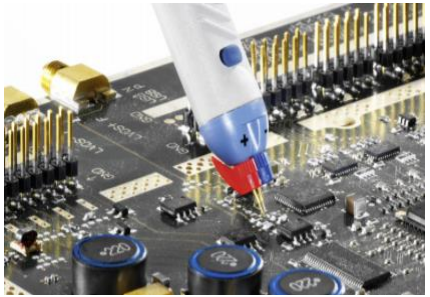
ACTIVE

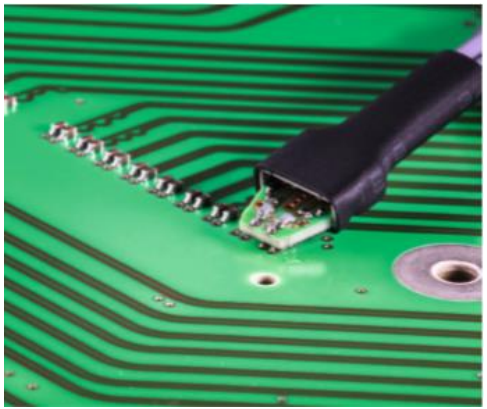
SPECIALIZED

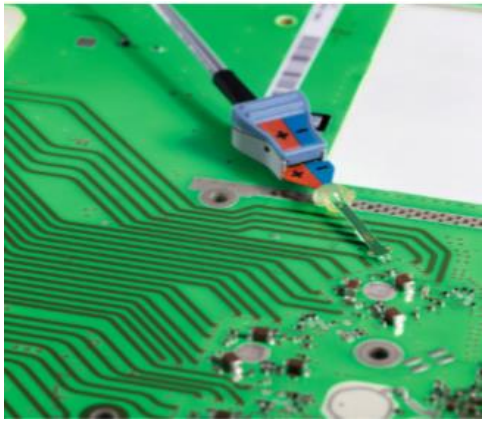
PCI EXPRESS
DEBUGGING – ACCESS TO THE SIGNAL

- 13 GHz modular probes – with appropriate tips
- Plan test points
- Soldering with short leads for best signal fidelity
- Browser flexible probing
- Note: select right probe tip for correct compensation





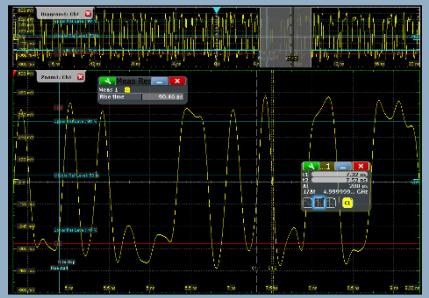




PCI EXPRESS
DEDICATED TESTS FOR VERIFICATION & DEBUG

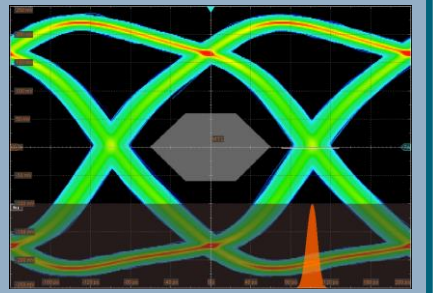
Timing and Level Measurements

- Verify level and timing of the signal
- Use cursors or automated measurements



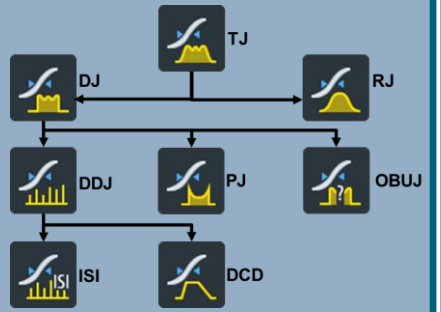
Eye Diagram

- Fast update rate for statistical confidence
- Clock-Data-Recovery (CDR)
- Mask tests, Histogram



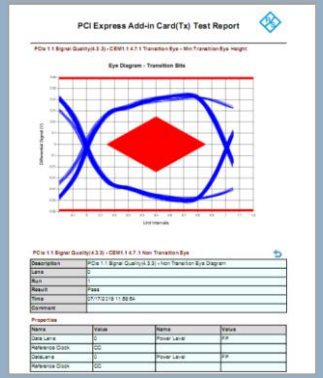
Jitter Analysis

- Break-down of jitter and noise into individual components for characterization & debugging



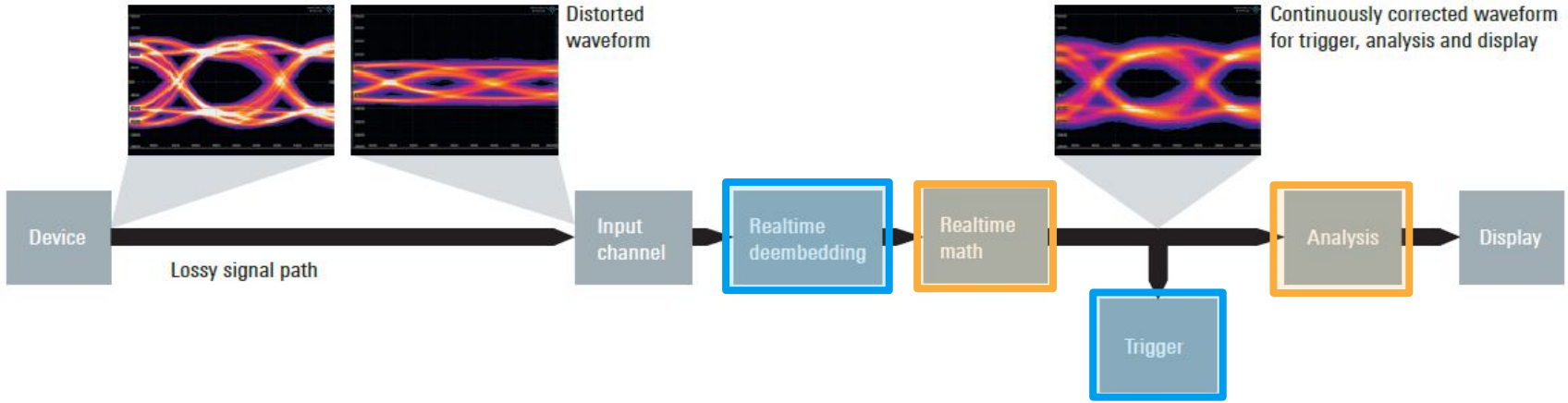
Automated Compliance Tests

- Verify compliance of the physical layer to interface standards and report results



REALTIME SIGNAL INTEGRITY UP TO 16 GHZ

Realtime Deembedding Architecture



Fast debugging
- ► 20 GSa/s: 750k wfm/s
- ► 40 GSa/s: 300k wfm/s

RT-Deembedding:
- ► Realtime transmission loss compensation

Realtime Math:
- ► V_{Diff} signal
- ► V_{CM} signal

Digital Trigger System:
- ► 16 Gbps Serial Trigger/CDR
- ► 25 ps glitch trigger

HW accelerated analysis:
- ► Mask Test
- ► Histogram

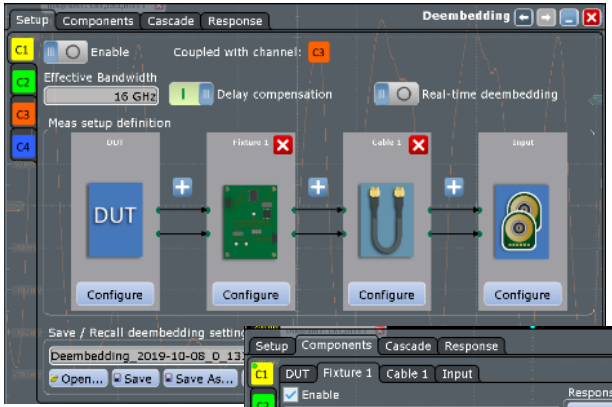
No time consuming post-processing

DEEMBEDDING MADE EASIER

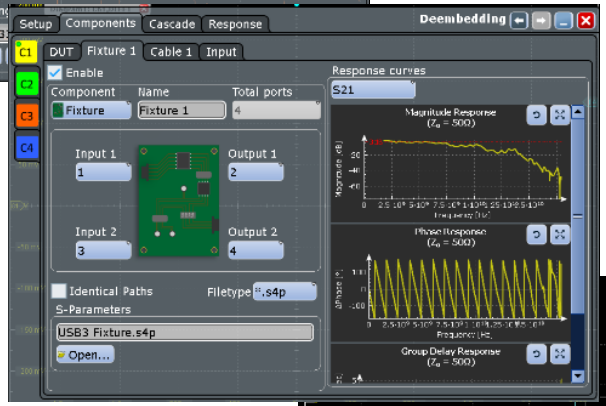
- Option RTO/P-K121 + RTP-K122
  - SW and HW (Realtime)
- Applied during acquisition
- Trigger on deembedded signal
- No update rate change
- Proven Cable / Probe
  - removes transmission loss effects
  - B7 pulse source

Condense this slide to incl. TDR/DT, jitter, HWCDR

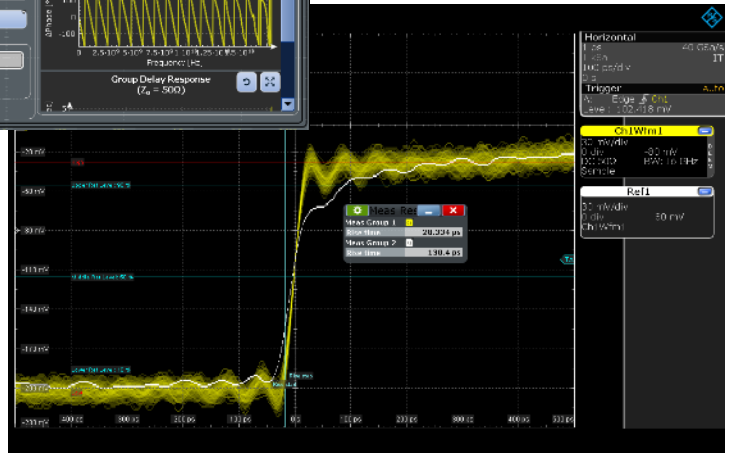
1. Define System Parameters



2. Import S-parameter



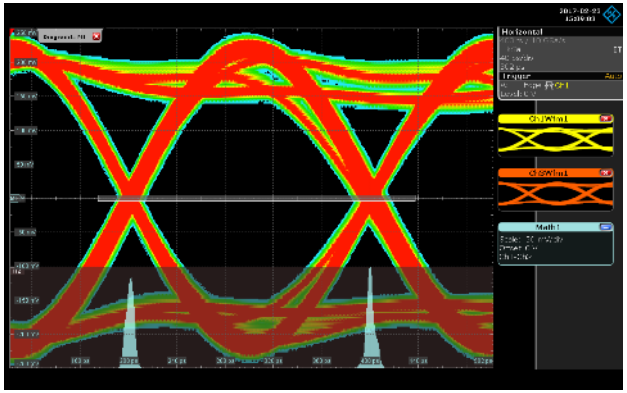
3. Observe deembedded response



PCI EXPRESS
REAL TIME EYE ANALYSIS

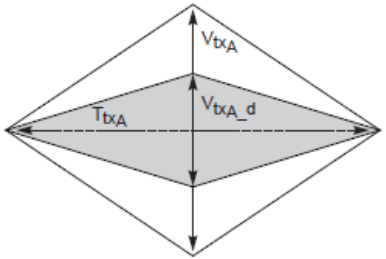
- Further debugging tools:
  - Serial pattern trigger
  - HW CDR
  - Real-time mask testing

5.0 Gbit/s

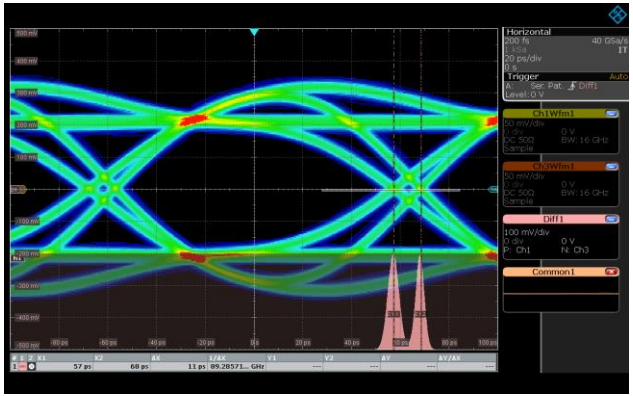


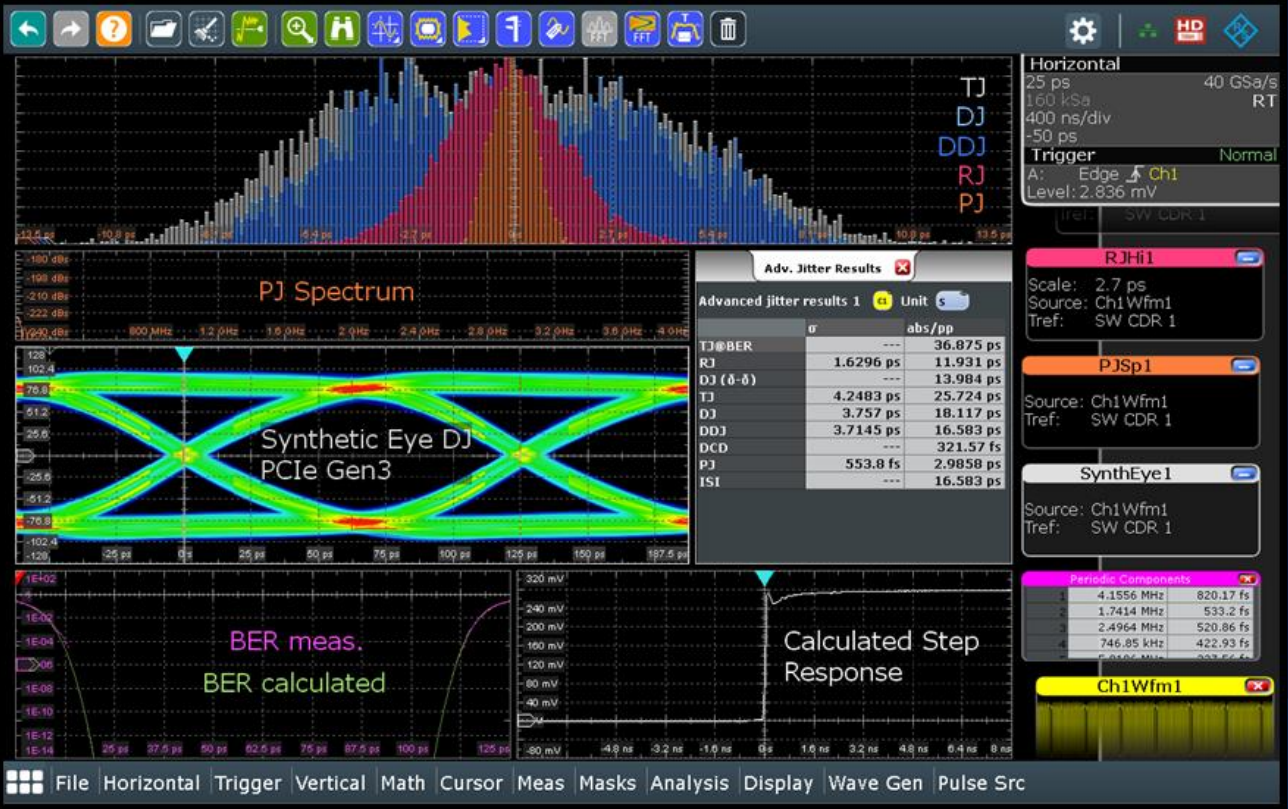
Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	514	1200	mV	Notes 1, 2, 5
V_{TXA_d}	360	1200	mV	Notes 1, 2, 5
T_{TXA}	287		ps	Notes 1, 3, 5
$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$		56.5	ps	Notes 1, 4, 5



8.0 Gbit/s





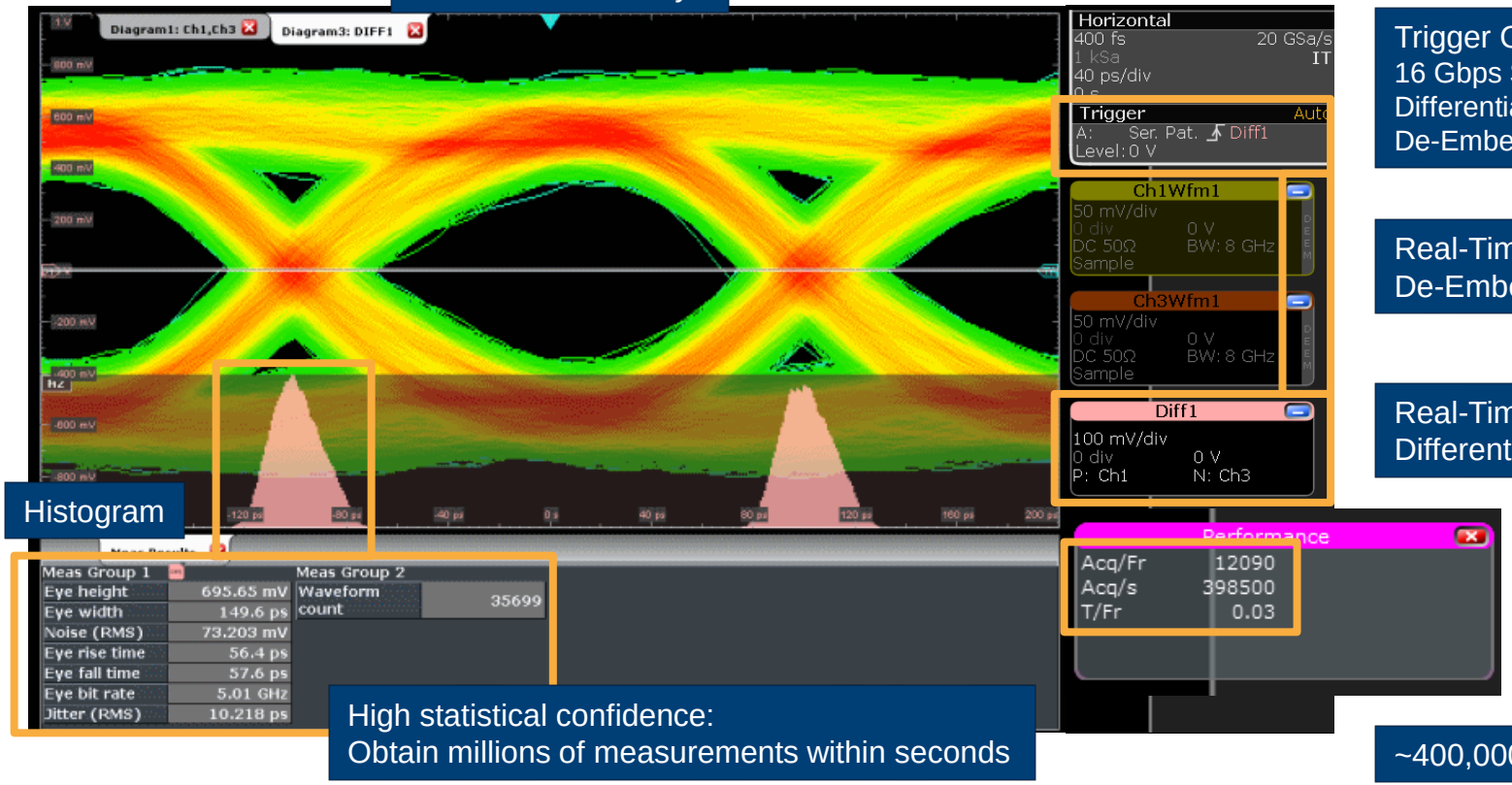
SIGNAL MODEL JITTER K133

- RTO and RTP
  - Up to 16 GHz
- Results
  - Histograms
  - PJ Spectrum & Comps
  - Eye diagram
  - Result table
  - BER bathtub
- **Step response**
  - **Only R&S Signal-Model!**

TDR/TDT ANALYSIS

- Options
  - TDR/TDT analysis option (RTP-K130)
  - 16 GHz differential pulse source (RTP-B7)
- Powerful capabilities
  - Integrated pulse source
  - Guided calibration
  - Fast results
  - Browser accessories (PacketMicro)
- Typical application
  - PCB debugging

Clock Recovered Eye



Histogram

High statistical confidence:
Obtain millions of measurements within seconds

Trigger On:
16 Gbps Serial
Differential Signal
De-Embedded

Real-Time
De-Embed

Real-Time
Differential Math

~400,000 UI/sec

REAL TIME EYE DIAGRAM TESTING

SUMMARY

- Compliance testing for PCIe is important for PCISIG for system interoperability
- Beyond compliance it is also critical to be able to look at:
  - Decoding
  - Serial Triggering
  - Eye Diagram testing
  - Deembedding
  - Impedance control via TDR / TDT
  - Jitter analysis
- **All in one instrument!!**

Find out more

www.rohde-schwarz.com

Thank you!

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Make ideas real