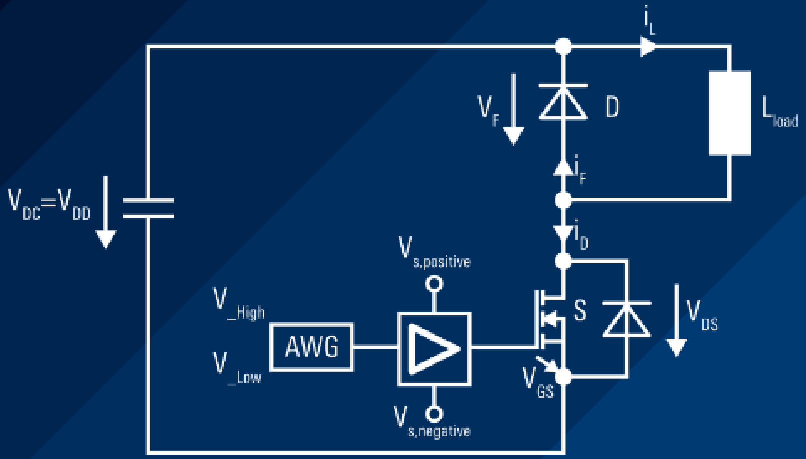
2021 R&S POWER ELECTRONICS DAY

掌握雙脈衝測試原理和方法

CS Wong 黃俊雄
Oscilloscope Product Manager Asia
亞洲示波器產品經理



ROHDE&SCHWARZ

Make ideas real

2021

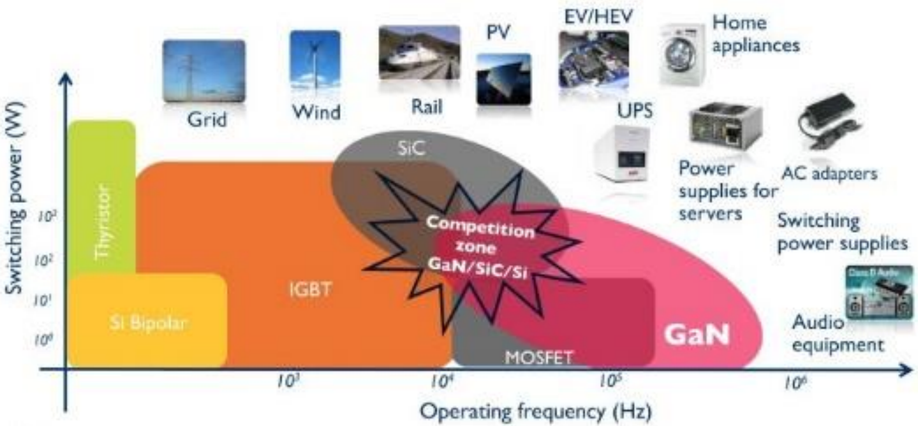
新一代
高功率電子

Wide bandgap technology (SiC 碳化矽 and GaN 氮化鎵) is driving the market adoption and paving way to new design and testing requirements

- ► Electrification of vehicles
- ► Powering data centers
- ► Green power
- ► Energy storage

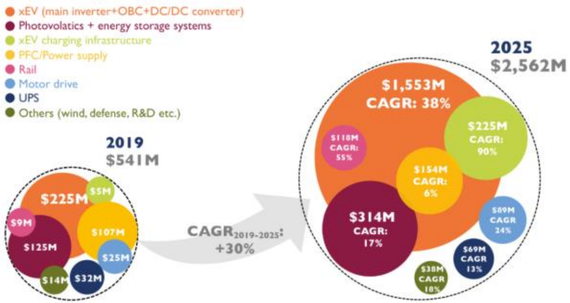
Power vs frequency on electronics: device technology positioning in 2020

(Source: Power GaN: Epitaxy, Devices, Applications, and Technology Trends report, Yole Développement, 2019)



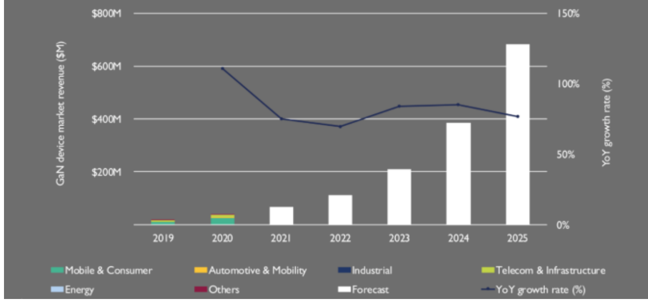
2019-2025 power SiC market forecast split by application

(Source: Power SiC: Materials, Devices and Applications 2020 report, Yole Développement, 2020)



Power GaN device market forecast between 2019 and 2025

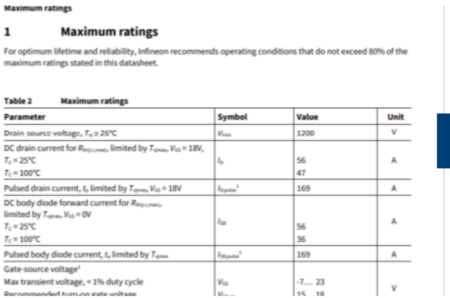
(Source: Compound Semiconductor Quarterly Market Monitor, Q4 2020, Module I, Yole Développement)



Source: Yole Development

DOUBLE-PULSE TESTING 雙脈衝測試
MANY USE-CASES 應用

Datasheet generation → **Module production test** → **Module selection** → **Converter Design**



Maximum ratings

1 Maximum ratings

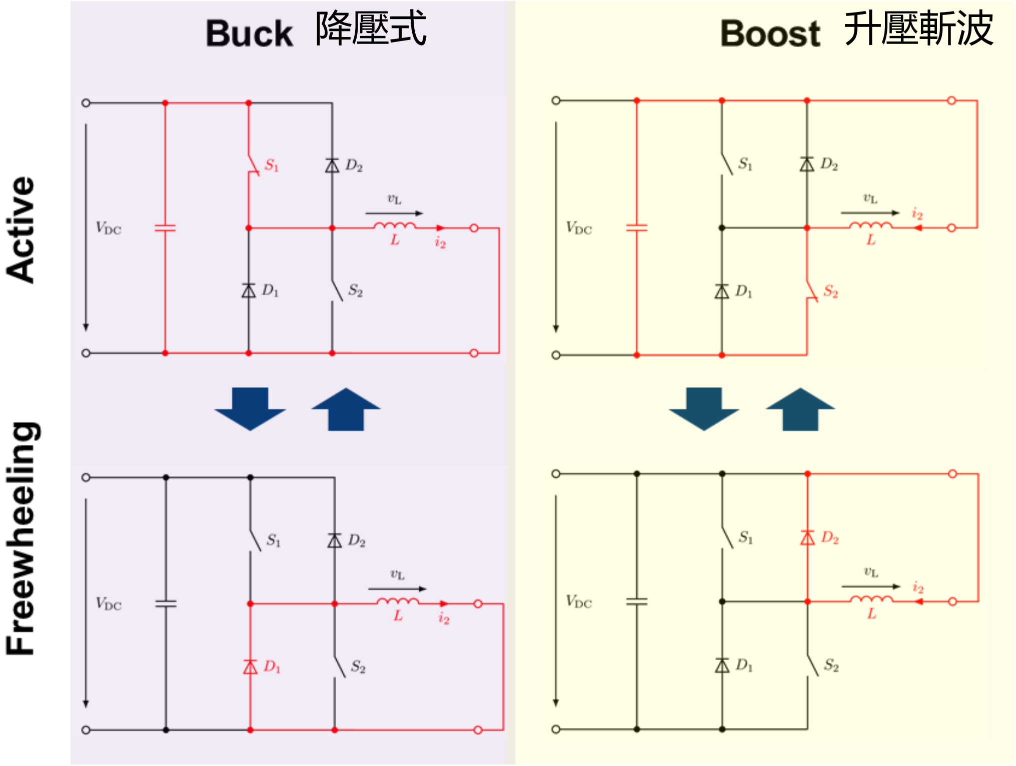
For optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Table 2 Maximum ratings

Parameter	Symbol	Value	Unit
Drain source voltage, $T_{vj} \geq 25°C$	V_{DSS}	1200	V
DC drain current for $R_{th(j-c,max)}$, limited by T_{vjmax}, $V_{GS} = 18V$, $T_C = 25°C$ $T_C = 100°C$	I_D	56 47	A
Pulsed drain current, t_p limited by T_{vjmax}, $V_{GS} = 18V$	$I_{D,pulse}$[1]	169	A
DC body diode forward current for $R_{th(j-c,max)}$, limited by T_{vjmax}, $V_{GS} = 0V$ $T_C = 25°C$ $T_C = 100°C$	I_{SD}	56 36	A
Pulsed body diode current, t_p limited by T_{vjmax}	$I_{SD,pulse}$[1]	169	A
Gate-source voltage[2] Max transient voltage, < 1% duty cycle Recommended turn-on gate voltage	V_{GS}	-7... 23 15 ... 18	V

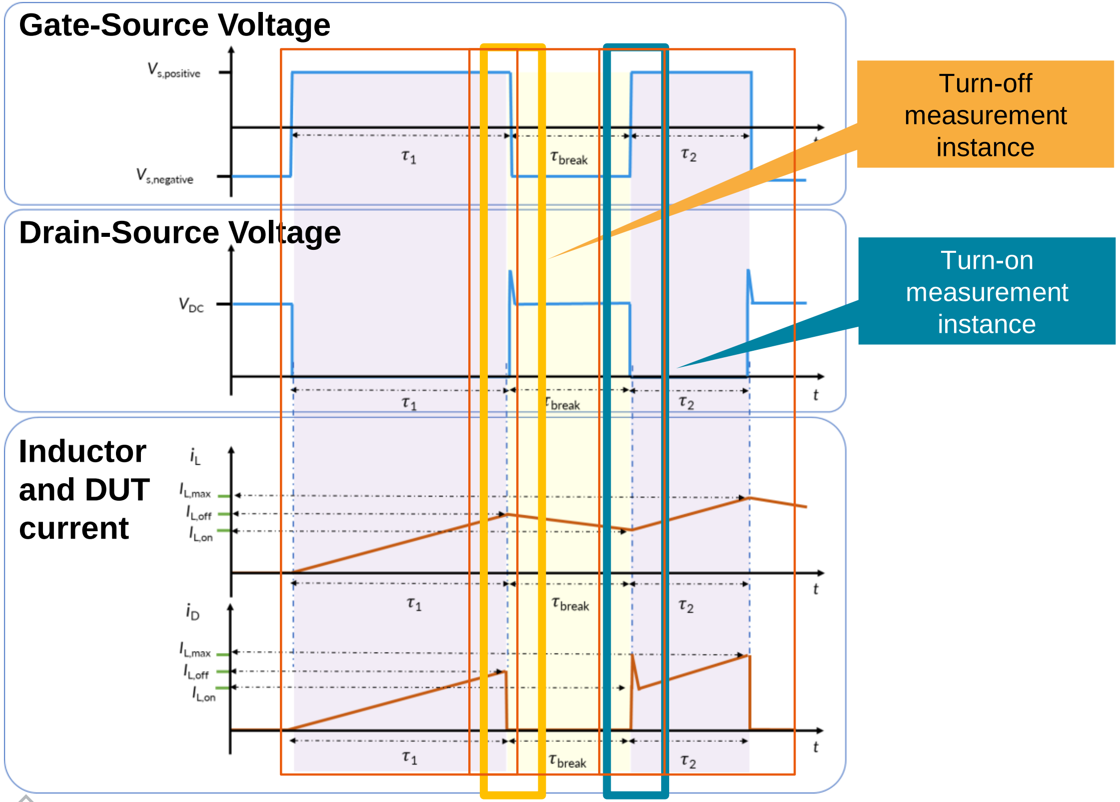
WHY DOUBLE PULSE TESTING 雙脈衝測試主要原因

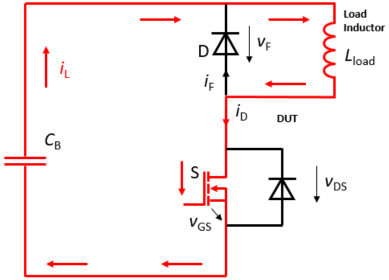
EXAMPLE: TWO-LEVEL CONVERTER 雙準位轉換器



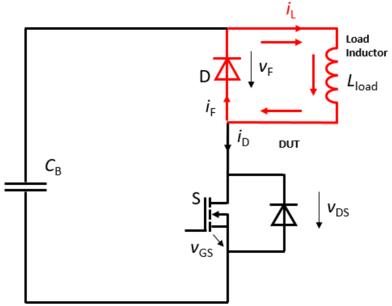
- **A double-pulse test allows to cover all four basic operation modes**
- **All main parameters can be measured**
  - Switching losses 開關損耗
  - Reverse recovery losses 反向恢复損耗
  - Switching times
    - Turn-on and turn-off delay time
    - Rise and fall times

THEORY AND TEST PROCEDURE
原理及測試步驟

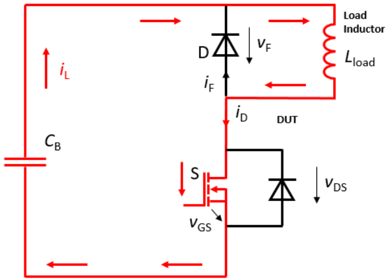




Interval τ_1
Inductor is "charged"



Interval τ_{break}
Turn-off measurement at target current



Interval τ_2
Turn-on measurement at target current

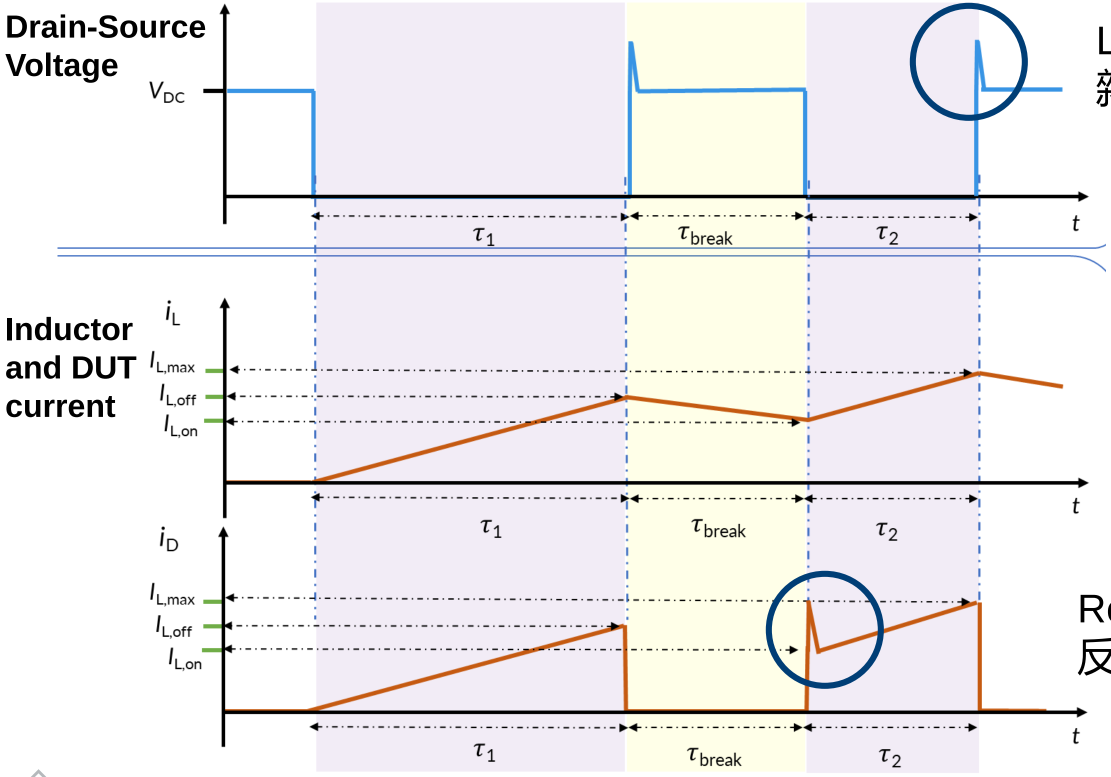
WHY NOT SINGLE PULSE?
單脈衝行不行?

- In most power devices, inductive load is bigger. When DUT turn off, inductive current continue to flow, causing diode to turn ON.

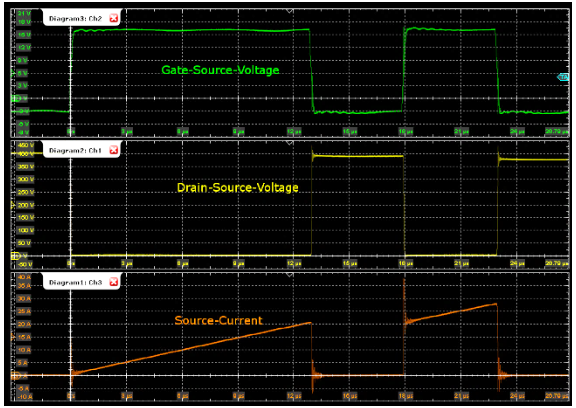
- Turning ON the DUT at time stage, the diode will have a reverse recovery process. This is unavailable if we only do a single pulse test.

- Double pulse test is hence more practical and realistic

BASIC OBSERVATION WAVEFORM
基本實驗波形

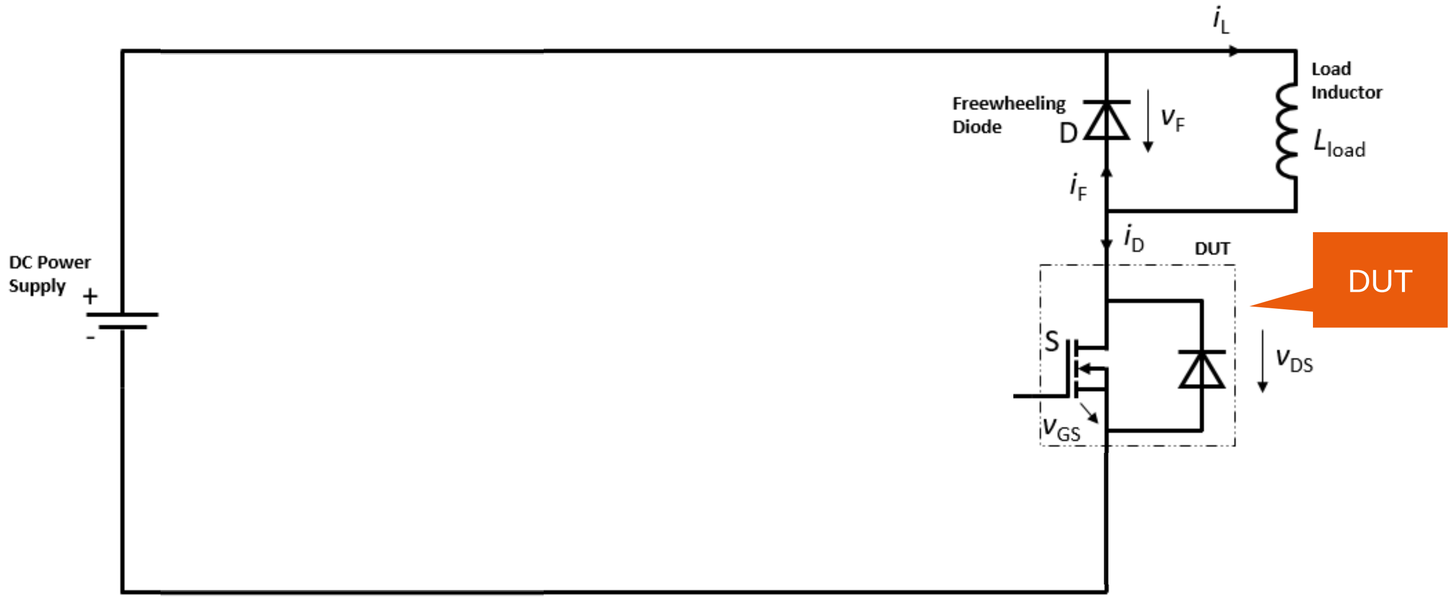


Loop inductances voltage spikes
雜散電感導致的電壓尖峰

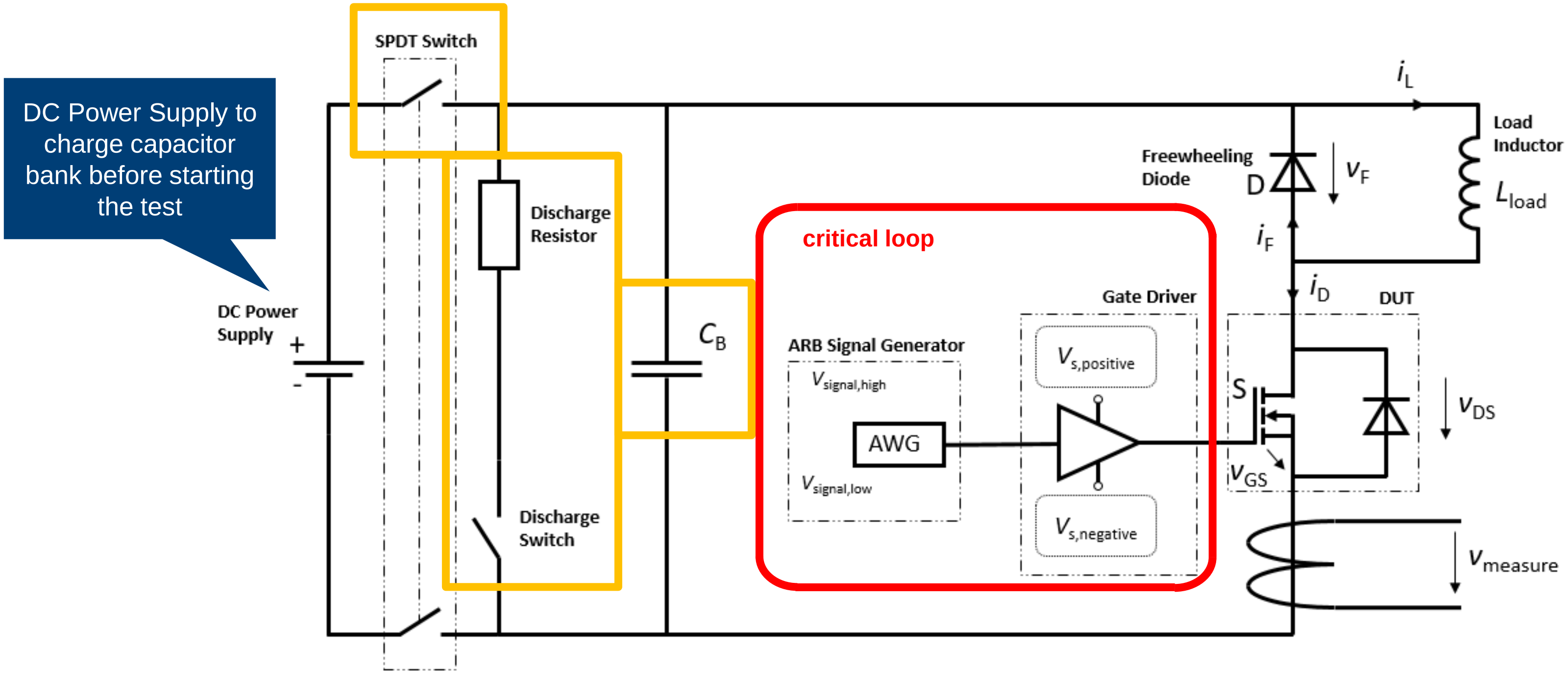


Reverse Recovery Current
反向恢復電流

TYPICAL SETUP
建立雙脈衝測試平臺



TYPICAL SETUP
建立雙脈衝測試平臺

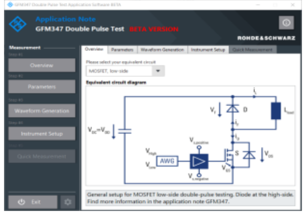


TYPICAL SETUP
建立雙脈衝測試平臺

HMF2550 ARB Generator

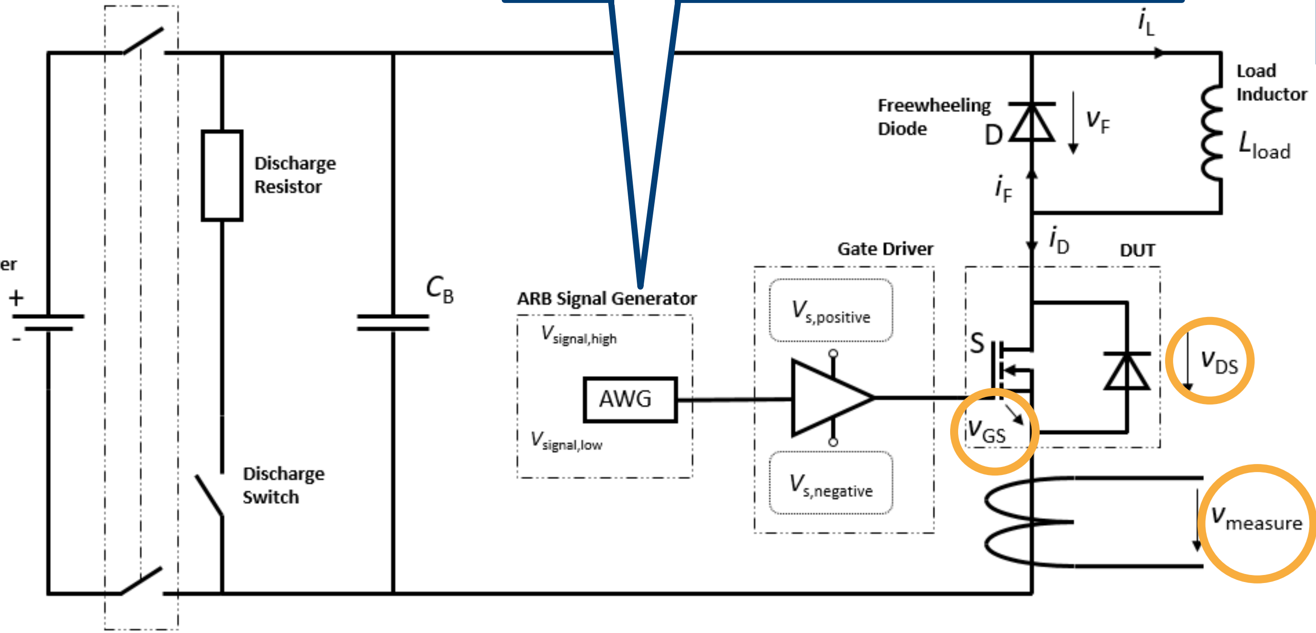
RTM3000 Oscilloscope

DBT SW



DC Power Supply to charge capacitor bank before starting the test

Load inductor, “stores” current for the actual test



Floating output important!

RTO2000 Oscilloscope

RTM3000 Oscilloscope

CIRCUIT CONSIDERATION
雙脈衝測試搭建參數

- **Components used in double-pulse test have massive influence on test result**

- **Load inductor**
  - Trade-off between optimum pulse current and constant current through break
  - Duration of first pulse should be below 100us to avoid self-heating of semiconductor
  - Low parasitics very important, usually air coils used

Maximum inductance

$$L_{\text{load}} \leq \tau_1 \cdot \frac{V_{\text{DC}}}{I_{\text{test}}}$$

Minimum inductance

$$L_{\text{load}} \geq -\left[R_{\text{s}} \cdot \tau_{\text{break}} \cdot \left(\frac{1}{\ln\left(\frac{\Delta I}{I_{\text{test}}+\frac{v_{\text{F}}}{R_{\text{S}}}}+1\right)}\right)\right]$$

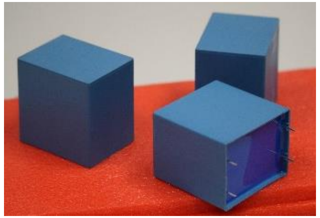
CIRCUIT CONSIDERATION
雙脈衝測試搭建參數

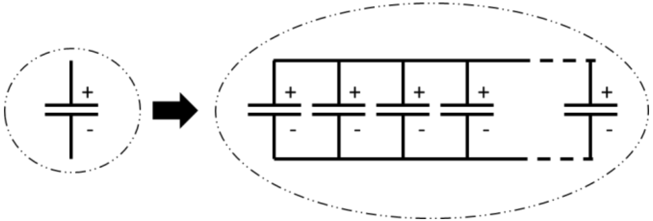
- **Components used in double-pulse test have massive influence on test result**

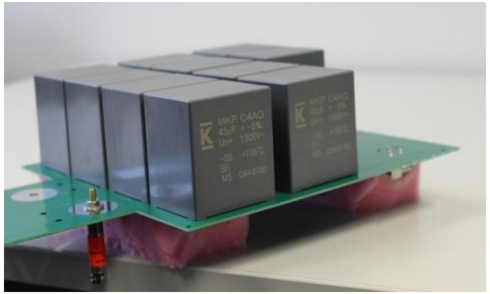
- **B) Capacitor bank**
  - Shall maintain DC-link voltage during test
  - Low parasitic inductance important
  - Multiple units with smaller capacitance are preferred
  - Film capacitors are usually the best choice

Minimum DC-link capacitor

$$C_B \geq \frac{L_{load} \cdot I_{test}^2}{2 \cdot V_{DC} \cdot \Delta V_{DC} - \Delta V_{DC}^2}$$

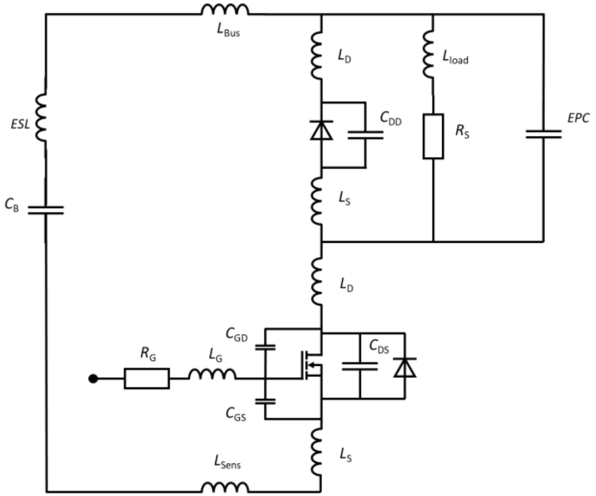






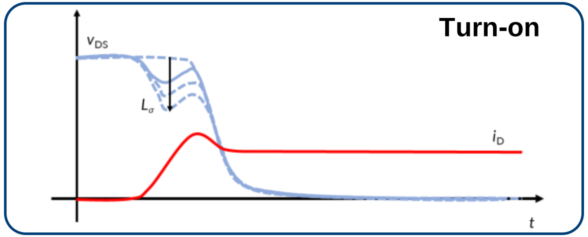
Small units in parallel decrease stray inductance

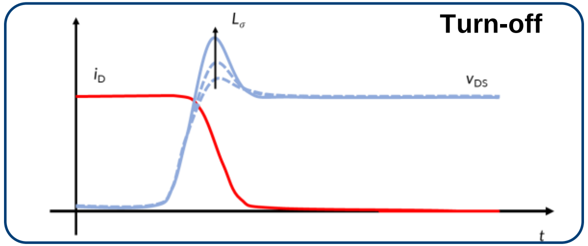
THE EFFECTS OF PARASITICS
散雜電容電感的影響



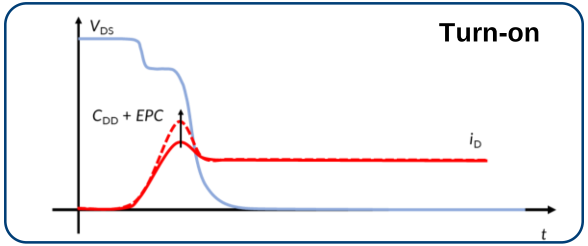
- ▶ Parasitic components cause voltage spikes and ringing, EMI interference and reliability problems
- ▶ Parasitics in application do not match with datasheet setup
  → device losses differ additional testing required
- ▶ Stray inductance of utmost importance

Impact of stray inductance L_σ

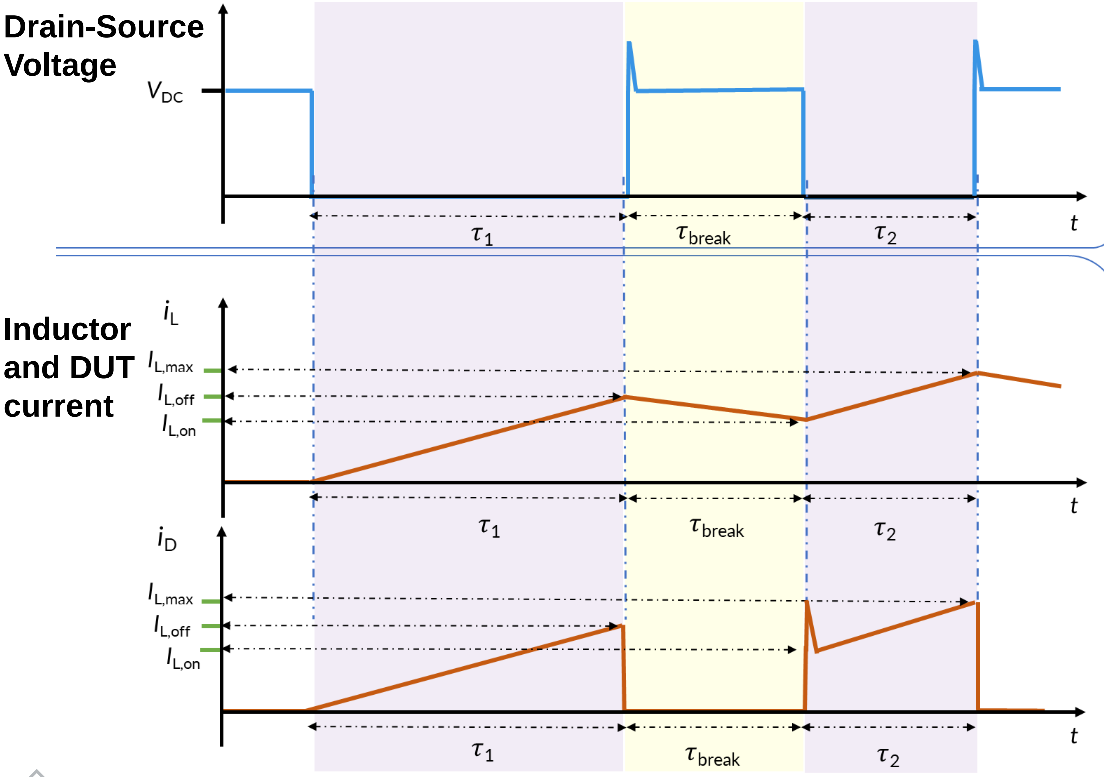


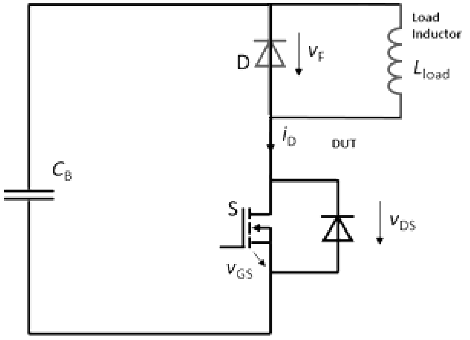


Impact of stored charge $C_{DD}+EPC$



SETTING UP THE PULSE
建立雙脈衝波形的特性





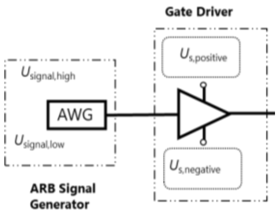
$$\tau_1 = L_{LOAD} * \frac{i_L}{V_{DC}}$$

τ_{break} is set long enough for the voltage and currents to settle out

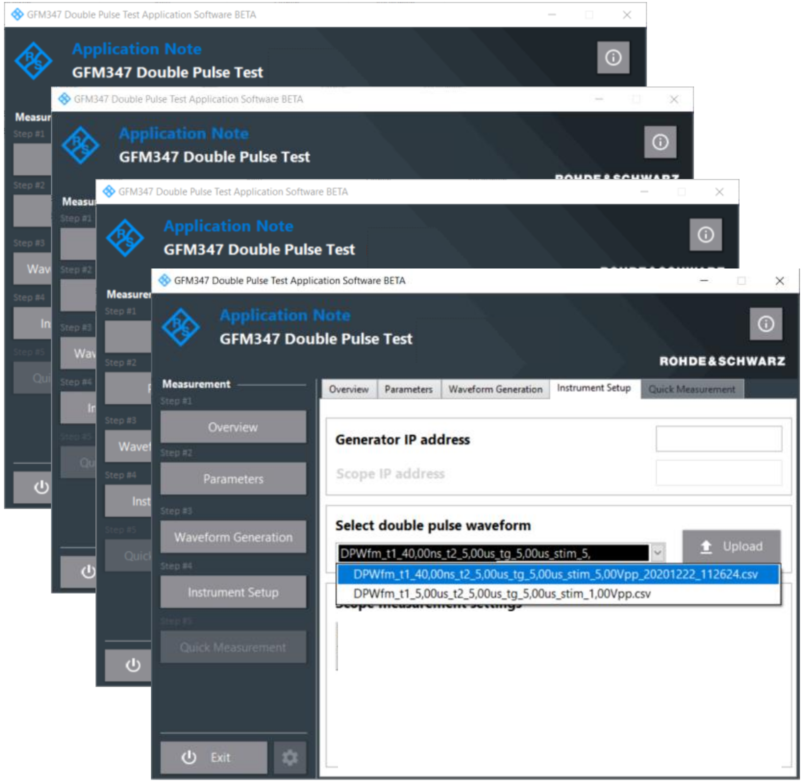
τ_2 usually short enough not to exceed the reverse bias SOA

$\tau_1 + \tau_2$ should not be too large to create self heating of the DUT

SETTING UP THE ARB WITH APP
建立任意波形軟體



- **Important considerations**
  - Clean turn-on procedure without any spikes
  - Right signal levels
- **Double pulse test App**
  - Create ARB waveform based on test parameters
  - Recall ARB waveforms using descriptive names
  - Directly upload to external ARB or oscilloscope
- **Tipp:** Always check ARB signal when creating new setup



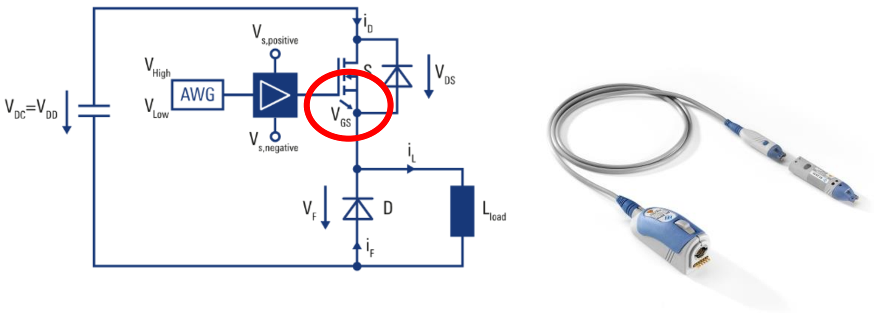
SETTING UP THE MEASUREMENT
測量搭配 – 電壓探棒篇

- **Passive probes are sufficient for floating setups**
  - Typically possible for device characterization setups
  - Care has to be taken on any (unintentional) grounding

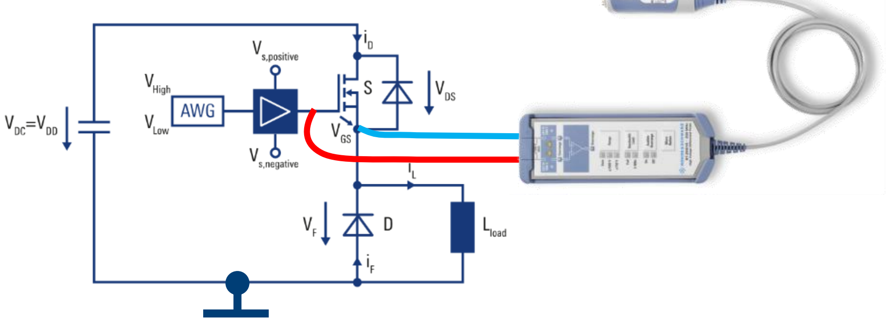
- **Broadband differential probes are an attractive alternative for floating setups**
  - Very high bandwidth of up to 1 or 2 GHz
  - Very low loading (~ 1pF)
  - Input voltage range of +/-50V DC with 10:1 attenuator

- **High-voltage differential probes are necessary if system-under-test is grounded**
  - Typically the case for prototypes
  - Provide CMRR to suppress switch-node signal

Floating High-side DUT

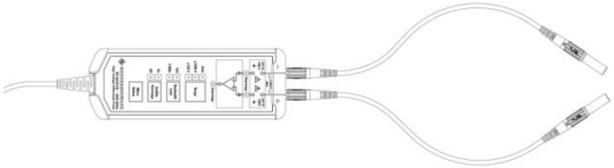


Grounded High-side DUT



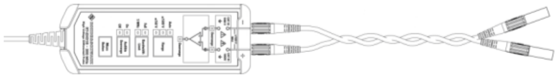
VOLTAGE PROBING PRACTICAL ASPECTS
探棒實測考量

- **Twisted of untwisted leads of differential probes**



pro	minimizes the capacitive load on the measuring point
con	interferers are looped in

Usually the better option

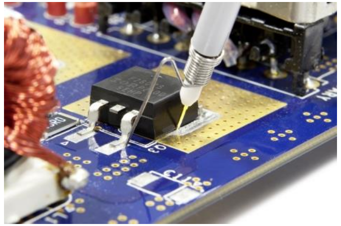


pro	interferers are minimized
con	greater load on the measuring point

Single-ended input capacity	**RT-ZHD16 + meas. leads**
untwisted	9 pF
twisted	12 pF

Rule of thumb: The differential input capacitance is approx. half the single ended capacitance

- **Passive probe connectivity**
  - Avoid long ground leads
  - Wrap ground leads if possible
  - Us CM-chokes



VOLTAGE PROBING CMRR
差分探棒共模抑制

► **Key parameter is rise time**

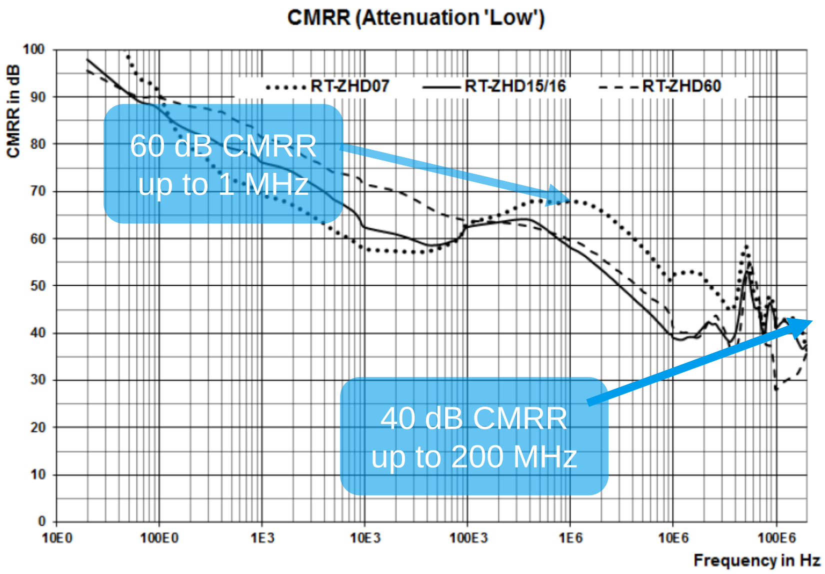
$$t_{rise} \approx \frac{0.4}{BW}$$

Rise time	400 ns	40 ns	4 ns
Bandwidth	1 MHz	10 MHz	100 MHz

► **Switch-node voltage determines required CMRR**

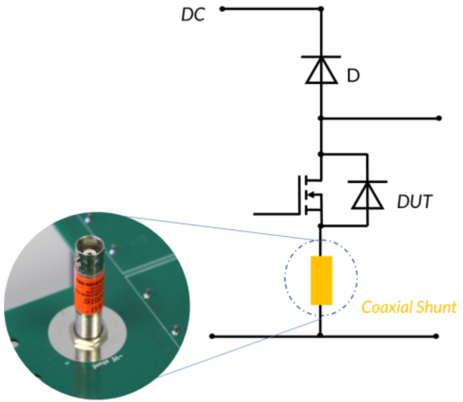
Switch-node voltage swing	10V	100V	1000V
Required CMRR for 1 V remaining CM signal	20dB	40 dB	60 dB

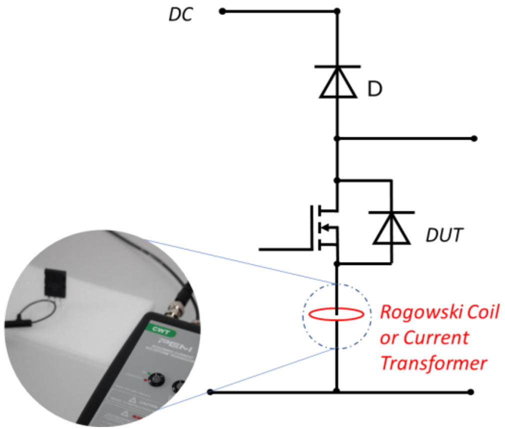
Typical performance of HV-Diff Probes



SETTING UP THE MEASUREMENT
測量搭配 – 電流探棒篇

- ► **Basic requirements**
  - – High measurement bandwidth
  - – Sensor as small as possible
  - – Low insertion inductance



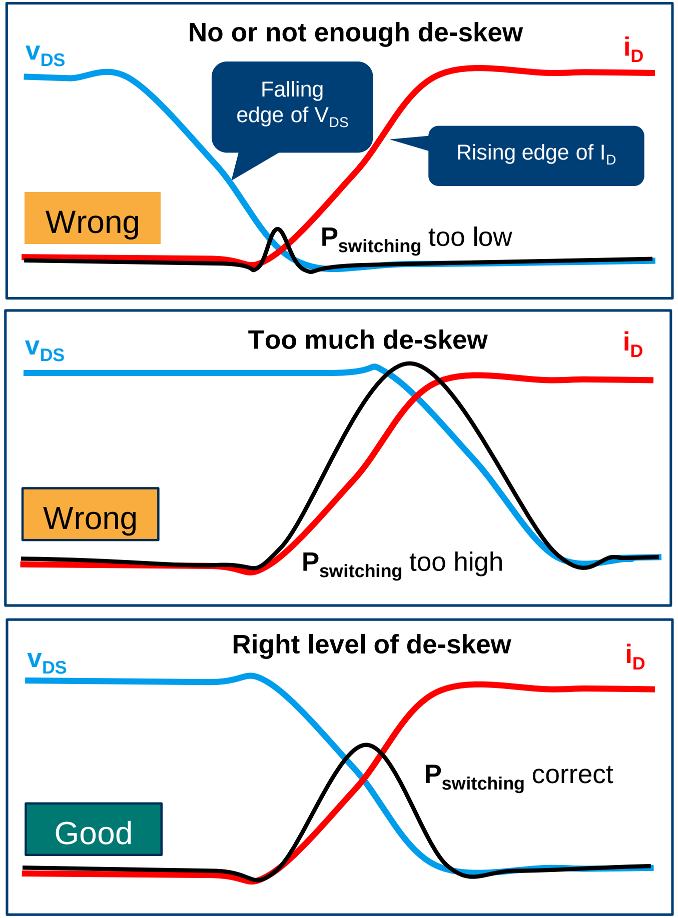


	Coaxial shunt	Rogowski probe	Current transformer
Pro's	• Very high bandwidth (2 GHz) • DC-measurement capability • Very low insertion inductance	• Physically small, no "design-in" of sensor necessary	• High bandwidth (~200 MHz) • High current possible
Con's	• Limited maximum current • Design-in of sensor necessary	• Limited bandwidth (typically 30-50 MHz but recently also higher bandwidth up to 100 MHz available) • Limited accuracy	• Design-in of sensor necessary • Large sensor with core, limits the possibility to have low-insertion inductance designs

DESKEW BASIC
相差校正

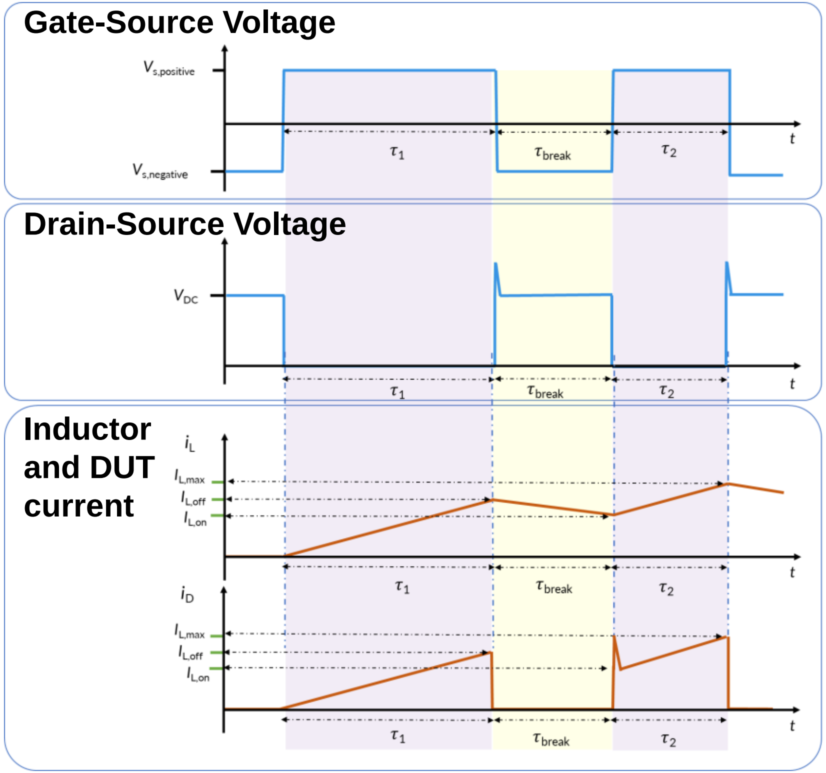
- **Voltage and current probes have different group delay**
- **Examples**
  - High voltage differential probe: ~8 ns group delay
  - Clamp-on current probe: ~15 ns
  - Small loop Rogowski probes: ~12 – 20 ns
- **For accurate switching loss measurements the delay has to be compensated for (de-skew)**
  - Often de-skew fixtures used but for double-pulse testing often not practicable

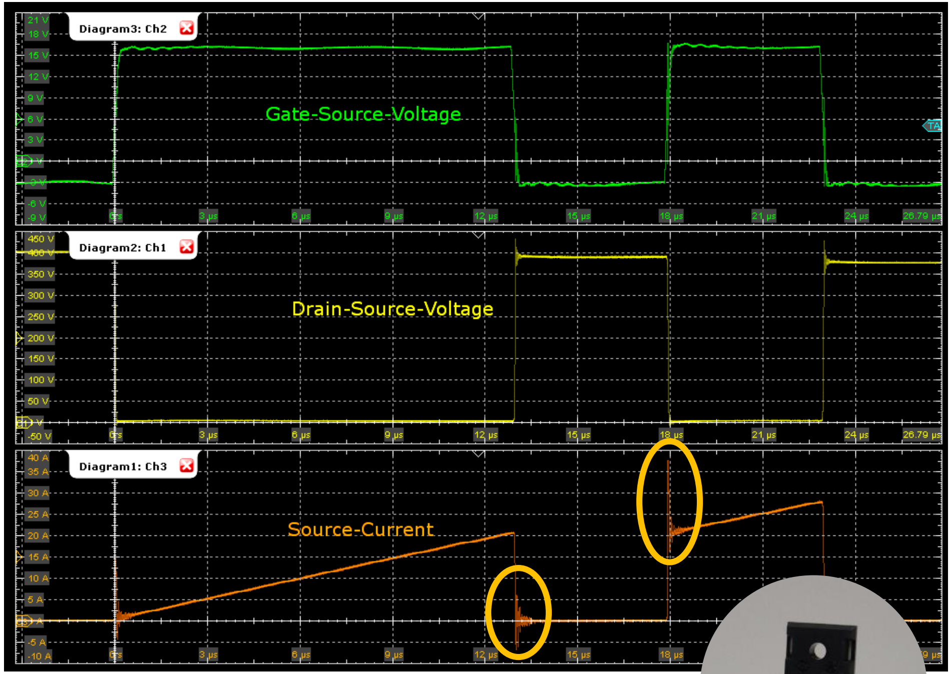
RT-ZF20 Power Deskew Fixture

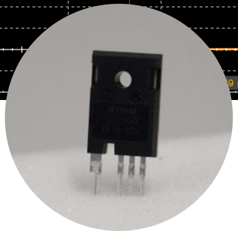


A PRACTICAL EXAMPLE 實測案列

650V 4-PIN TO-247 SIC MOSFET (ROHM), 400V DC LINK

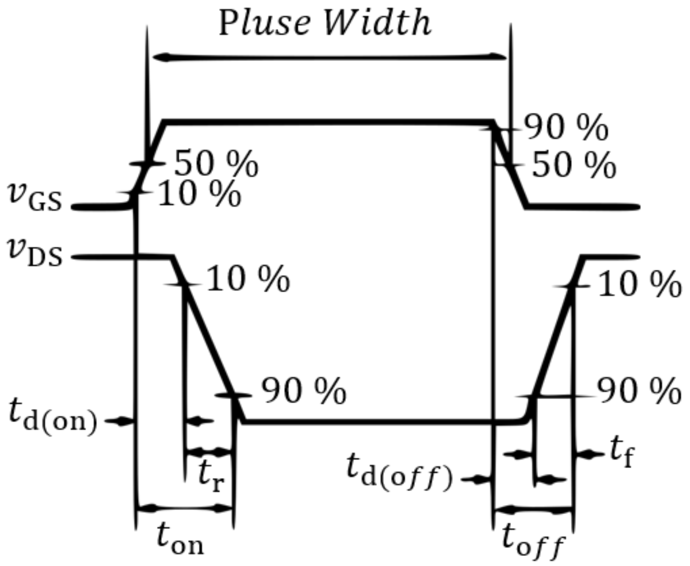




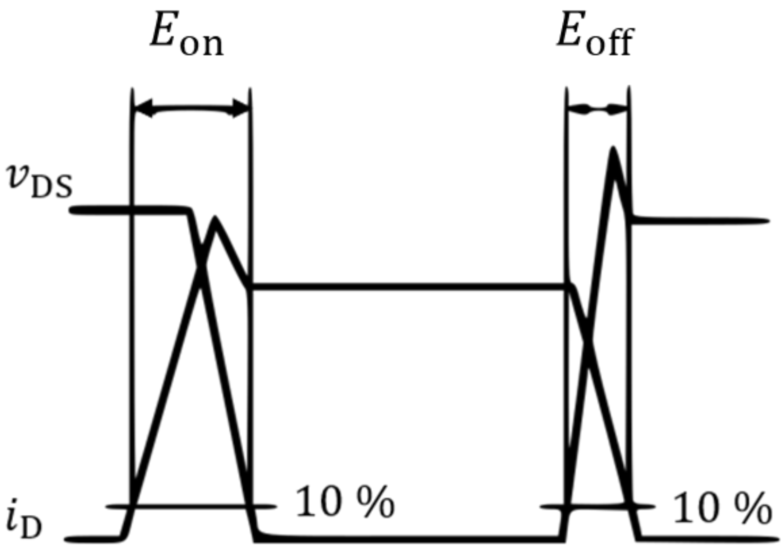


TURN-ON AND TURN-OFF TIMING AND ENERGY
開關過程時序與功率測量

Timings



Losses

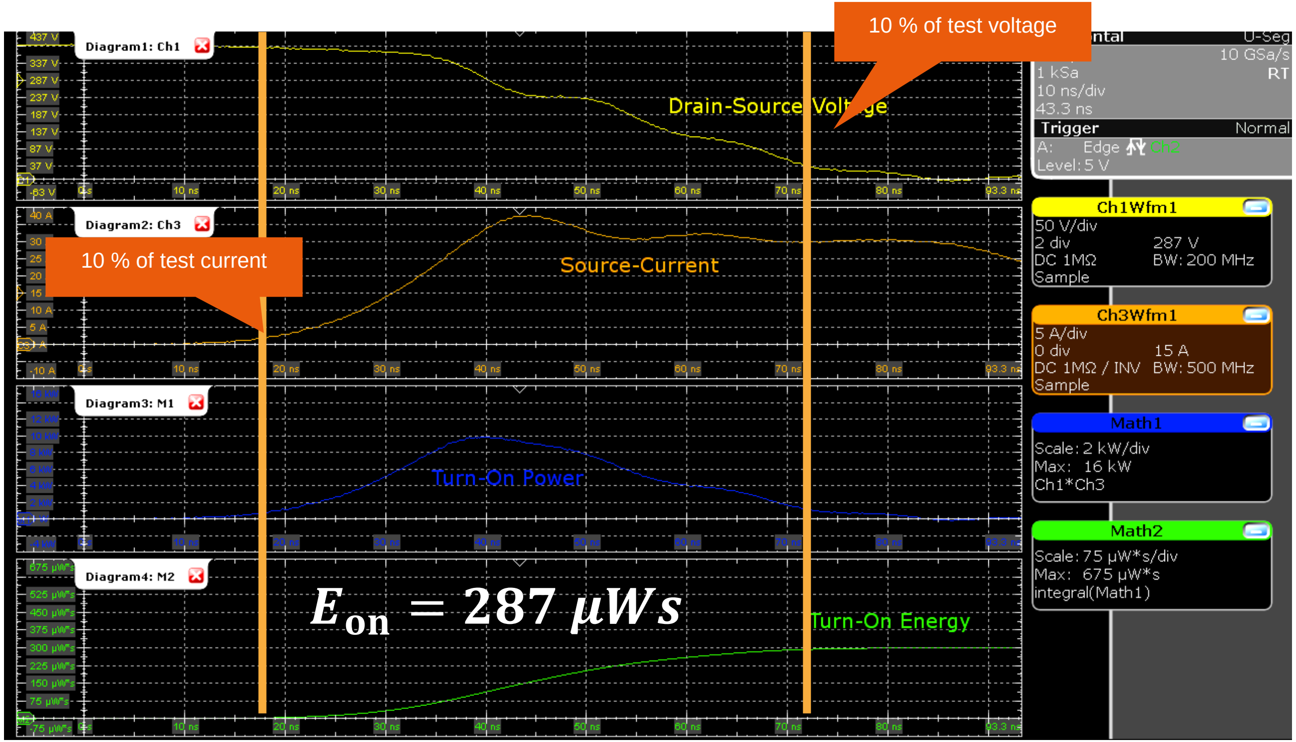


Definition from IEC 60747-8 for MOSFET

A PRACTICAL EXAMPLE 實測案列
TURN-ON ENERGY 打開功率

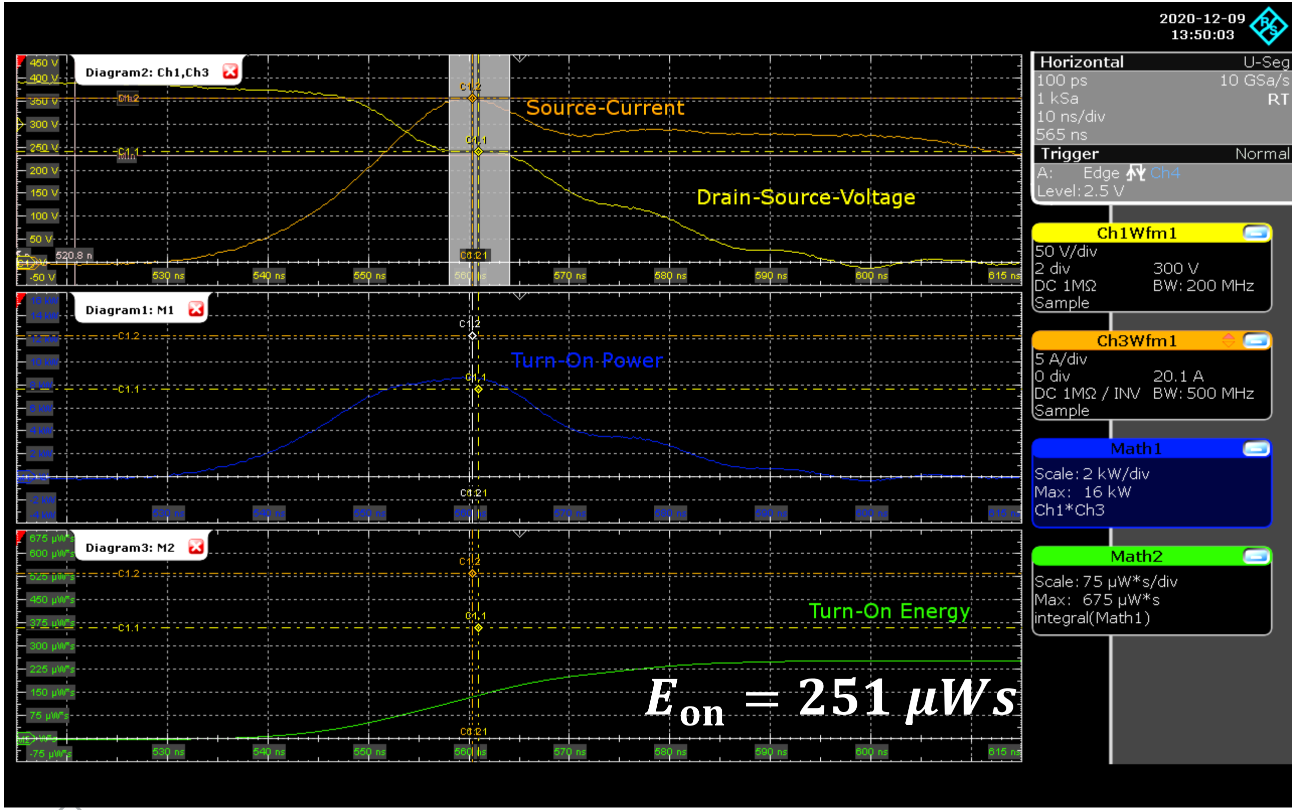
$$P_{\text{turn-on}} = v_{\text{DS}}(t) \cdot i_{\text{D}}(t)$$

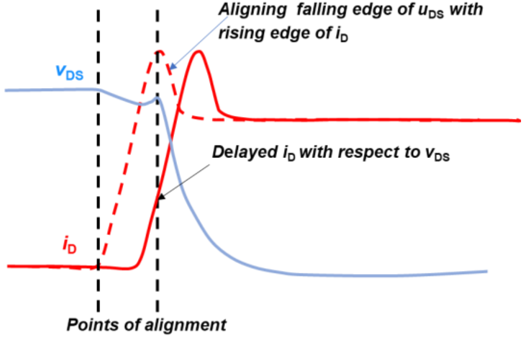
$$E_{\text{on}} = \int_{t_{\text{I}_{\text{test10}}}}^{t_{\text{V}_{\text{DC10}}}} P_{\text{turn-on}} \; dt$$

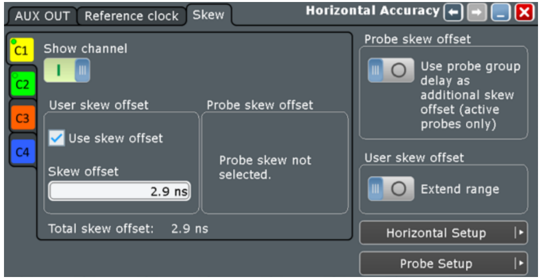


PRACTICAL EXAMPLE 實測案列

DE-SKEW 相位校正

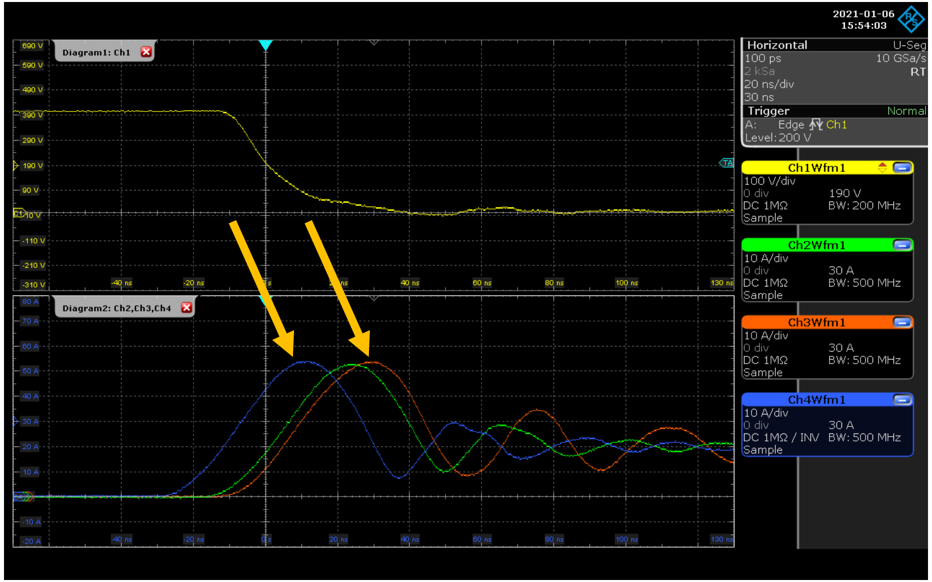




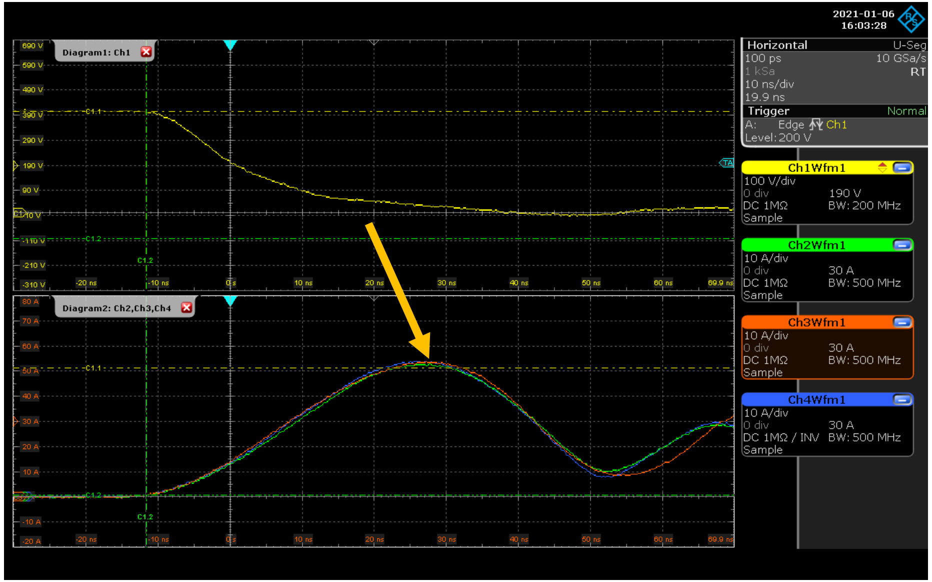


Deviation for this case: 14.3 %

PRACTICAL EXAMPLE 實測案列
CURRENT PROBE 電流探棒相位校正



No de-skew



With de-skew

► Conclusion: All variants match and can be used in this example

CONCLUSIONS 總結

- **Double-pulse testing starts with designing the setup**
  - Important topics are DC link capacitor design, inductor design, probing, grounding
- **Careful design of measurement important**
  - De-skew between current and voltage signals
  - Floating vs grounded setups
- **Design Automation requires comparability**

2021 R&S POWER ELECTRONICS DAY

THANK YOU
謝謝

For more information:
www.rohde-schwarz.com

ROHDE & SCHWARZ

Make ideas real