#### Advanced Deembedding – Accurate Fixture Modelling for Precise VNA Measurements of Non-Coaxial DUTs

Joern Pfeifer Application Engineer Vector Network Analyzer

#### **ROHDE&SCHWARZ**

Make ideas real



#### Jörn Pfeifer

- Senior Application Engineer Network Analyzer
- ▶ With Rohde & Schwarz since 2016
- R&S High Speed Data Link Expert Core Team Member
- Open Alliance Automotive Ethernet TC9 Working group contributing member



#### Agenda

- Introduction and Basics:
  S-Parameter and Calibration
- Fixture Compensation Methods Overview
- Advanced Deembedding and Fixture Modelling



#### Agenda

- Introduction and Basics:
  S-Parameter and Calibration
- Fixture Compensation Methods Overview
- Advanced Deembedding and Fixture Modelling



# Why use Advanced De-embedding Tools?

- VNA calibration usually calibrates up to end of coaxial cables
- But many DUTs do not have coaxial adapters
  DUT on PCB
  - Fixtures needed for special connectors
- Use of S-Parameter de-embedding to accurately compensate effects of fixtures or lead-ins





#### S-Parameter Basics Realization of Network Analyzer Test Set



Advanced Deembedding

#### **S-Parameter Basics**



Scattering parameters represent the relationship between the waves (a, b)

- ► S-Parameters represent reflection and transmission coefficients
- ► S-Parameters are dimension free (units disappear when ratioed)
- ► These coefficients are based on a defined line-system (usually 50 ohms)



#### **Balanced/ Mixed Mode S-Parameters**

Measure the balanced 2-port device as unbalanced 4-port device with unbalanced VNA. VNA Calculates mixed mode S-Parameters out of measured single ended S-Parameters.



Naming Convention: S mode res., mode stim., port res., port stim.

# VNA System Error Correction (Calibration): Coaxial Interface

- Correction of systematic errors of the instrument and cables (test set)
- Applying a set of known calibration standards at the desired reference plane to characterize the test set for correction in the calibration
- Typically used calibration kits consists of Through, Open, Short and Match standards (TOSM)

Also automatic calibration units available



#### VNA System Error Correction (Calibration): PCB Probes Example: Packet Micro PCB Probing Solutions

PACKETMICRO

- ► Precise positioning with XYZ0-Positioners
- ► Reference plane on the PCB with cal substrate
- Single ended & differential probes
- Microscope for close up view of your PCB
- Calibration substrate for TOSM calibration
- ► Up to 20 GHz



#### VNA System Error Correction (Calibration): PCB Probes Example: DVT Differential Probing Solutions

- ► 40/50/70 GHz differential probes, no ground
- ► Use of coaxial calibration
- Deembedding of differential probe model
- ► Use de-embedding tool to create probe model



#### VNA System Error Correction (Calibration): Wafer Probes Example: MPI Wafer Probing Solutions

- Micro Positioners
- Unique puck controlled air bearing stage
- MPI Titan Probes



- Use of mmW Converters possible
- Calibration software "QAlibria"



#### Agenda

- Introduction and Basics:
  S-Parameter and Calibration
- Fixture Compensation Methods Overview
- Advanced Deembedding and Fixture Modelling



# **Offset Compensation**

► Offset compensation of fixtures:





Transmission line equivalent serial circuit

 "Auto length and loss" compensates magnitude and phase offsets









### **Offset Compensation**

- Standard feature of the R&S®VNAs
- Works best if a short length has to be compensated
- ► Should be used only up to some GHz
- Uses "open" and/or "short" measurements for compensation
- No correction of mismatches, it is not a type of calibration!



# **Time Domain Gating**

- Selection of relevant parts of the DUT in time domain
- Retransformation into frequency domain
- No insertion loss data
- ► No S-Parameter file creation possible





Advanced Deembedding

#### **TRL/ LRL / TRLLLM Calibration**

- ► Shift of reference plane to Thru/2
  - Cal data definition of thru: length = 0
- Limited frequency range
  - More lines needed to cover higher frequency range
  - Match needed to cover low frequencies
  - $\rightarrow$  High effort
- Different behavior of cal kit and fixture leads to errors



#### **Delta-L Measurements with R&S VNA**

- Introduced by Intel
- Motivation: Insertion loss characterization of (quasi-ideal) PCB transmission lines
- Delta-L 4.0 example: Eigenvalue Method





#### Agenda

- Introduction and Basics:
  S-Parameter and Calibration
- Fixture Compensation Methods Overview
- Advanced Deembedding and Fixture Modelling



#### **S-Parameter De-embedding**

- Use S-Parameter deembedding feature of R&S VNA to deembed fixture influence
- But: How to get S-Parameter file of your fixture?
- → R&S VNA Deembedding Options



Trc1 S11 Smith 200 mU/ Ref 1 U 1 V							
0.5 0.2 0.5 0.5 2							
Ch1 Center 500.0025 MHz Pwr -10 dBm Bw 10 kHz Span 999.995 MHz							
Trc3 S11 dB Mag 5 dB/ Ref 0 dB 2 ℃							
25			M1		M1 500	402500 MHz	-0.0245 dB
0 d0			Ÿ_				
-25							
Ch1	Center 500.0025 MHz	Pv	vr -10 dBm Bw	10 kHz		Span 9	99.995 MHz
-	Single Ended						
	Deembedding	Active	File Name 1		Swap Gates	Display File	Zero X-Mo
	P1 @ L1	✓ myfile.s2					
	P2 🔍 L2						
q							
mbe	•	_	<u> </u>		_	_	
Offset E	- Overview						🗙 Close

#### **IEEE 370 Standard**

- "Electrical Characterization of Printed Circuit Board and Related Interconnects at Frequencies up to 50 GHz"
- ► 3 major topics:
  - Test-fixture Design Criteria
  - De-embedding Verification
  - S-Parameter Integrity and Validation
- R&S tools fulfill requirements of IEEE STD 370
  - Ataitec In Situ De-embedding
  - CSS / Packet Micro Smart Fixture De-embedding

Advanced Deembedding

- Arcane - Eazy De-embedding



STANDARDS ASSOCIATION

IEEE Standard for Electrical

Frequencies up to 50 GHz

**Characterization of Printed Circuit** 

Board and Related Interconnects at

# **New R&S De-embedding Tools**



- Available for R&S ZNA, R&S ZNB / ZNBT and R&S ZND
- Deembedding workflow implementation
  - ZN-K210 EZD (Arcane)
    → based on IEEE 370 open source code
  - ZN-K220 ISD (Ataitec)
    → meets IEEE 370 requirements
  - ZN-K230 SFD (CSS/PacketMicro)
    → meets IEEE 370 requirements
- Delta-L workflow implementation
  - ZN-K231 Delta-L+ (CSS/PacketMicro)
    → Intel technology

# **De-embedding of Lead-in / Lead-out Traces**





Lead-out traces

#### ► Problem:

Differences between coupon and test fixture would lead to errors (different connector and line impedances (e.g. fiber weave), different signal routing, etc.)

- ► Solution:
  - "Impedance Correction" feature creates fixture \*.snp files out of Fixture + DUT measurements
  - Algorithm only determines length of fixtures from coupon measurement

# Partner De-embedding Tools VNA Firmware Integration

🚸 ISD - Balanced Ports



DUT has no standard adapters where calibration is possible



Measure test fixture "coupon": 2xThru or 1xOpen/ 1xShort

Measure DUT + test fixtures



VNA shows result for DUT only (by implementing fixture \*.snp files in de-embedding menu)





#### Use Case #1: PCB Test with De-embedding

- ► Step 1: Coaxial calibration
- ► Step 2: De-embedding of lead-in and lead-out
- ► All measurements at new reference plane





#### Use Case #2: Connector Test Fixture Compensation

- ► Step 1: Coaxial calibration
- ► Step 2: De-embedding of lead-in and lead-out
- ► Reference plane at connector under test





#### Use Case #3: Cable Test Fixture Compensation

- ► Step 1: Coaxial calibration
- ► Step 2: De-embedding of lead-in and lead-out
- ► Reference plane at cable under test





#### Use Case #4: SoC Test (System on Chip) Fixture Compensation

- ► Step 1: Coaxial calibration
- ► Step 2: Characterization of lead-in with VNA and extrapolation to DC
- ► Step 3: Import to Oscilloscope



#### Use Case #5: RF Devices without Coaxial Connectors

- ► Step 1: Coaxial calibration
- ► Step 2: De-embedding of lead-in and lead-out
- ► Reference plane at device under test





#### De-embedding with Impedance Correction: Example R&S ZNB with ZNB-K220 / ISD

- Automotive Ethernet 1000BASE-T1 STP
- ► Task: measure "inline connector" return loss
- Problem:
  - time domain gating will show reflection due to cable mismatch
- ► Solution:
  - use ZNB with K220 / ISD and impedance correction to get S-Parameter for Deembedding

DUT + Fixtures:



2 x thru "coupon" to get de-embedding files:



#### **R&S ZNB with Integrated De-embedding Workflow Example: ZNB-K220 / ISD**

► Inline Connector Return Loss result with ISD deembedding



Connector under test



#### **R&S ZNB with Integrated De-embedding Workflow Example: ZNB-K220 / ISD**

► Inline Connector Insertion Loss result with ISD deembedding







#### **R&S ZNB with Integrated De-embedding Workflow Example: ZNB-K220 / ISD**

- TDR Impedance of Fixtures and DUT
- S-Parameter view in postprocessing



#### **R&S De-embedding Tools**

For R&S Network Analyzers ZNA / ZNB / ZNBT / ZND:

![](_page_33_Picture_2.jpeg)

![](_page_33_Picture_3.jpeg)

![](_page_33_Picture_4.jpeg)

![](_page_33_Picture_5.jpeg)

**R&S ZNBT** 

**R&S ZNA** 

Advanced Deembedding

Find out more

#### www.rohde-schwarz.com

# Thank you!

#### ROHDE&SCHWARZ

Make ideas real

![](_page_34_Picture_5.jpeg)