Smart Jammer / DRFM Testing
Test and Measurement Solutions for the next level

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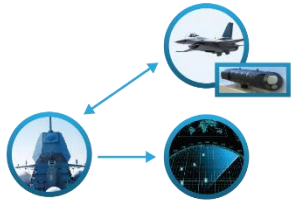
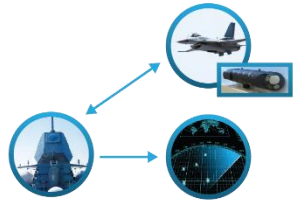
Market Segment Management Aerospace & Defense

Content



List of acronyms



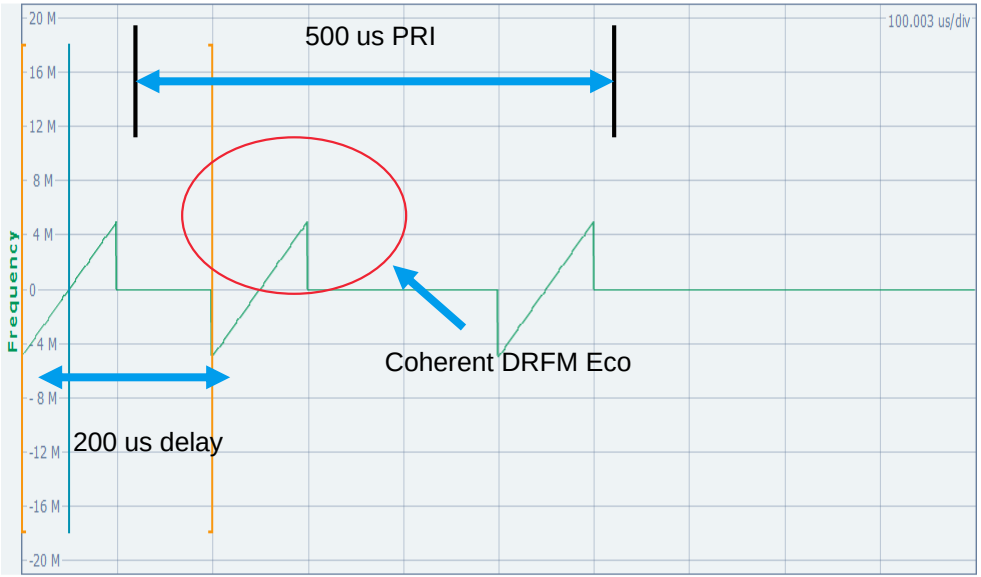
ADC – analog to digital converter
AESA – Active Electronically Scanned Array
AOA – angle of arrival
CPI – coherent processing interval
CVR – crystal video receiver
DAC – digital to analog converter
DF – direction finding
DIFM – digital instantaneous frequency measurement
DRFM – digital RF memory
DSP – digital signal processor
FPGA – field programmable gate array
ECM – Electronic Counter Measure
ECCM – electronic counter counter measures
EW – Electronic Warfare
IFM – instantaneous frequency measurement
RCS – radar cross section
RFFE – Radio Frequency Front End
RGPO – range gate pull off
VGPO – velocity gate pull off
SPG – signal processing gain
SWAP – size weight and power
ToT – time on target
TRM – transmit receive module

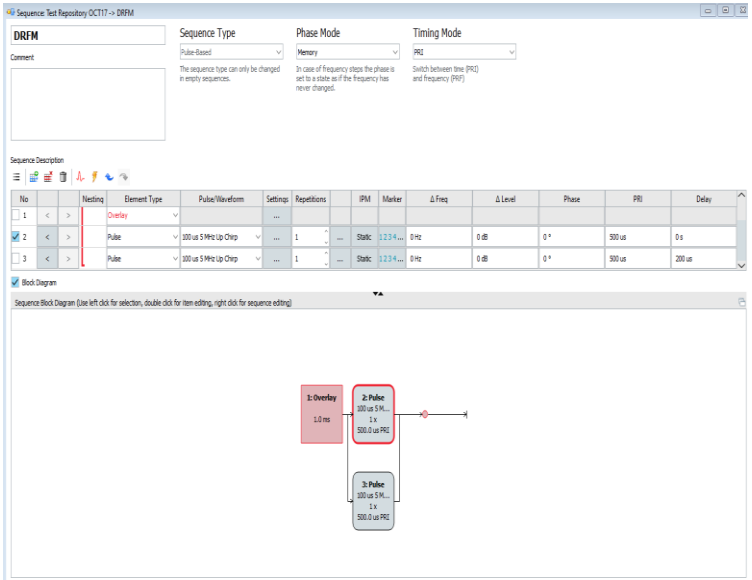
DRFM History

1975

- Earliest references to Digital RF Memory appear in an AOC article by Sheldon C. Spector, entitled "A Coherent Microwave Memory Using Digital Storage: The Loopless Memory Loop“.

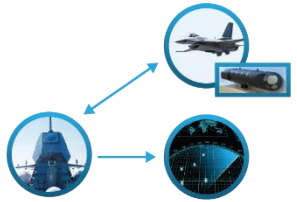
Principles of DRFM





DRFM History

1980



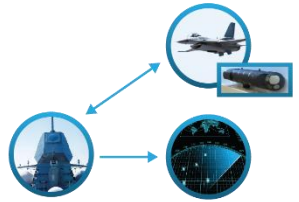
- DRFM is further developed as an ECM technique to pulse compression in Pulse Doppler Radar

- Development included: complex EW pods, towed decoys, later also disposable decoys

- Pulse Compression Technique - during WW2
    1. Improved range resolution and signal to noise ratio (SNR)
    2. Signal Processing Gain (SPG) – results in high processing gain
    3. Barrage jamming relatively ineffective - insufficient signal power due to SPG

DRFM History

Modern days



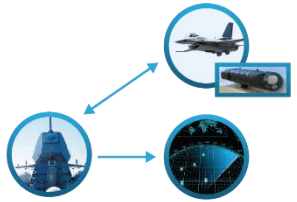
- DRFM Jammers are an essential part of the EW Electronic Attack suite
- Wideband technology and SWAP characteristics >2GHz
- Access to vast processing power via FPGAs and modern DSPs have allowed for a wide array of deceptive techniques – both coherent and non-coherent
- Freely Configurable integrated techniques generator
- Narrow and wideband coherent noise
- CW jamming
- Inverse gain techniques
- Deceptive techniques include:
  - Coherent range and velocity Pull-Off/In
  - False Doppler and range targets
  - Random false Doppler and range targets
- …

HENSOLDT
Detect and Protect.

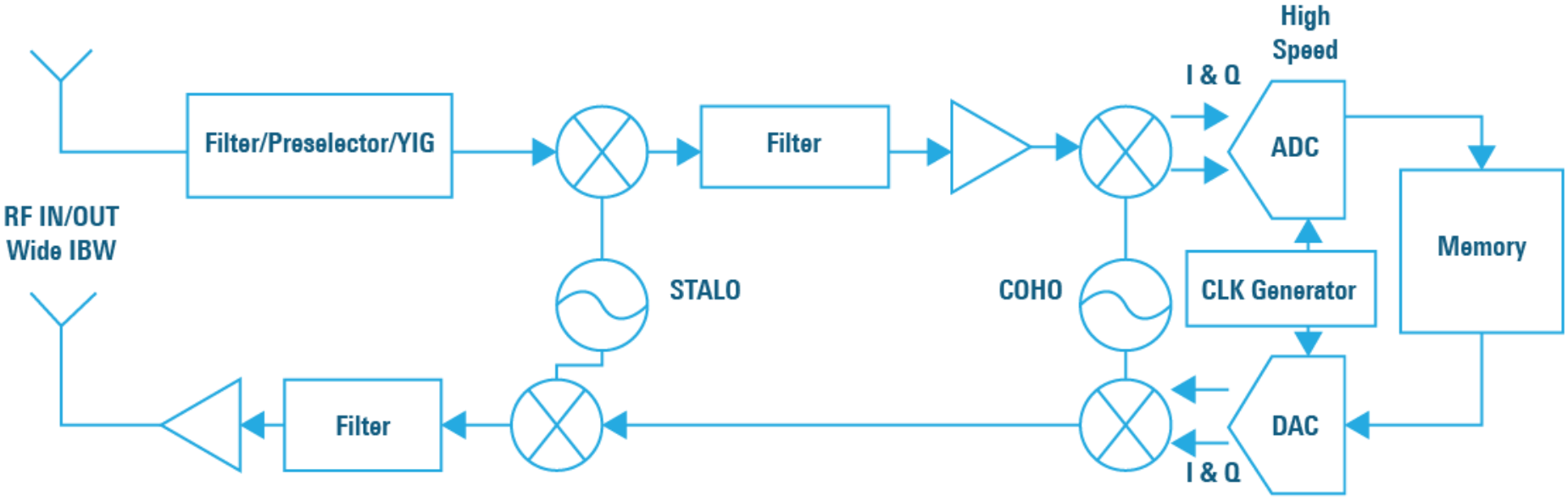
LEONARDO

DRFM Technology

Basic DRFM Block Diagram

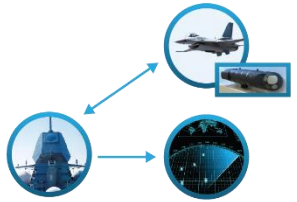


- Basic functionality: good approximation of an ideal point scatterer
- High fidelity return in Range, Doppler and RCS
- Coherent Transmit and Receive Paths

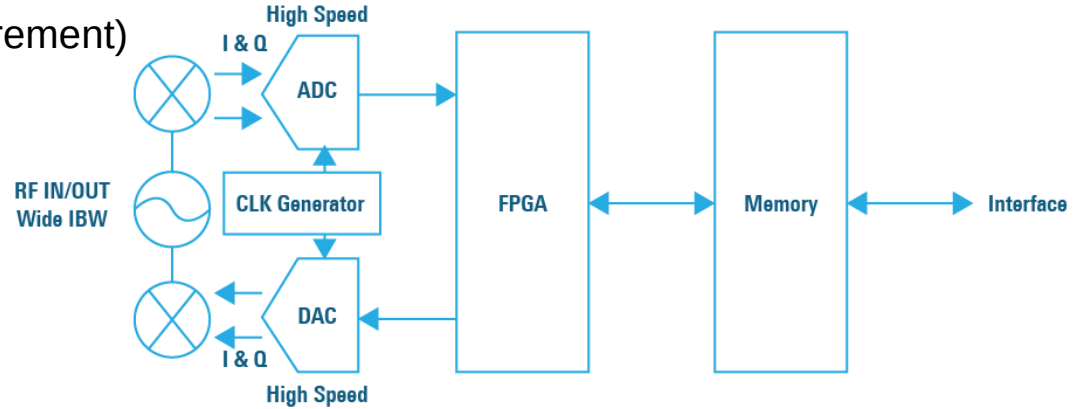


DRFM Technology

Modern DRFM Jammers

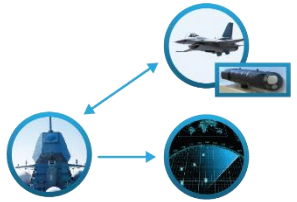


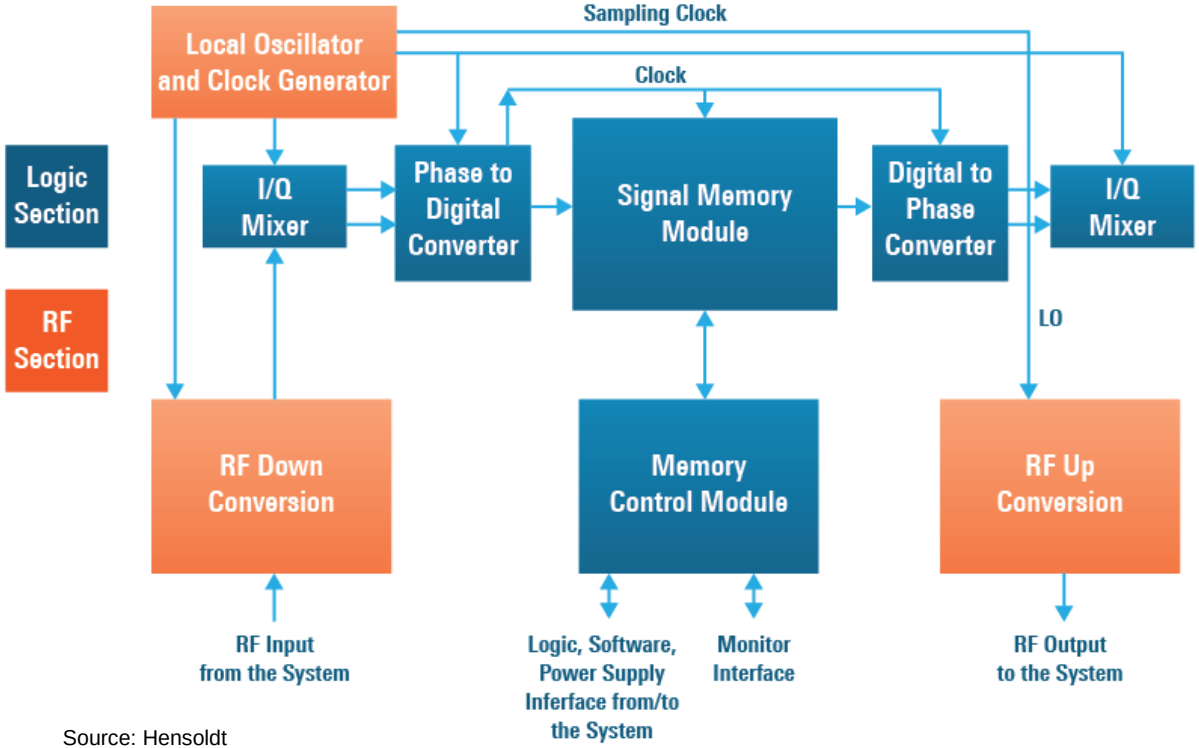
- Modern DRFM Jammers make extensive use of
  - FPGAs
  - High Speed ADCs and DACs for wideband operation
  - Wideband RFFEs
  - DIFM (digital instantaneous frequency measurement)
  - Phase correction
- Receiver Architectures
  - IFM (instantaneous frequency measurement)
  - CVR (crystal video receiver)
  - Digital Channelized Rx
  - …



DRFM Technology

Modern DRFM Jammers – example Hensoldt





Standard ECM Functions

- Coherent range and velocity Pull-Off/In
- Velocity gate Pull-Off/In
- Fixed false Doppler and range targets
- Random false Doppler and range targets
- Phase modulation
- Multi-frequency false targets
- Narrow and wideband coherent noise
- Narrow and wideband non-coherent noise
- Swept spot noise
- Multi-frequency noise
- CW jamming
- Frequency offset jamming, coherent and non-coherent
- Inverse amplitude techniques (with amplitude quantisation)
- Target scintillation
- Due to the programmability, other „custom-made" ECM functions can be installed. A combination of ECM techniques is possible.

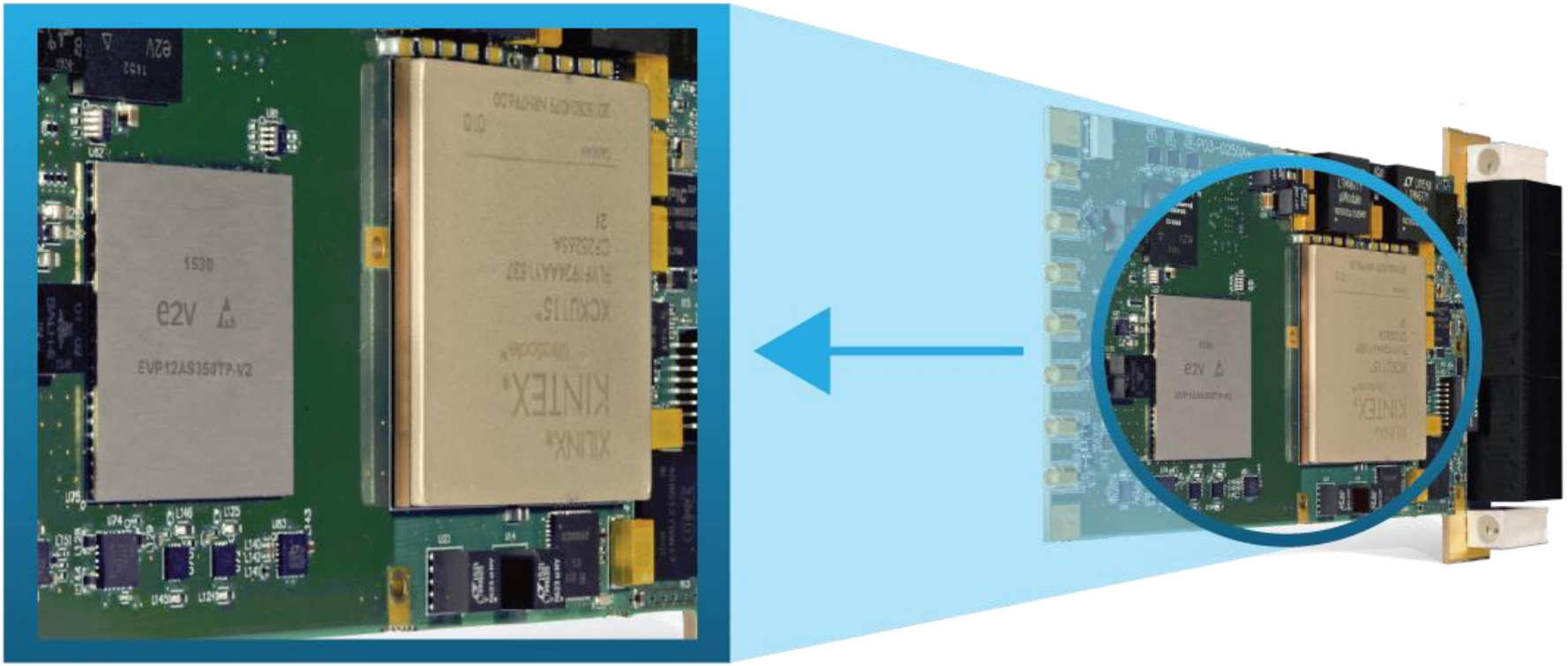
Characteristics and Performances

- Extremely wide band, single board DRFM
- Freely configurable integrated techniques generator
- Multi-threat capability
- Coherent and non-coherent ECM techniques
- Extremely fast digital signal detection
- Instantaneous bandwidth: up to 2,3 GHz
- Quantisation: up to 10 Bit amplitude
- Frequency accuracy: extremely accurate
- Volume: 3 litres
- Power consumption: 50 Watt

Source: Hensoldt

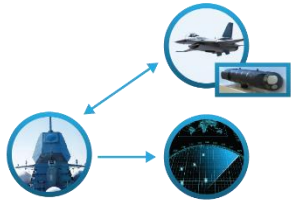
DRFM Technology

DRFM Module from Apissys: http://www.apissys.com/products/product/av125/23



DRFM Board Specifications

Source: http://www.apissys.com/products/product/av125/23#specification



Analog Input/Output

Coupling: AC
Input bandwidth > 5.5 GHz
Input Full scale : 8.5 dBm
Output bandwidth > 6 GHz
Output Full scale : -3.5 dBm (NRZ)
Impedance: 50 Ohm
Connectors: SMPM

Analog-Digital Conversion

One channel, Fs ≤ 5.4 GHz
Resolution: 12 bit
Sampling Performances @1 GHz, -1dBFS
- SNR: 55 dBFS
- SFDR: 60.5 dBc
- ENOB: 8.5 bits

Digital-Analog Conversion

One channel, Fs ≤ 5.4 GHz
Resolution: 12 bit
Sampling Performances @1 GHz, 0dBFS
- SFDR: 59 dBc, NRTZ mode

Sampling Performances @3 GHz, 0dBFS
- SFDR: 55 dBc, NRTZ mode

Clock

Internal:
- 1 GHz to 5.0 GHz low jitter clock

External Input Clock:
- Frequency: 2 GHz to 5.4 GHz
- Connector: SMPM, 50 Ohm and VPX P2

External reference:
- Frequency: 10 MHz to 800 MHz
- Connector: SMPM, 50 Ohm and VPX P2.

Trigger

External: 0 to 2 Vp
Connector: SMPM, 50 Ohm

FPGA

n
FPGA: Xilinx Kintex Ultrascale XCKU115-2FLVF1924

Memory

Two banks 256M64 DDR3 SDRAM, 800 MHz clock
Two 1 Gbit QSPI NOR FLASH memory

VPX interface

P1:
- Data plane: two fat pipes
- Expansion plane: one fat pipe
- Control plane: 2 ultra-thin pipes
- 2 user-defined ultra-thin pipes

P2:
- USB2.0 and 10/100 Ethernet
- 26 LVCMOS33 signals
- 4 SUB-LVDS differential pairs

Software support

Software Drivers:
- Windows 10
- Linux

Application example:
- Windows and Linux

Firmware support

VHDL cores for all hardware resources
Base design
Supported by Xilinx VIVADO 2016.2 and later

Ruggedization

As per VITA 47:
- Air cooled : EAC4 and EAC6
- Conduction cooled : ECC3 and ECC4

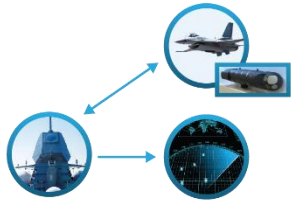
Power dissipation

+12V: 6.2 A max (75W)
+5V: 3.0 A max (15W)
+3.3V: 3.2 A max (10W)
+3.3VAUX: 0.6 A max (2.0W)

Weight

Air cooled : 550g
Conduction cooled : 650g

DRFM Test Requirements



R&S NRPxx

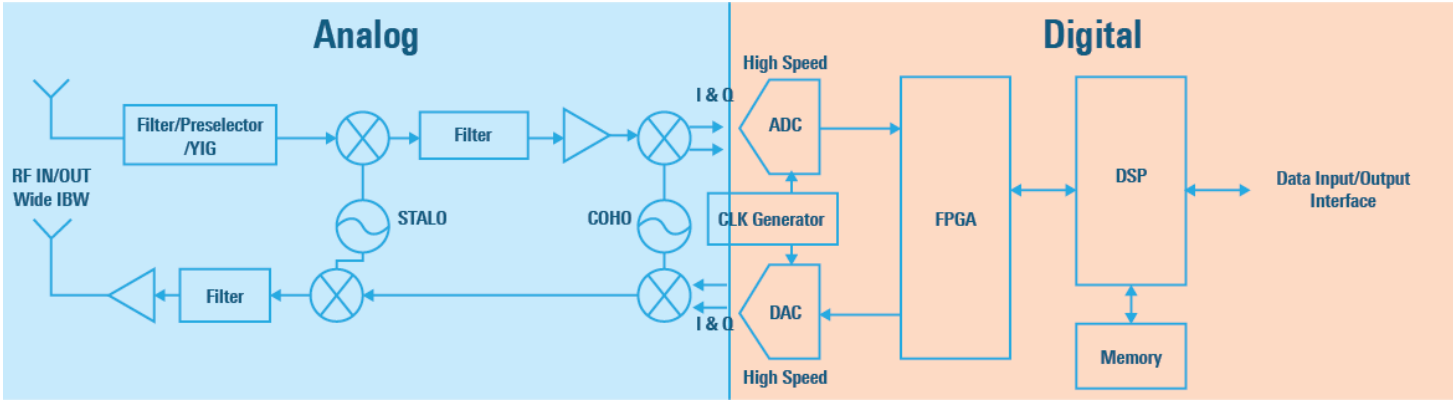
Test Systems
DF, Phase Coherent
Signals

R&S Pulse
Sequencer

R&S FSW

R&S FSWP

R&S ZVA / ZNB / ZNT



R&S SMA100B

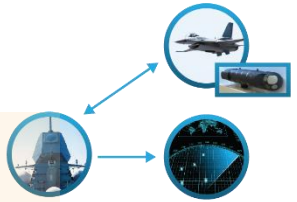
R&S CMA180

R&S SMW

R&S SGx

R&S RTP

DRFM Test – excerpt of some key requirements

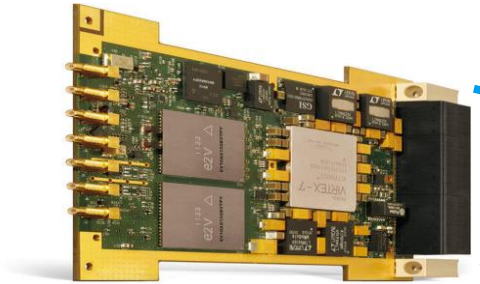


- **System Level**
  - DF
  - Deception Techniques
  - Phase / Pulse Stability
  - Latency
  - EVM
  - Spectral Purity
  - GNSS Tests
  - MILEMC
- **RF/IF Stage**
  - Spurious measurements
  - Dynamic Range
  - Compression point
  - Gain/Phase/Frequency Response
  - Noise Figure
  - Input/Output Impedance
  - Image rejection
  - Receiver sensitivity
  - IP3
  - Quadrature error
  - LO Phase Noise
  - LO Leakage
  - LO Long Term Stability
  - Antenna radiation pattern
- **Digital Stage**
  - Power/Signal Integrity
  - LO/Clock Jitter
  - Latency
  - Timing
  - EQ Flatness
  - EMI debugging
  - FPGA Tests
  - DSP Tests
  - ADC/DAC Tests
    - SFDR
    - EnoB
    - Speed
    - Quantization Error

DRFM Test Requirements – System Level

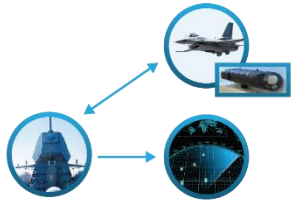
- **System Level**
  - DF
  - Deception Techniques
  - Phase Stability
  - Latency
  - EVM
  - Spectral Purity
  - MILEMC

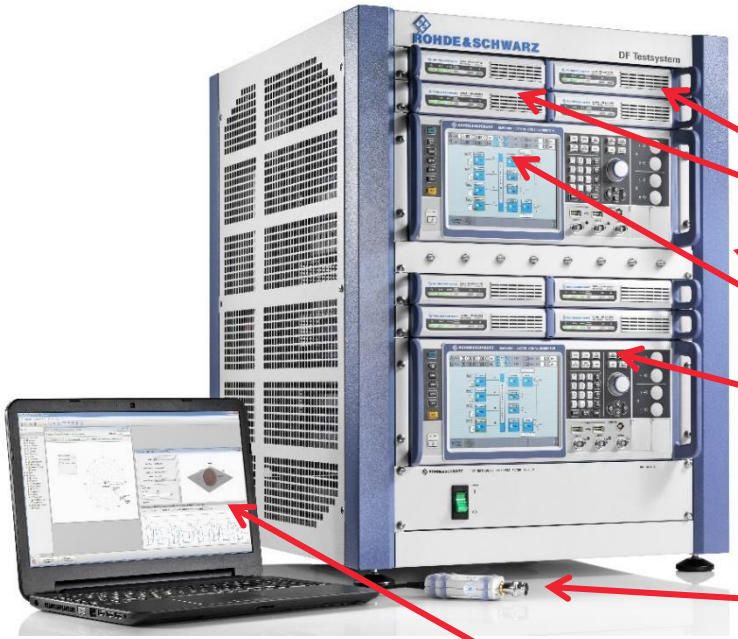
R&S Pulse Sequencer



DRFM Test Requirements

System Level Tests – Direction Finding





Angle-of-Arrival estimation or other applications require signals that are aligned in time and phase at the reference plane

R&S®SGS100A and R&S®SGU100A for additional RF channels

8 independent RF outputs up to 20 GHz with 160 MHz bandwidth

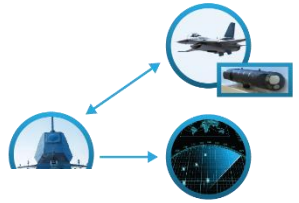
R&S®SMW200A with 4 separate, independent basebands
Option SMW-B90 Phase Coherence required

R&S®NRP-Z81 power sensor

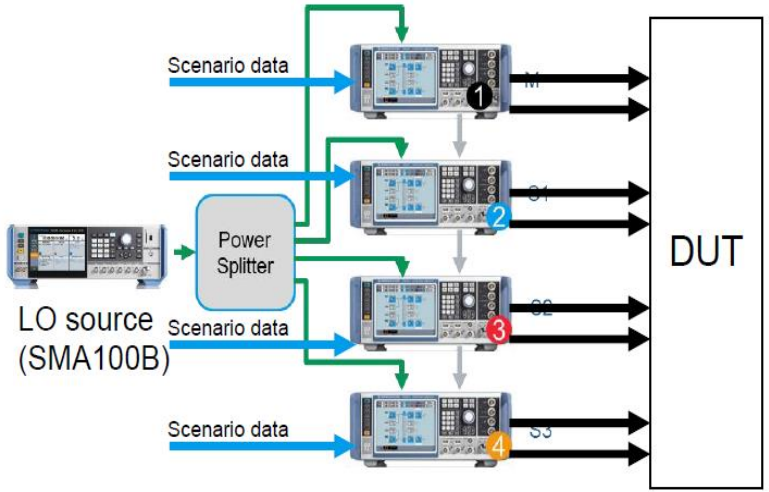
R&S®Pulse Sequencer software for scenario definition and full remote control of system

DRFM Test Requirements

System Level Tests – AOA Simulation



- Radar scenario (blue arrows)
  - R&S Pulse Sequencer Software provides radar scenario or
  - Radar scenario is streamed to SMW200A from customer simulator
- Key hardware requirements for best simulation performance
  - Highly repeatable and stable amplitude, phase and timing differences between RF ports
- Proposed hardware setup
  - Common local oscillator (LO) signal from SMA100B high end analog signal generator (green arrows) to all SMW200A
  - SMWs' baseband generators are synchronized (grey arrows)



4 x SMW200A with improved coupling provide 8 phase coherent RF output signals

DRFM Test Requirements

System Level Tests – Deception Techniques Analysis

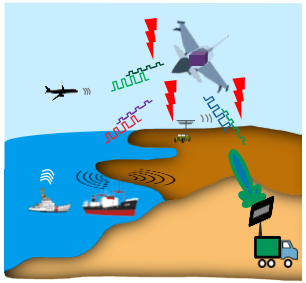
- Simulation of the dense emitter environment (up to 256 emitters in a 4GHz BW; interleaving / de-interleaving)
- Generation of realistic radar signals incl radar mode switching
- Analysis of the deception technique
- Comparison to original radar signal
- Streaming of up to 6 million PDWs per second with PDW interleaving

PDW Streaming

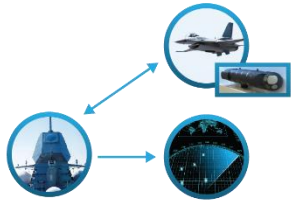
+

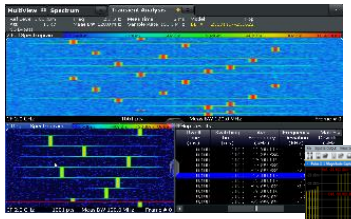
R&S SMW

=



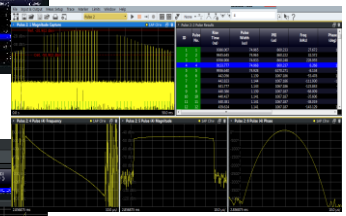
R&S FSW

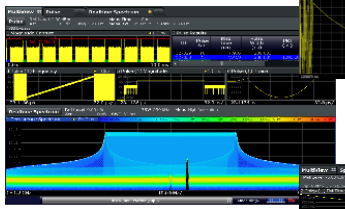




R&S FSW-K60H

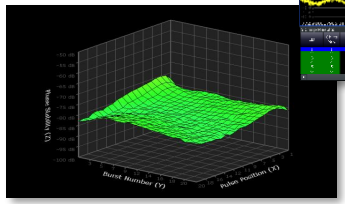
R&S FSW-K6





R&S FSW-B512R

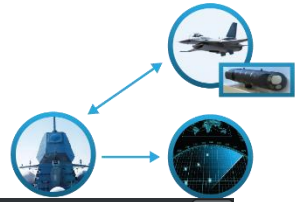
R&S FSW-K60C



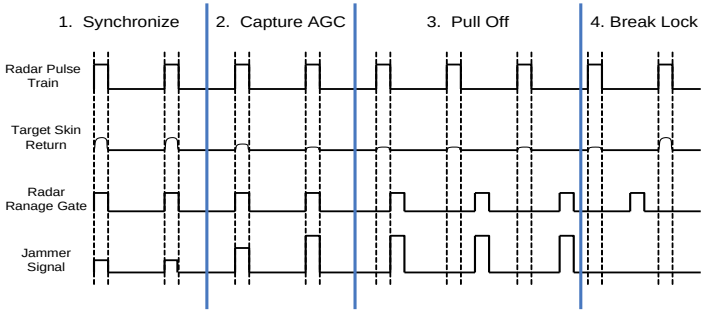
R&S FSWP-K6P

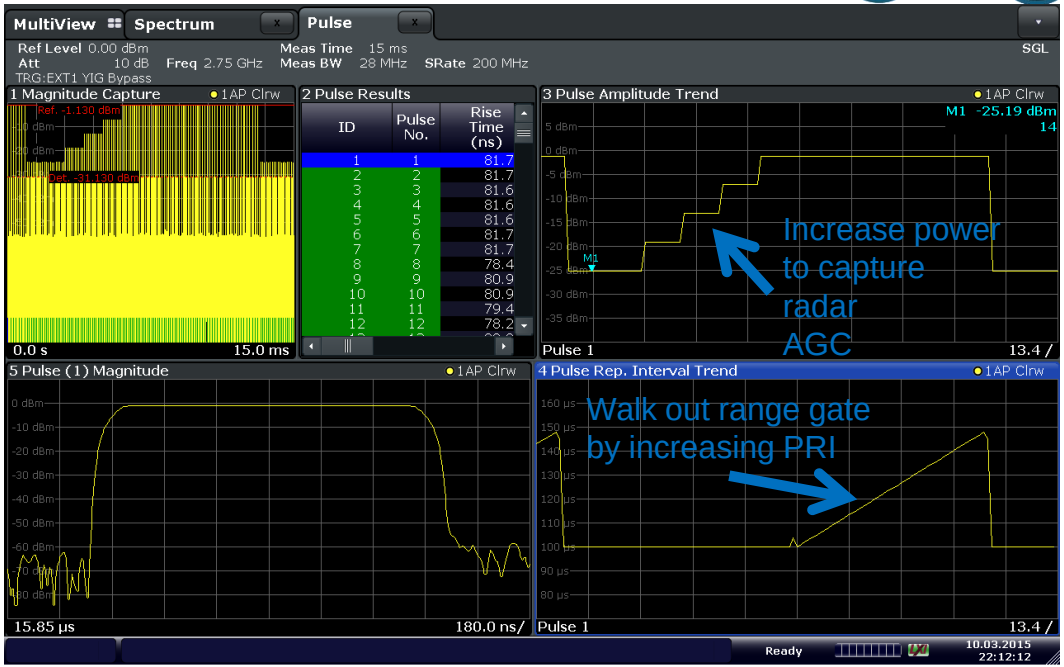
DRFM Test Requirements

System Level Tests – Deception Techniques Analysis – Example RGPO



- Cover the target skin return—or synchronize
- Increase power to capture the radar's automatic gain control (AGC)
- Begin pulling or pushing the range gate in time
- Drop the jamming—forcing the radar to loose lock





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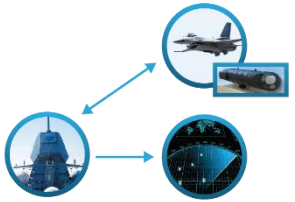
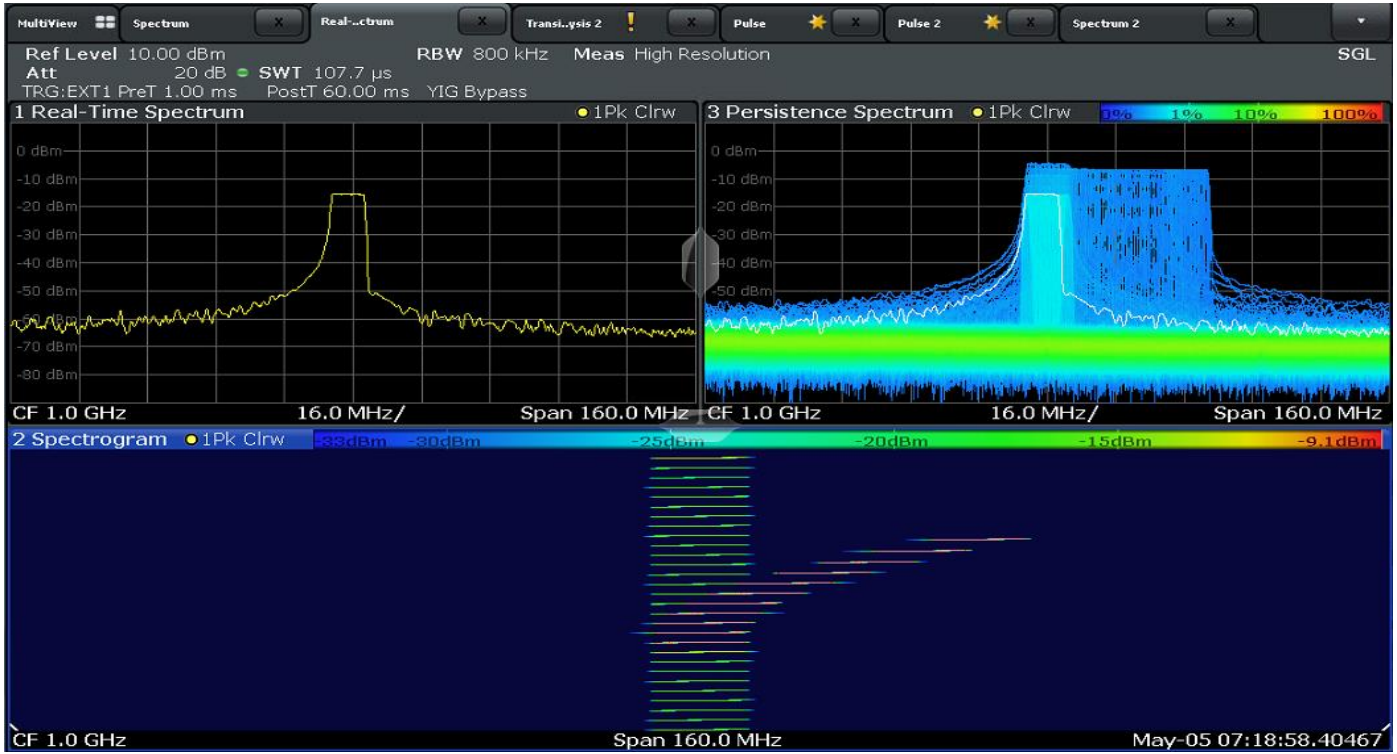
DRFM Test Requirements

System Level Tests – Deception Techniques Analysis – EW Measurement Science

DRFM Test Requirements

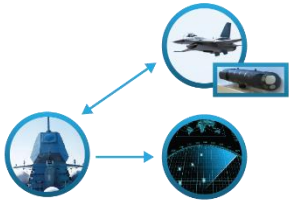
System Level Tests – Deception Techniques Analysis – VGPO Real Time





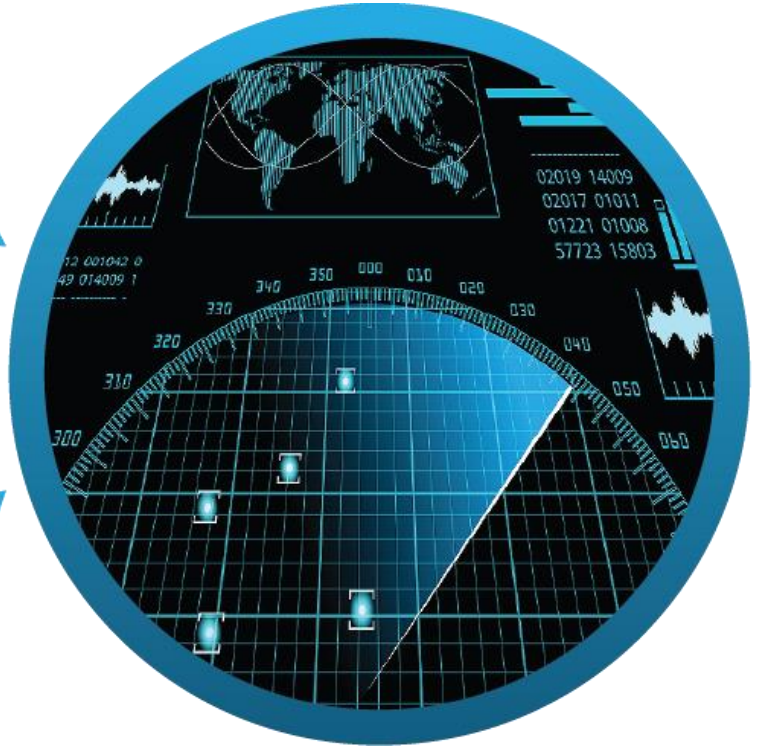
DRFM Test Requirements

System Level Tests – Deception Techniques Analysis / Distortion Measurements – FSWK6s



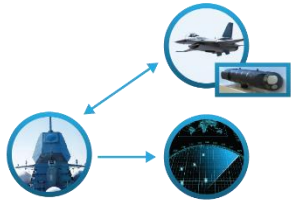
Original radar signal

Spoofed radar signal



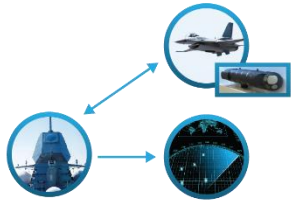
DRFM Test Requirements – RF/IF Stage

- **RF/IF Stage**
  - Spurious measurements
  - Dynamic Range
  - Compression point
  - Gain/Phase/Frequency Response
  - Noise Figure
  - Input/Output Impedance
  - Image rejection
  - Receiver sensitivity
  - IP3
  - Quadrature error
  - LO Phase Noise / Leakage / Long Term Stability
  - Antenna radiation pattern



DRFM Test Requirements

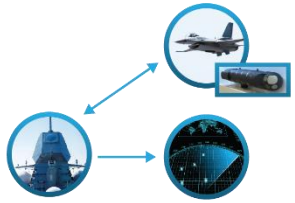
RF/IF Stage – Spurious Measurements – Faster & Easier with FSW-K50



- **Fast** - Up to 20 times faster than existing spectrum analyzer spurious searches, specially at low RBWs
- **Easy** - RBW is automatically calculated based on maximum allowed spur level

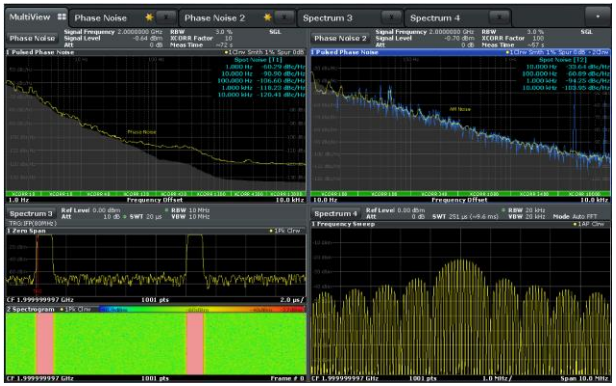
DRFM Test Requirements

RF/IF Stage – Phase Noise / VCO Characterization - FSWP



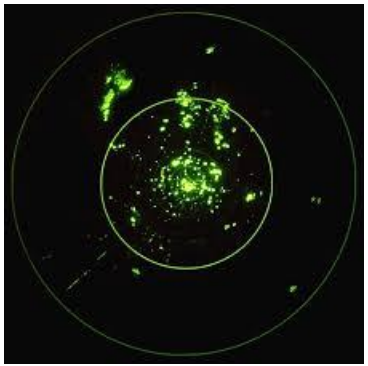
Benefits

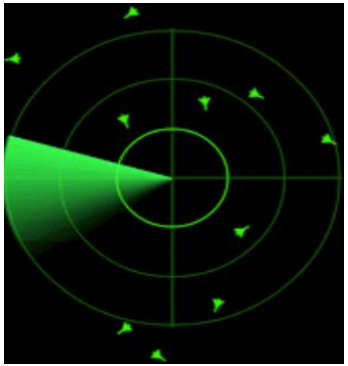
- Fast – from hours to minutes
- Easy – at the push of a button, no additional components
- Accurate – highest performance on the market

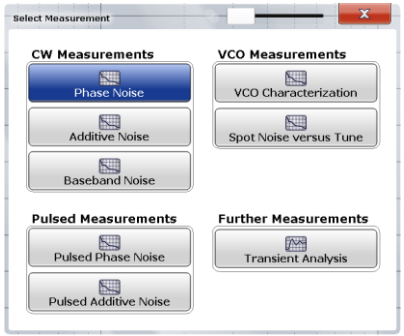


Highlights

- Phase noise, VCO tester and a signal and spectrum analyzer in one box
- Measurement of phase noise on pulsed sources
- Simultaneous measurement of amplitude noise and phase noise
- Internal source for measuring additive phase noise
- Low-noise internal DC sources for VCO characterization

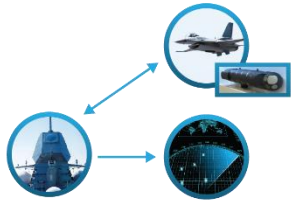






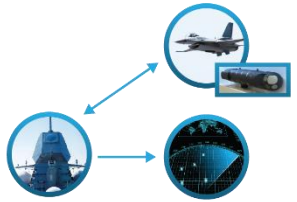
DRFM Test Requirements

RF/IF Stage - VCO Tests – All parameters in one view - FSWP



DRFM Test Requirements

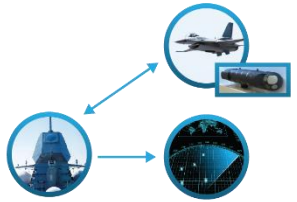
RF/IF Stage – LO Stability – Allen Variance



- David W. Allan (born September 25, 1936, Mapleton, Utah) is an American physicist and author of the Allan variance
- The Allan variance is a two-sample variance used to analyze the time-domain frequency stability of oscillators
- The classical variance is non-convergent for common sources of noise such as: random walk and flicker
- Whereas, the Allan Variance converges for all common noise types and allows inference to the type and level of the noise

DRFM Test Requirements

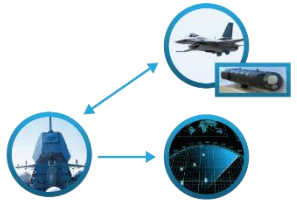
RF/IF StageTests – Pulse Stability



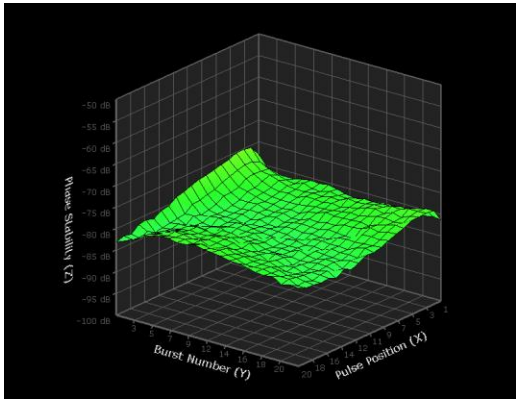
- Many possible factors including mechanical, thermal and electrical effects can affect stability
  - Phase noise in components like oscillator, mixer, multiplier and filter
  - Electromagnetic perturbations (e.g. causing parasitic coupling between or inside modules)
  - Thermal variation in power devices
  - Fluctuation in switching power supply (leading to ripple and slow variation of bias)
  - AM-PM conversion in a saturated amplifier
  - Mismatch between different stages of the transmitter module
  - Memory effects (thermal and trapping effects)

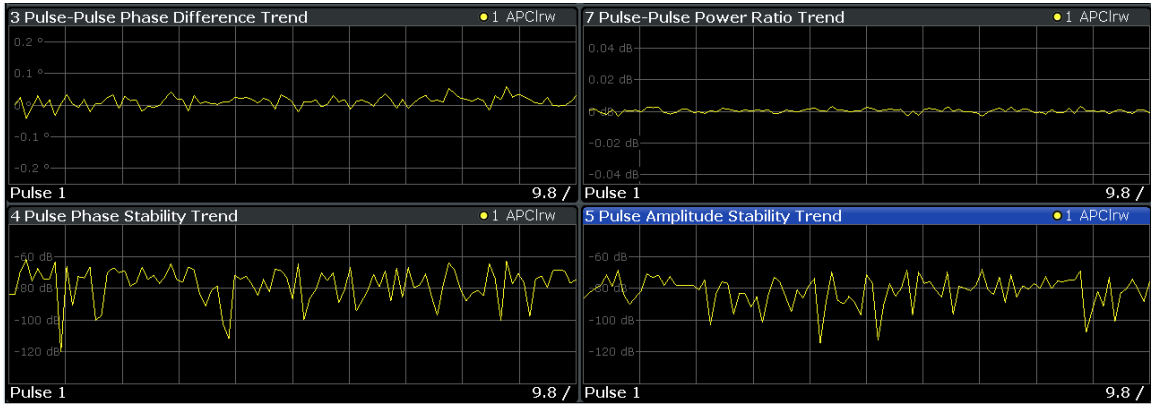
DRFM Test Requirements

RF/IF Stage – Pulse Stability – Phase / Amplitude – FSWP-K6p



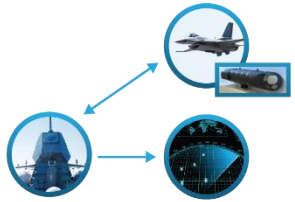
- Phase stability
  - Difference to average phase
  - Correction of frequency offset (linear phase change)
- Amplitude stability
  - Difference to average amplitude





DRFM Test Requirements

RF/IF Stage – RF Components

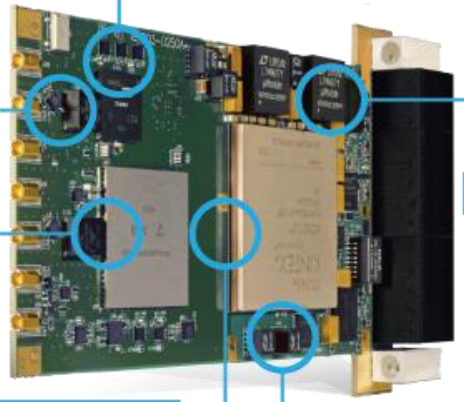


Phase Noise Testers, Spectrum Analyzers e.g. FSWP, FSW

Network Analyzers

Clock Verification

RF Components



Signal Generators e.g. SMA100B

Power Integrity

Data Converter Design

Oscilloscopes e.g. RTO, RTE

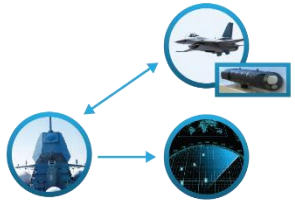
Protocol-Level Debug

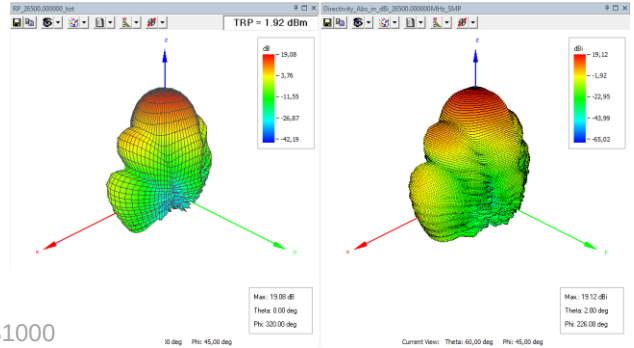
SerDes PLL Verification

Power Supplies e.g. HMP

DRFM Test Requirements

RF/IF Stage - Antenna Tests





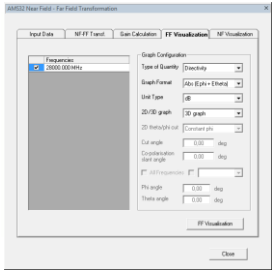
ATS1000: Passive Antenna Measurement and Nearfield - Farfield Transformation
Application Note

Test Systems
Interference,
TRM,
Phase Coherent
Signals

R&S ATS1000

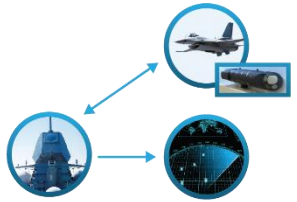
R&S DST200

R&S AMS32

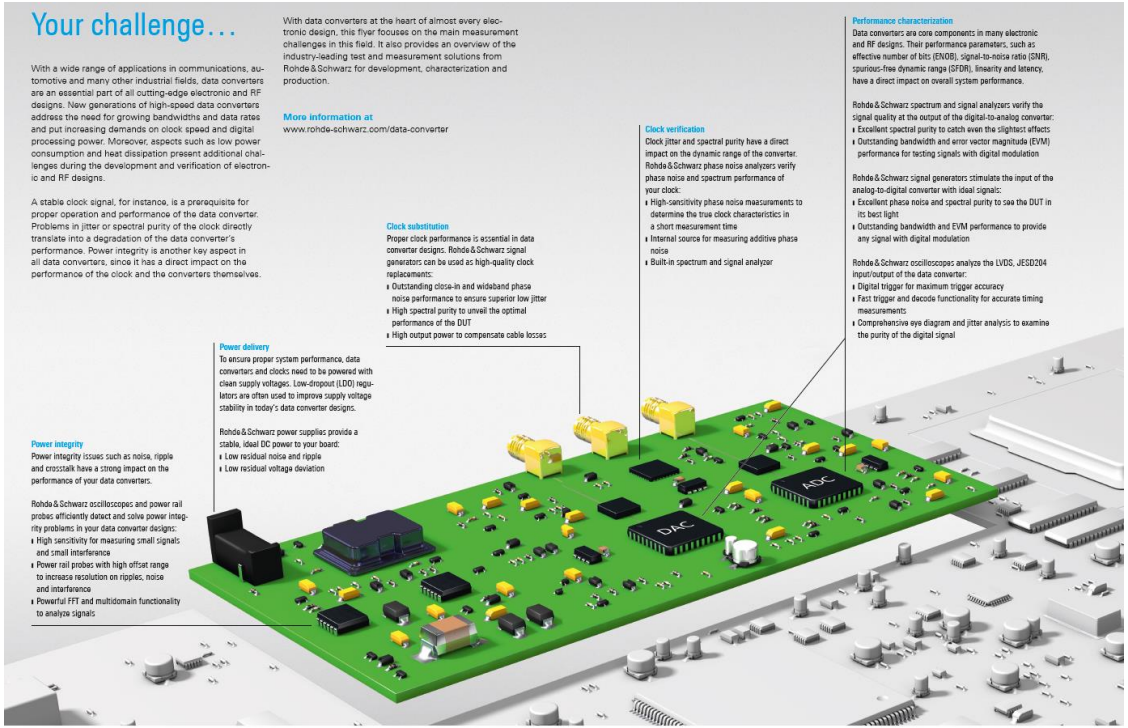


R&S ZNAxx

DRFM Test Requirements – Digital Stage

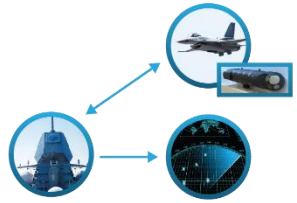


- **Digital Stage**
  - Power/Signal Integrity
  - LO/Clock Jitter
  - Latency
  - Timing
  - EQ Flatness
  - EMI debugging
  - FPGA Tests
  - DSP Tests
  - ADC/DAC Tests
    - SFDR
    - EnoB
    - Speed
    - Quantization Error



DRFM Test Requirements

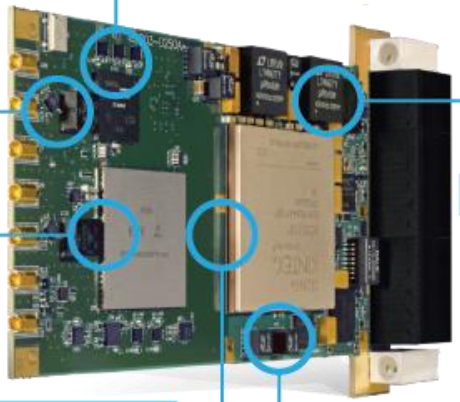
Digital Stage - Overview



Phase Noise Testers, Spectrum Analyzers e.g. FSWP, FSW

Network Analyzers

Clock Verification



Passive Components

Data Converter Design

Power Integrity

Signal Generators e.g. SMA100B

Oscilloscopes e.g. RTO, RTE

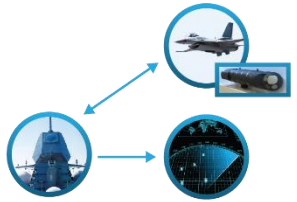
Protocol-Level Debug

SerDes PLL Verification

Power Supplies e.g. HMP

DRFM Test Requirements

Digital Stage – Power Integrity

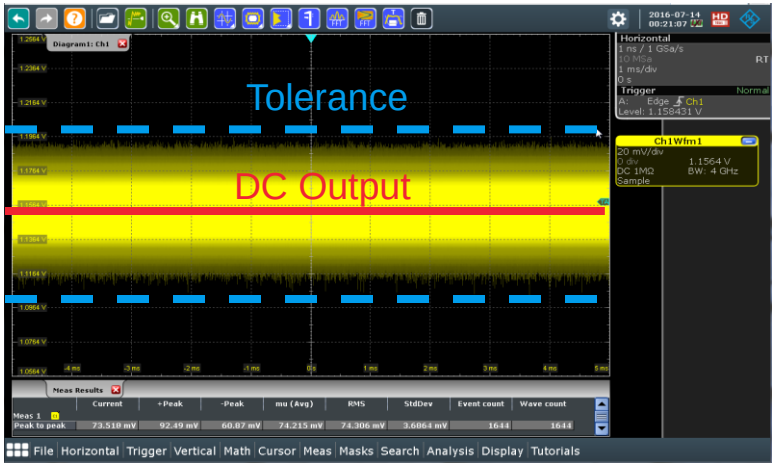


Building Blocks

- power distribution network (PDN)
- low dropout regulators (LDO)

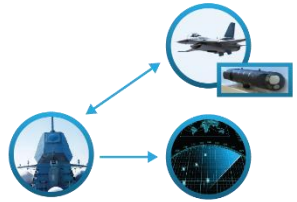
Typical Performance Parameters

- power integrity: ripple, noise, …
- PDN impedance:
  - resonances cause PI problems
  - resonances cause EMI / EMS problems
- LDO power supply rejection ratio (PSRR)



DRFM Test Requirements

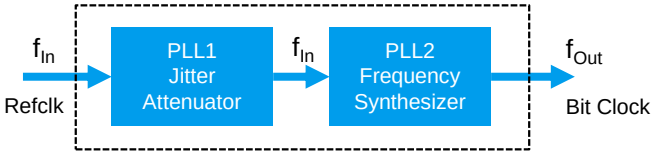
Digital Stage – Clock Jitter



Building Blocks

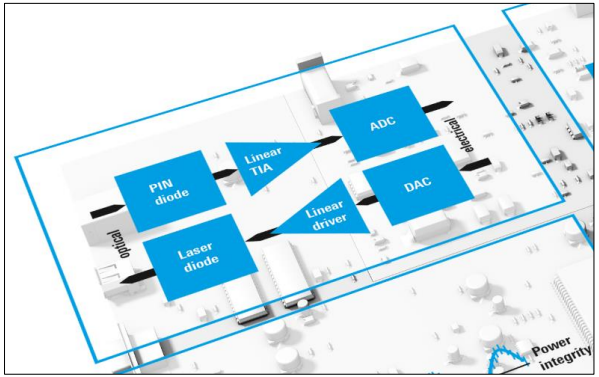
- ADC / DAC clock synthesizers
- SerDes PLLs

➔ often two-stage architecture:



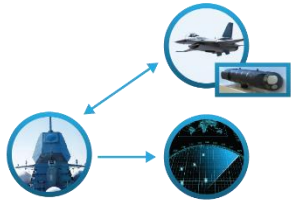
Typical Performance Parameters

- absolute phase noise / jitter
- additive phase noise / jitter
- jitter attenuation (Jitter Transfer Function JTF)
- system margin testing
- power supply noise rejection (PSNR)

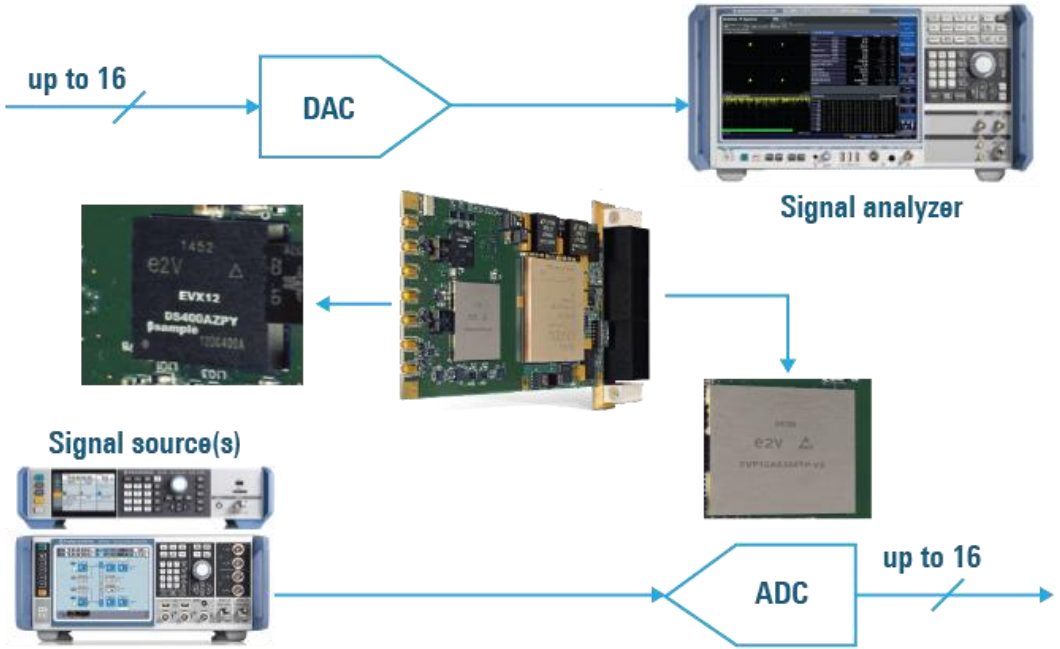


DRFM Test Requirements

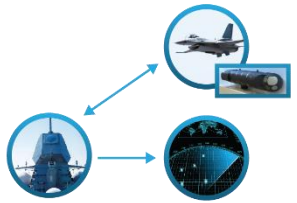
Digital Stage – ADC/DAC Measurements



- DAC
  - Testing of output signal quality like SFDR
  - Phase noise testing
  - Measurement of modulation quality for digital output signal like EVM, ACLR, …
  - Test signals generated in test mode by DAC or from an external baseband source
- ADC
  - Testing of RF input circuitry
  - Generic testing with single and dual tone CW signals (intermodulation)
  - Test with real signal as used in later application



DRFM Jammer Test
Our Best Solutions in Service of Our Customers



Smart Jammer / DRFM Testing
Test and Measurement Solutions for the next level

Yassen Mikhailov
Market Segment Management Aerospace & Defense