Webinar series: 5G Device Testing Journey

VALIDATION OF DIGITAL DESIGN OF NEXT GEN DEVICES

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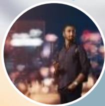
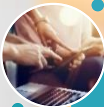
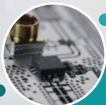
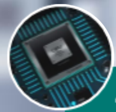
Make ideas real









Date	Topic
15th June	Production test strategies and smart solutions
8th June	Making 5G lab testing more realistic with R&S®CM360º
1st June	ONE tool for automated device testing
25th May	Simplifying 5G mobile device testing
11th May	Challenges to 5G mmWave component characterization
4th May	Validation of digital design of next gen devices

5G DEVICE TESTING JOURNEY

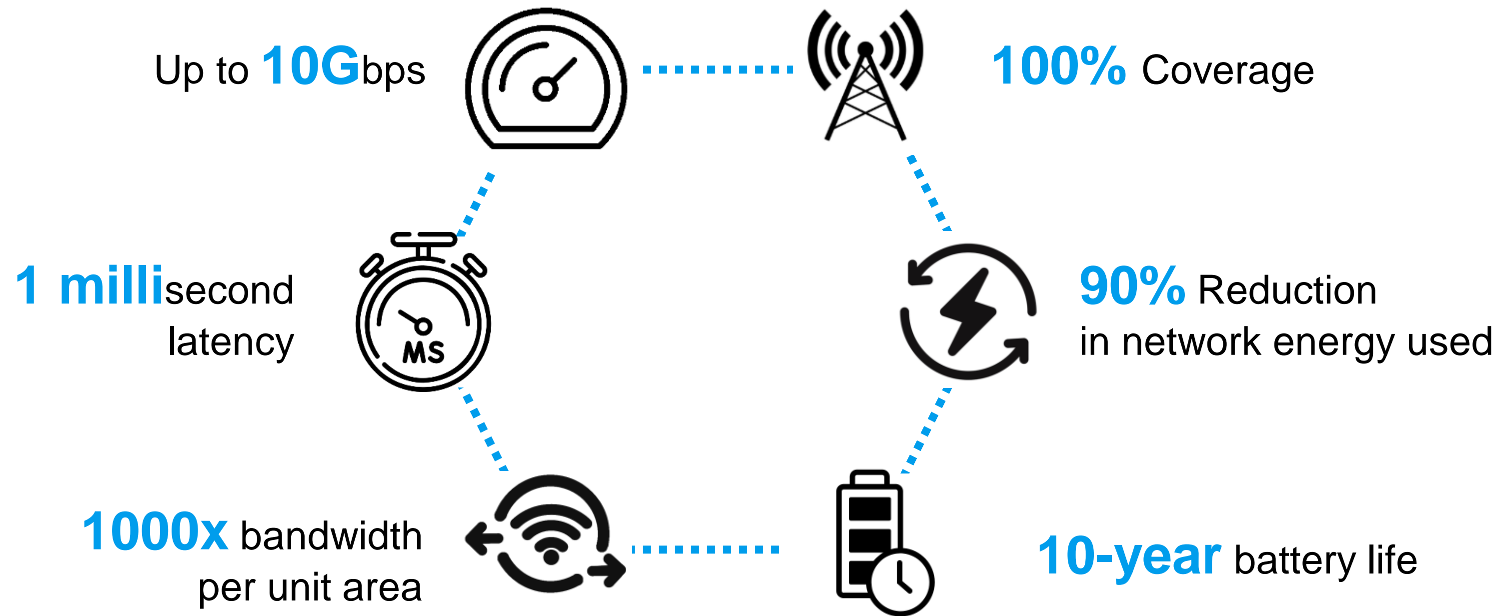
Webinar Series

TOPICS

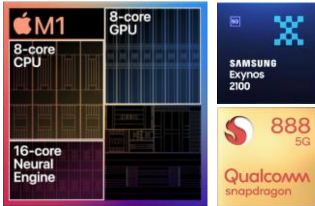
- ► What is in next gen?
- ► Base Station / Cellular Device Architecture
- ► High Speed Digital Interfaces
- ► Power Integrity
- ► Summary

Validation of digital design of next gen devices

KEY DRIVERS BEHIND THE NEXT GEN NETWORK & DEVICES



DIGITAL LEAP IN NEXT GEN DEVICES



Warp-Speed processing

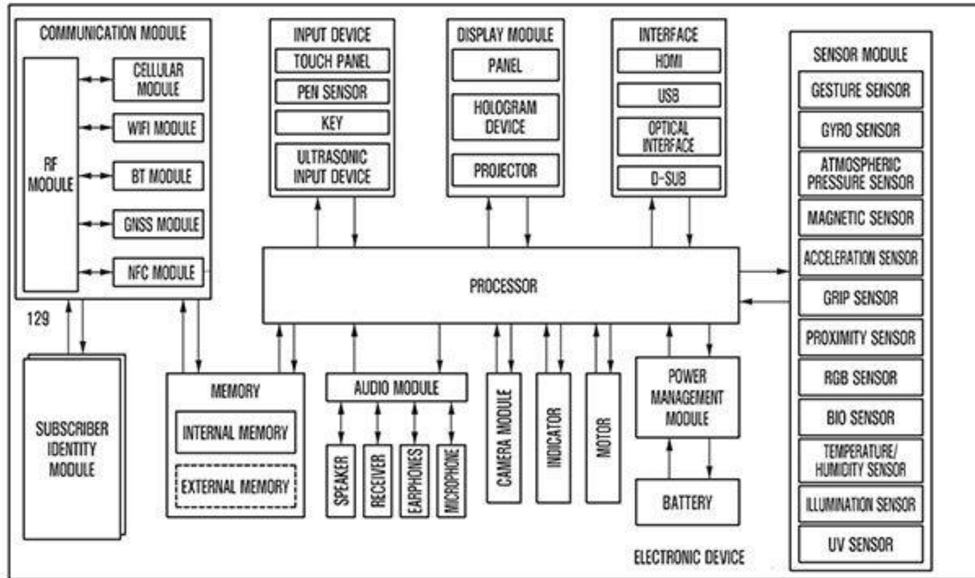
Camera Resolution

Connectivity

Battery Life

Crystal Clear Display Refresh Rate

DEVICES ARE COMPLEX SYSTEM



NEXT GEN DEVICES TRENDS

Digital Design & Power Trends

- Memory: LPDDR4 –> LPDDR4x -> LPDDR5 starts
- Digital Processor: 7nm -> 5nm -> 3nm planned for 21/22
- Display interface: higher resolution
- Camera interface: higher resolution
- Additional sensors / health features
- Data / charging: USB -> USB Type C -> Wireless / Wireless Charging (Qi)
- Power management: plenty of PMICs
- Battery technologies: longer battery time
- Integration: Multi-chip, System-on-a-chip, etc.

RF Trends

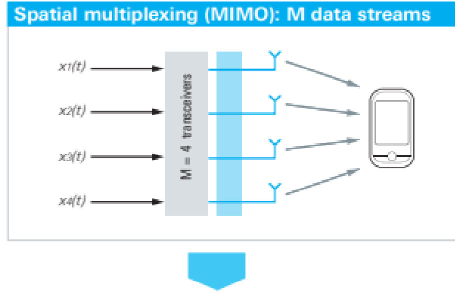
- More Radios for new cellular and non-cellular standards
- MIMO antennas

INCREASING MIMO DEGREES & BEAMFORMING

Increase data rates and energy efficiency:

- increase bandwidth (mmWave)
- **massive MIMO**
- **beamforming**
- virtualized network architecture

MIMO: Multiple antennas at the TxRx to increase capacity.



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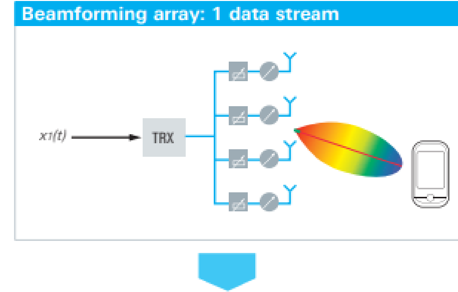
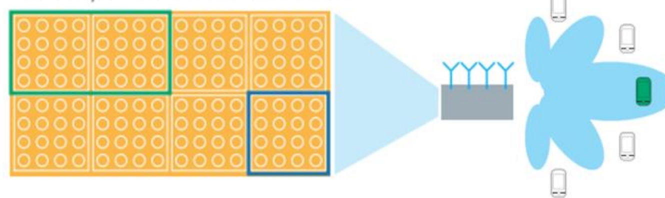


Beamforming: Increases antenna gain by bundling transmitted energy and directing it towards the user.

Massive MIMO: Very high number of antenna elements at the transceiver.
Combination of beamforming and spatial multiplexing.



Increasing demand for higher MIMO degree.
Operators with mid-band spectrum show greater confidence in Massive MIMO, e.g. China, US.
Beamforming as an essential measure to increase system efficiency, especially for mmWave.

BASE STATION / CELLULAR DEVICE ARCHITECTURE

Review of key components and how to address their testing.

5G BASE STATION ARCHITECTURE
Digital Design, Power and RF Components

Signal Integrity Analysis & Debugging of all Digital Interfaces

RF Signal Analysis

Memory DDR
RefClk
PCIe
Control I/Os (SPI, I2C, ..)
Embedded Processor (e.g. ASIC, CPU)
L2 processing
L1 processing
Baseband Processor (e.g. FPGA, ASIC)
Coding
Modulation
Digital Beamforming
CFR
DPD
BB Unit

Ethernet
PCIe

(e)CPRI

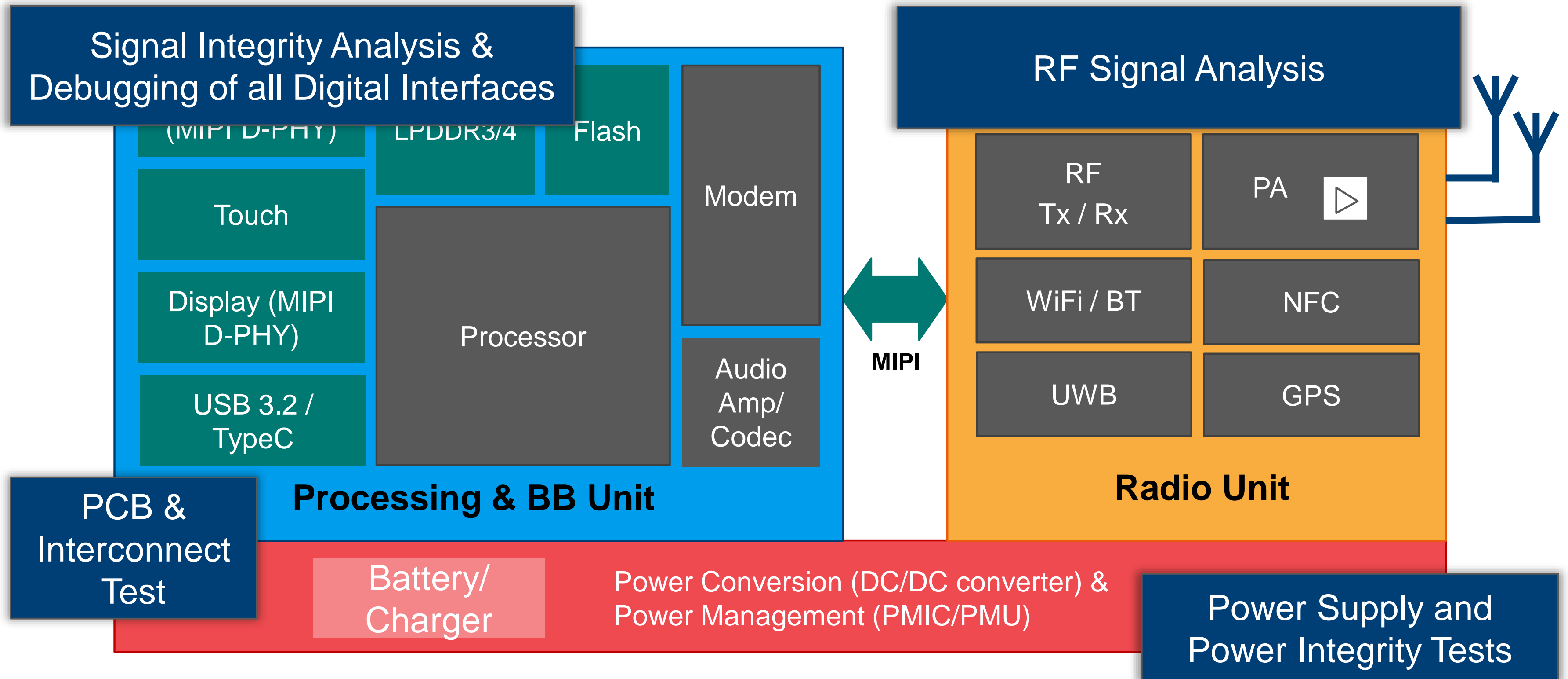
Transceiver
ADC
DAC
Down-converter
Up-converter
RF Conditioning / Amplification
Radio Unit

PCB & Interconnect Test

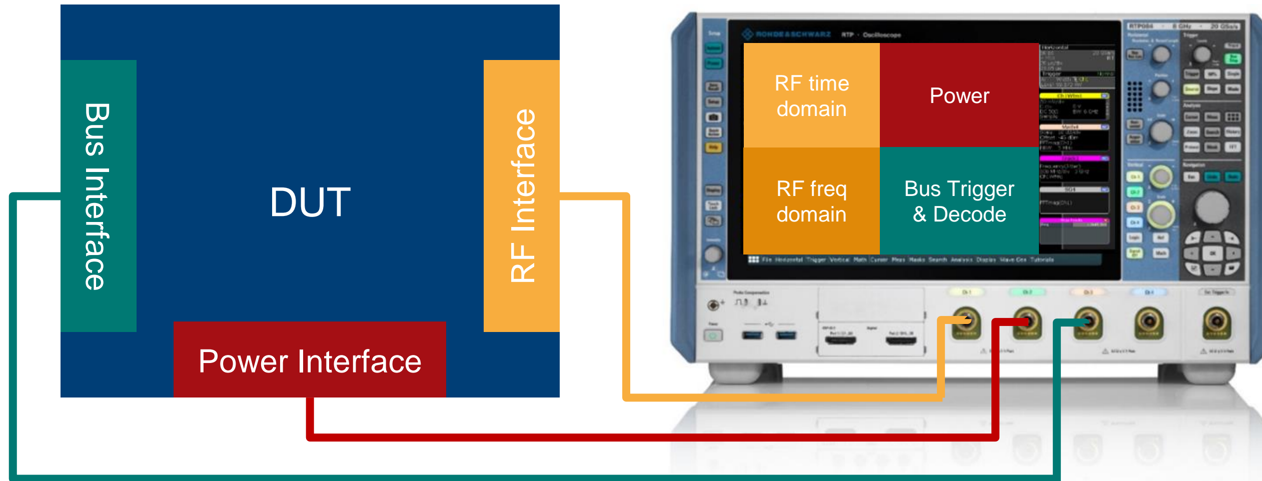
Power Conversion & Power Management

Power Supply and Power Integrity Tests

5G CELLULAR DEVICES ARCHITECTURE
Digital Design, Power and RF Components



SYSTEM-LEVEL DEBUGGING
MULTIDOMAIN ANALYSIS



CAN,UART … MIPI-RFFE
CIPR, Ethernet, PCIe,
USB, MIPI-DPHY, (LP)DDR, etc.

System-level Debugging

- ▶ Combine multiple measurements from different DUT interfaces on the same screen
- ▶ Look for possible correlations to determine causes of signal anomalies

HIGH SPEED DIGITAL INTERFACES

Why fast and reliable signal integrity solutions including PCB and interconnect tests are so important for integration of High Speed Digital Interfaces?

HIGHSPEED DIGITAL INTERFACES CHALLENGES

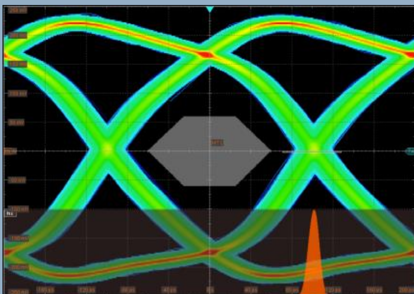
- Signal integrity challenges due to increasing data rates
- Interference issues due to increasing level of integration

For optimal Signal Integrity analysis – T&M equipment needs to collect statistical data fast.

HIGH SPEED DIGITAL INTERFACES
Require Dedicated Tests for Verification & Debugging

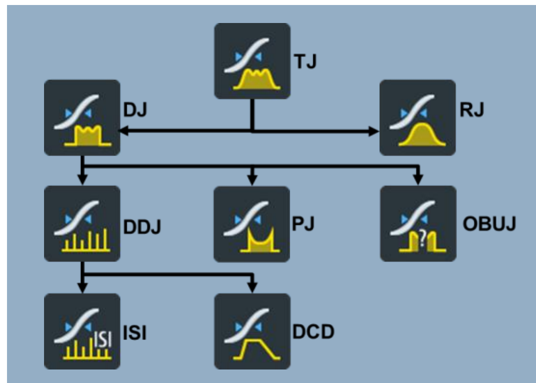
Eye Diagram

- Fast update rate for statistical confidence
- Continuously operating Clock-Data-Recovery (CDR)
- Mask tests
- Deembedding function to compensate transmission loss



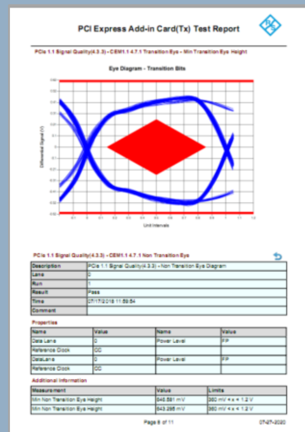
Jitter Analysis

- Break-down of jitter and noise into individual components for characterization & debugging



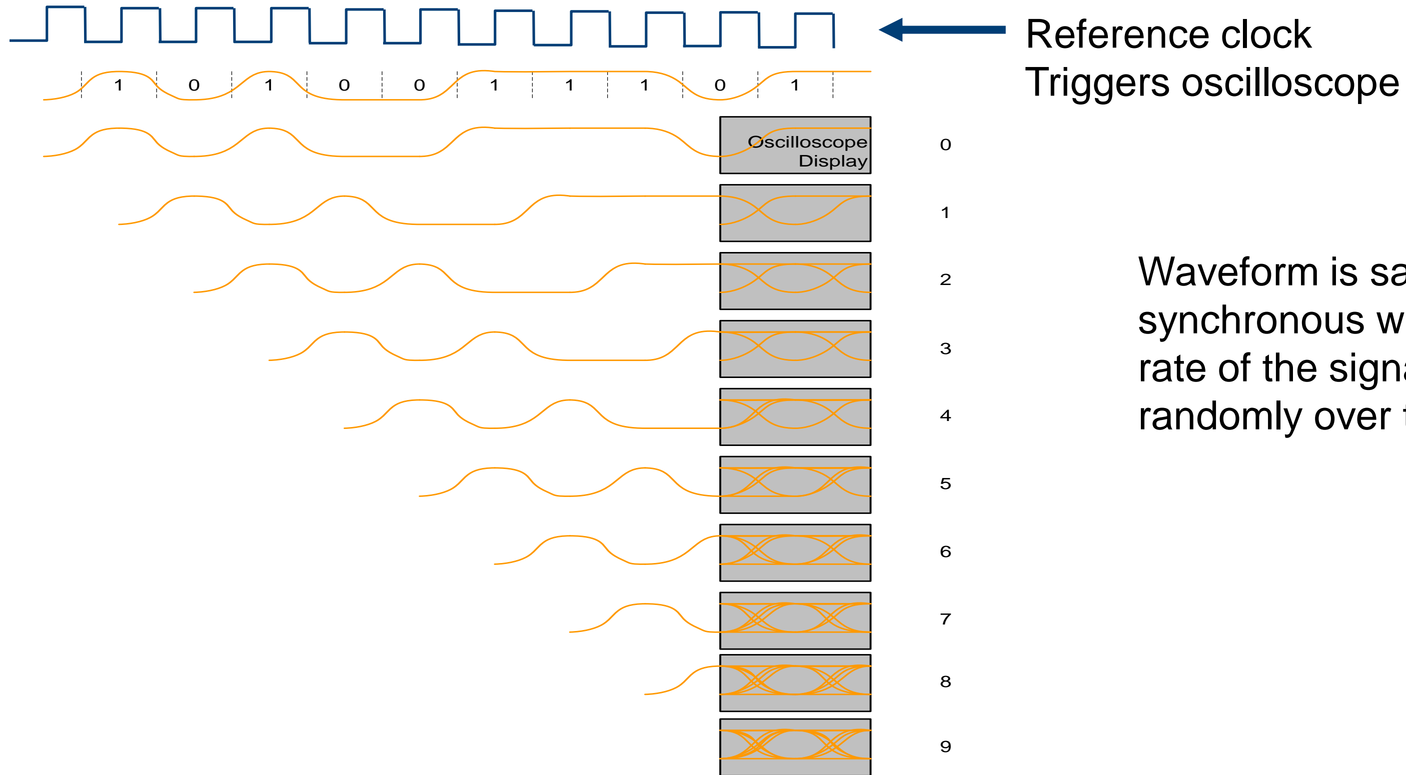
Automated Compliance Tests

- Verify compliance of the physical layer to interface standards and report results



EYE DIAGRAM BASICS

GENERATING EYE DIAGRAMS

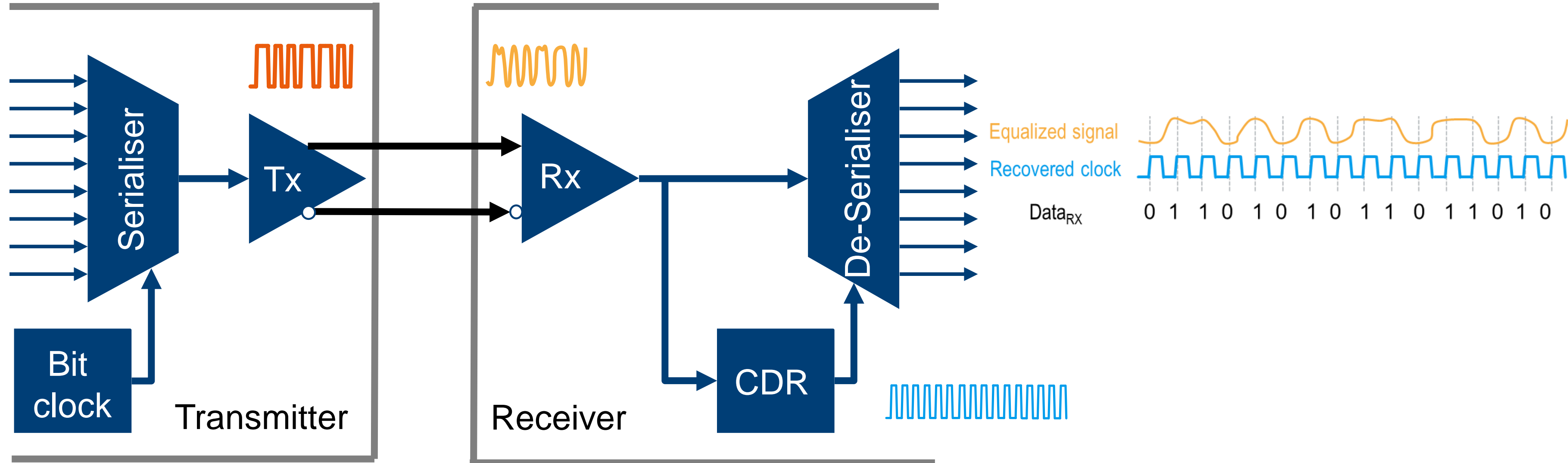


Reference clock
Triggers oscilloscope

Waveform is sampled synchronous with the bit rate of the signal and randomly over time

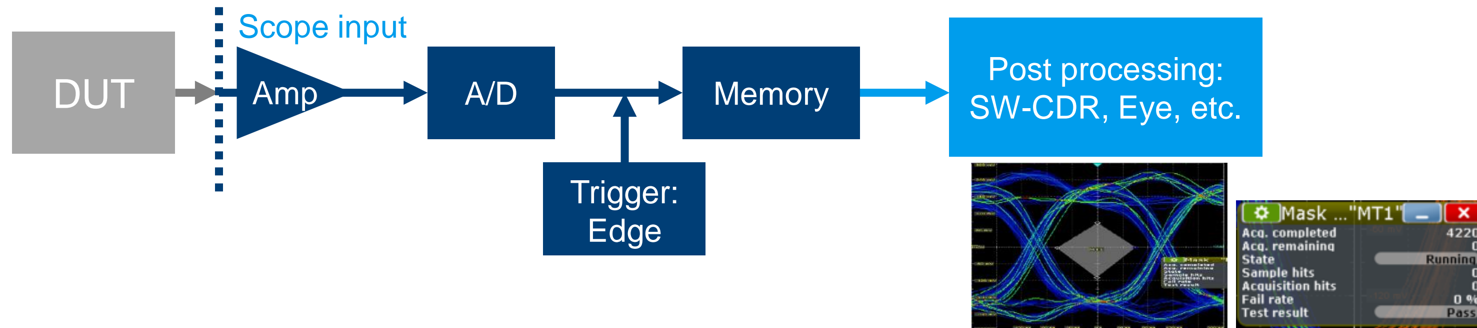
REFERENCE CLOCK FOR EYE DIAGRAMS
CLOCK-DATA-RECOVERY

- Timing Reference can be from a reference clock (parallel clock signal) or from the data signal itself (embedded clock signal)
- Clock data recovery is typically uses a Phase Locked Loop (PLL) or Delay Looked Loop (DLL)



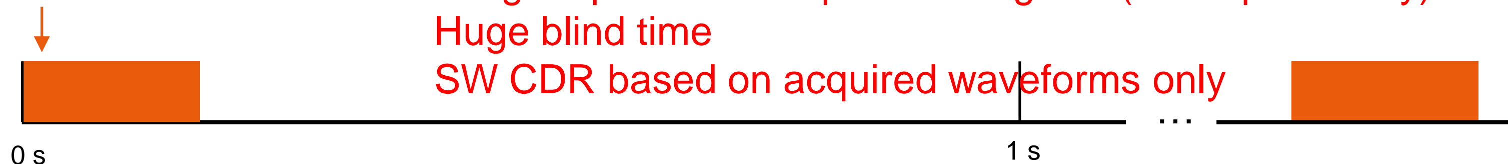
EYE DIAGRAM IN POST-PROCESSING

- Analysis based on a single acquisition with long Record length and SW-CDR in postprocessing
  - Acquired waveform is “folded” over into an eye based on software recovered clock
  - CDR – settling time (typ. >10us) and new synchronization for every new acquisition



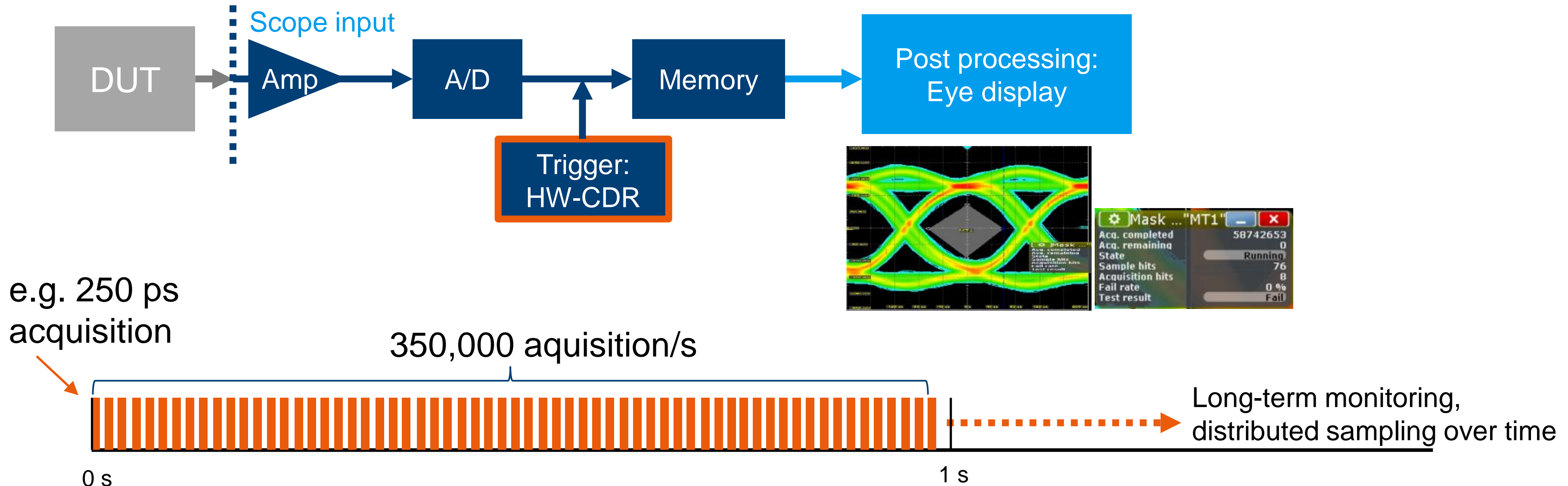
e.g. 100 us acquisition

Long acquisition to capture enough UI (eats up memory)
Huge blind time
SW CDR based on acquired waveforms only



REALTIME EYE DIAGRAM

- Analysis based on a multiple acquisition, short Record Length and CDR in Hardware
  - Acquired bits are overlaid to an eye based on HW-CDR timing
  - CDR – looked once and runs continuously



MAKING IT FAST – REAL-TIME ANALYSIS

Clock Recovered Eye

Trigger On:
16 Gbps Serial Pattern
Differential Signal
De-Embedded Signal
Clock Data Recovered

Real-Time
De-Embedding

Real-Time
Differential Math

Histogram

Millions of
Measurements

~400,000 UI/sec

Horizontal
400 fs 20 GSa/s
1 kSa IT
40 ps/div

Trigger Auto
A: Ser. Pat. Diff1
Level: 0 V

Ch1Wfm1
50 mV/div
0 div 0 V
DC 50Ω BW: 8 GHz
Sample

Ch3Wfm1
50 mV/div
0 div 0 V
DC 50Ω BW: 8 GHz
Sample

Diff1
100 mV/div
0 div 0 V
P: Ch1 N: Ch3

Performance

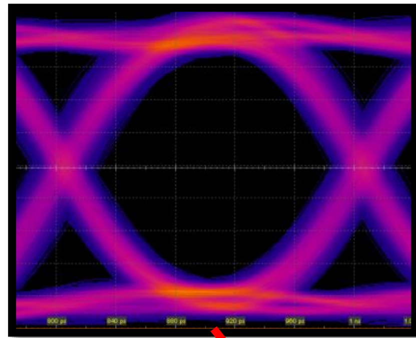
Acq/Fr	12090
Acq/s	398500
T/Fr	0.03

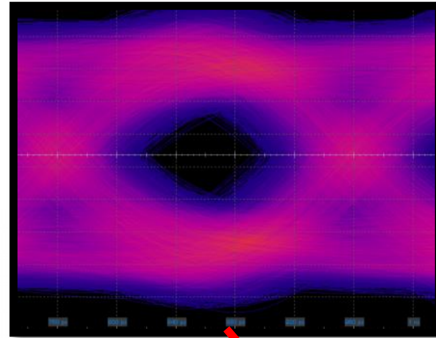
Meas Group 1	
Eye height	695.65 mV
Eye width	149.6 ps
Noise (RMS)	73.203 mV
Eye rise time	56.4 ps
Eye fall time	57.6 ps
Eye bit rate	5.01 GHz
Jitter (RMS)	10.218 ps

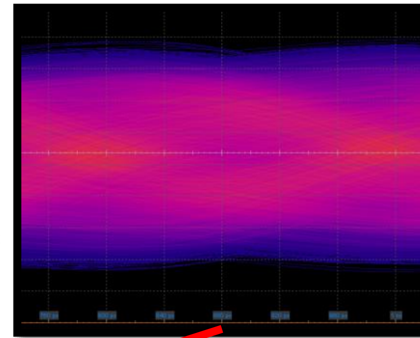
Meas Group 2	
Waveform count	35699

Validation of digital design of next gen devices

CONCEPT OF DEEMBEDDING

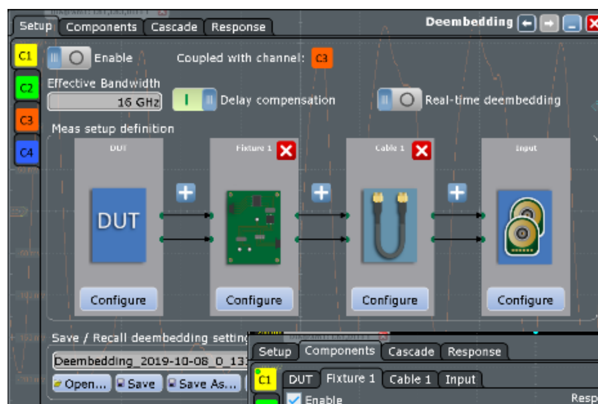




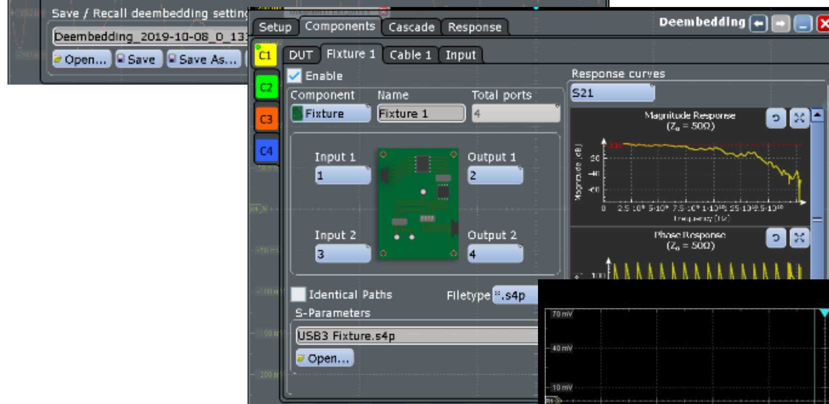


DEEMBEDDING MADE EASIER

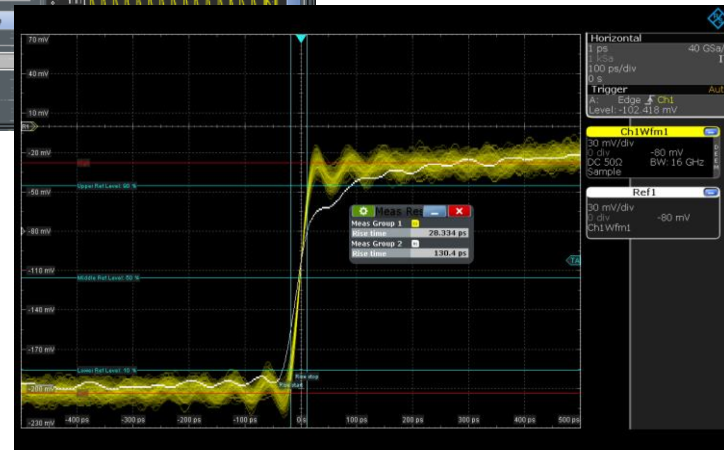
- ▶ Option RTO/P-K121 + RTP-K122
  - – SW and HW (Realtime)
- ▶ Applied during acquisition
- ▶ Trigger on de-embedded signal
- ▶ No update rate change
- ▶ Proven Cable / Probe
  - – removes transmission loss effects
  - – B7 pulse source



1. Define System Parameters



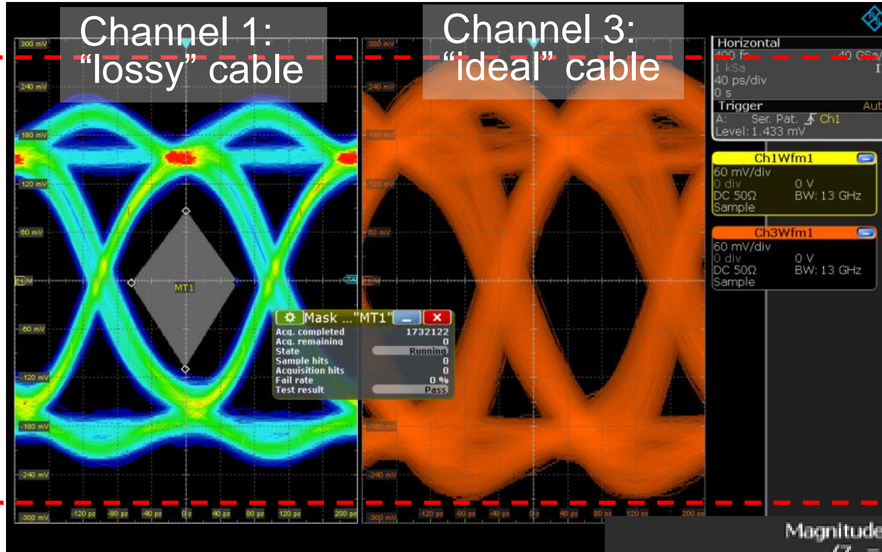
2. Import S-parameter



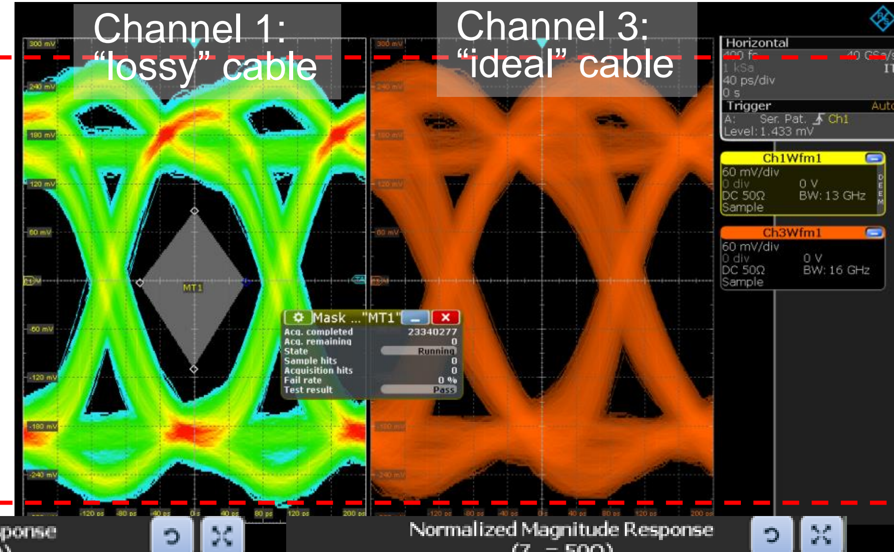
3. Observe deembedded response

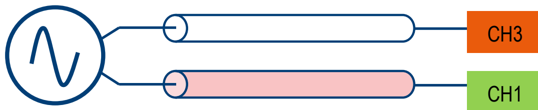
EXAMPLE – USB 3.2 GEN1 SIGNAL

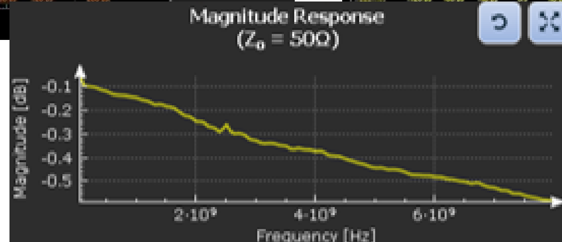
De-embedding: OFF

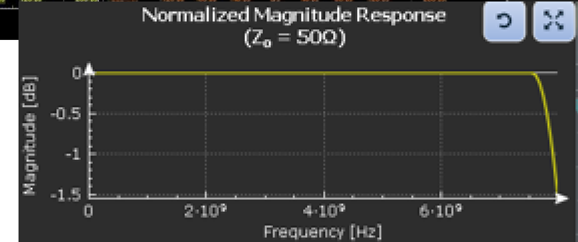


De-embedding: ON



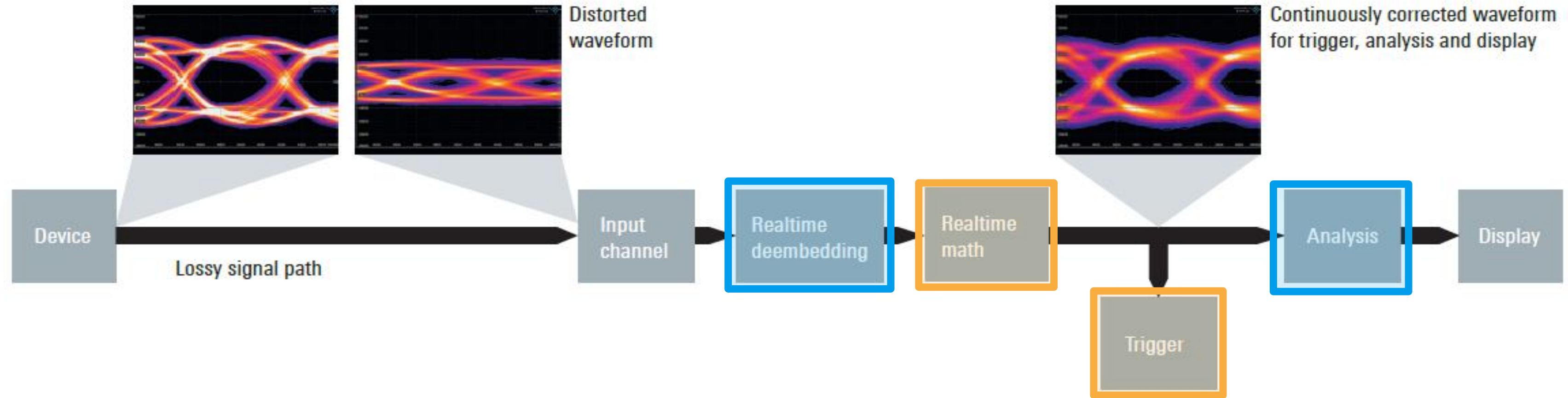






REALTIME SIGNAL INTEGRITY UP TO 16 GHZ

Realtime Deembedding Architecture



Fast debugging

- 20 GSa/s: 750k wfm/s
- 40 GSa/s: 300k wfm/s

- Realtime transmission loss compensation

- RT-Math: V_{Diff} / V_{CM} Signals
- 16 Gbps Serial Trigger/CDR
- 25 ps glitch trigger

HW accelerated analysis:

- Mask Test
- Histogram

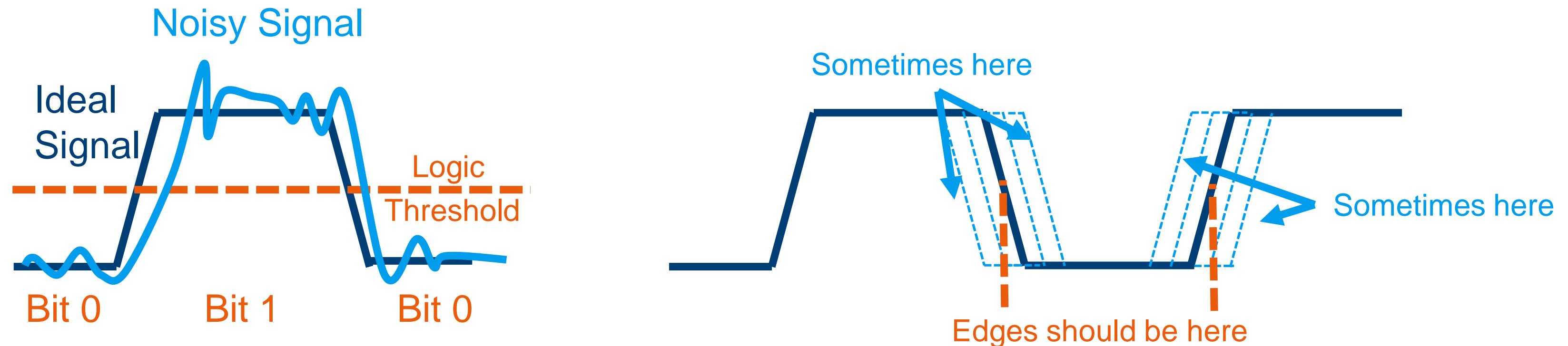
No time consuming post-processing

JITTER BASICS

WHAT IS JITTER?

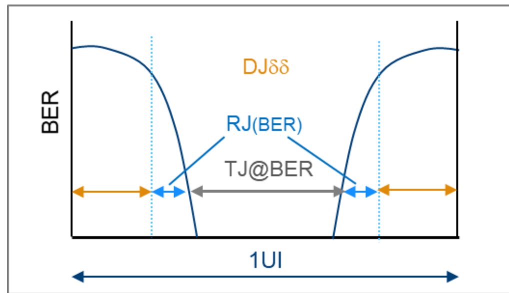
Timing Uncertainty | **Frequency Domain Phase Noise** | **Time Domain Jitter**

Jitter is the short-term variations of a digital signal's transition edges from their ideal position



REASONS TO MEASURE JITTER

TJ Stability



Bathtub Plot

Measure Bit Error Ratio (BER) to 10^{-12}

"1 Bit Per every 1 Trillion Bits"

Oscilloscopes estimates it

Standards Requirement

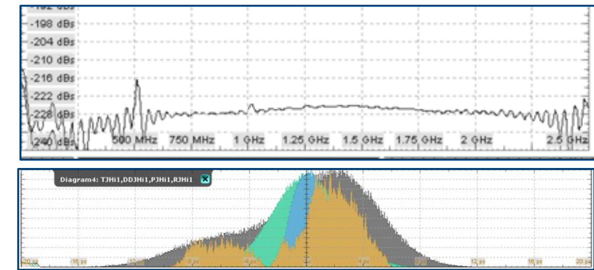
Table 4-4: Total System Jitter Budget for 5.0 GT/s Signaling

Jitter Contribution	Max RMS Rj (ps)	Max Dj (ps)	Tj at BER 10^{-12} (ps)
Tx	1.4	30	50
Ref Clock	3.1	0	43.6
Media	0	58	58
Rx	1.4	60	80
Linear Total Tj:			231.6
Root Sum Square (RSS) Total Tj:			200

USB spec require RJ, DJ and TJ @ 10^{-12}

Standards require separation and provide limits

Debugging



Find root cause sources

What-if you fix it? Analysis

JITTER COMPONENTS

Total Jitter is composed out of several jitter contributions:

- Random Jitter: "unbounded"
- Deterministic Jitter: usually "bounded"

Total Jitter (TJ)

EVOLUTION OF SEPARATION ALGORITHMS

A New Method for Jitter Decomposition Through Its Distribution Tail Fitting

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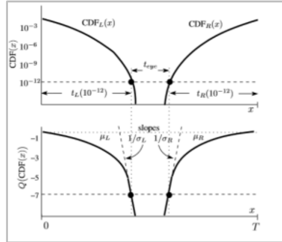
Abstract

We present a new time-domain jitter separation method. Such a method automatically searches and fits the tail parts of the jitter histogram with nonlinear jitter models and

media, reflections, cross-talk, electromagnetic interference (EMI), systematical modulations, and pattern dependency, for DJ; and thermal noise, shot noise, flick noise, random modulation, non-stationary interference, for RJ. In the real world applications, what is measured, in general, is the



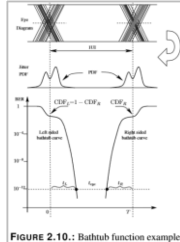


FIGURE 2.10.: Bathtub function example.

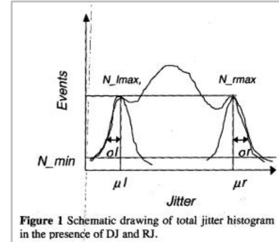
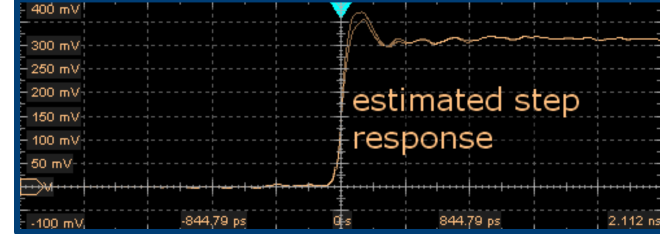


Figure 1 Schematic drawing of total jitter histogram in the presence of DJ and RJ.



Jitter Separation

"Tail"-fitting &
Dual-Dirac-Model

Extension with
Transformation into Q-Space

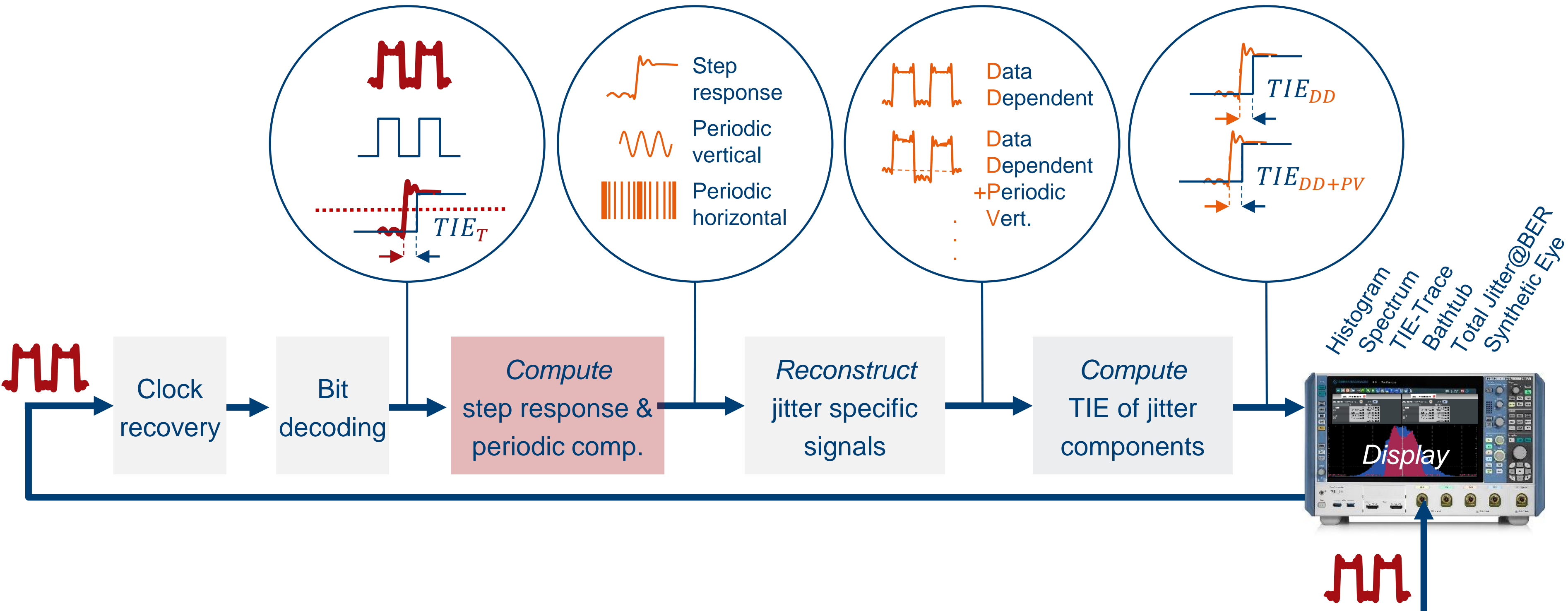
R&S's modern approach:
Signal-Model-based

2000 **2008** **2020**

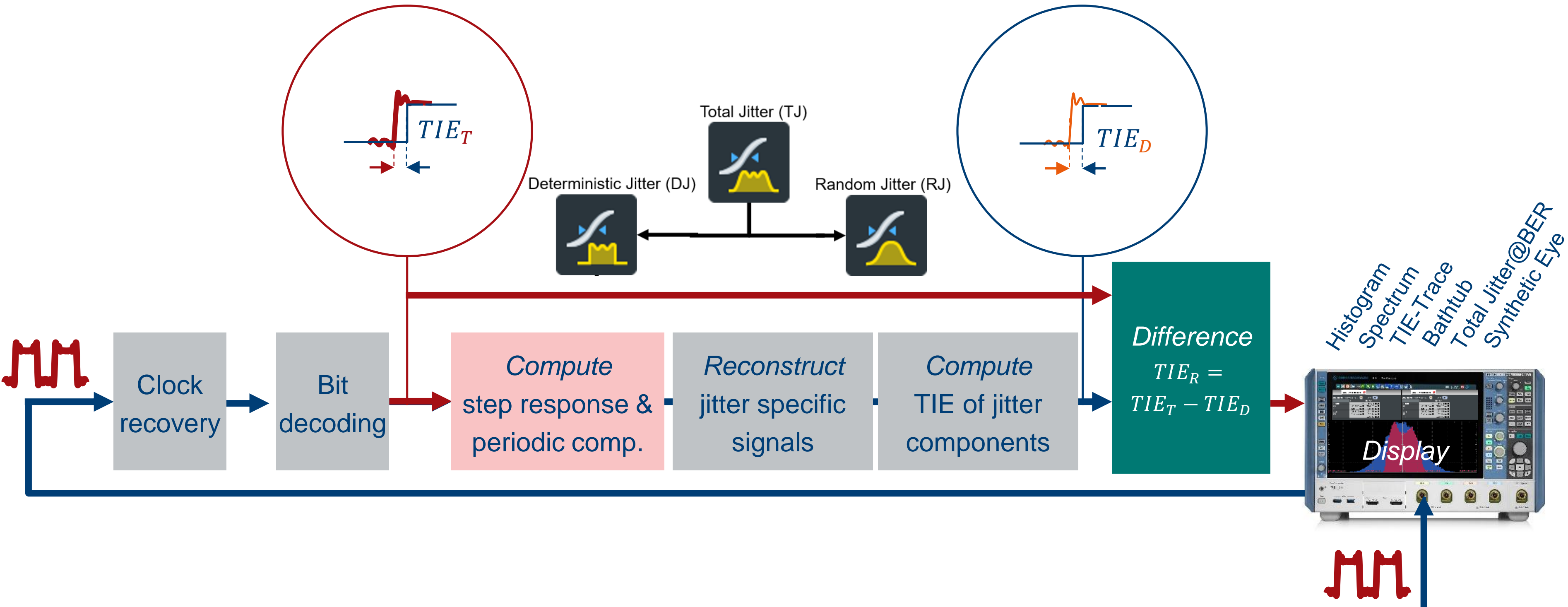
Extensions DDJ/ISI/DDC and
spectrum view for PJ, etc.

Extension with
Noise Separation

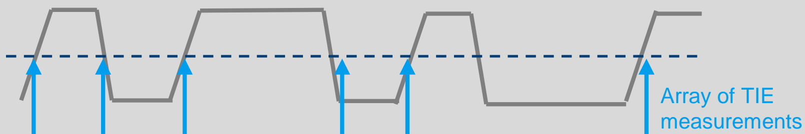
NOVELL R&S APPROACH DETERMINISTIC COMPONENT



NOVELL R&S APPROACH RANDOM COMPONENT

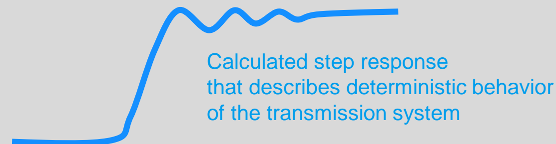


Legacy TIE-based approach



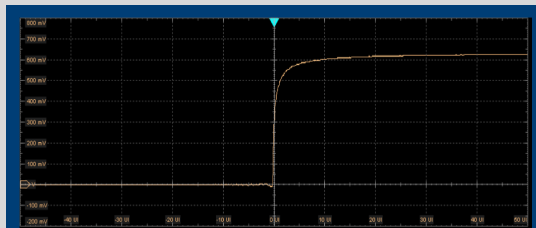
- Reduce Signal information to a set of TIE measurements at a voltage threshold

R&S's Signal Model-based approach

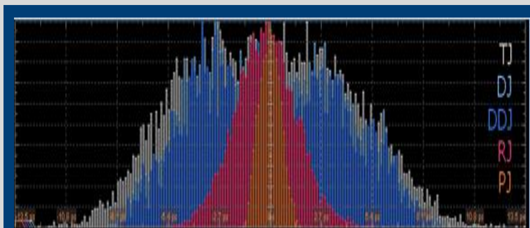


- Parametric signal model with all signal information for most accurate and reliable jitter decomposition

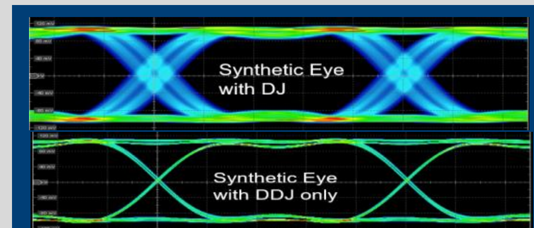
Use more result data for faster debugging



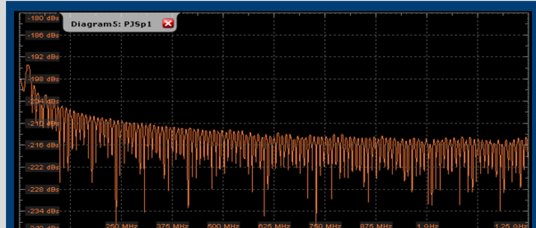
Understand channel characteristic



View individual jitter components



Select what jitter component to include

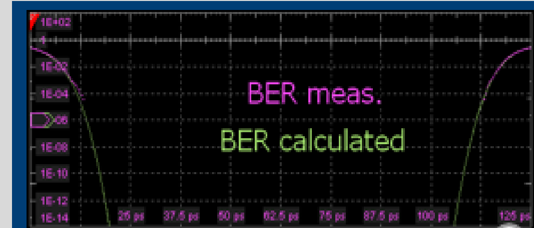


Detect root cause of PJ in spectrum

Periodic components 1

	Frequency	Value	Direction
1	19 MHz	50.481 ps	Horizontal
2	4.5032 MHz	28.695 ps	Horizontal
3	57.001 MHz	13.543 ps	Horizontal
4	684.63 kHz	4.8239 ps	Horizontal
5	95.001 MHz	4.8077 ps	Horizontal
6	19.685 MHz	1.977 mV	Vertical
7	39.369 MHz	1.4551 mV	Vertical
8	59.055 MHz	747.16 µV	Vertical
9	6.2992 GHz	54.494 µV	Vertical
10	6.2598 GHz	32.261 µV	Vertical

Detect root cause of PJ in table report



Calculate TJ for all or selected components

AUTOMATED COMPLIANCE SOFTWARE

TESTING BASED ON COMPLIANCE REQUIREMENT

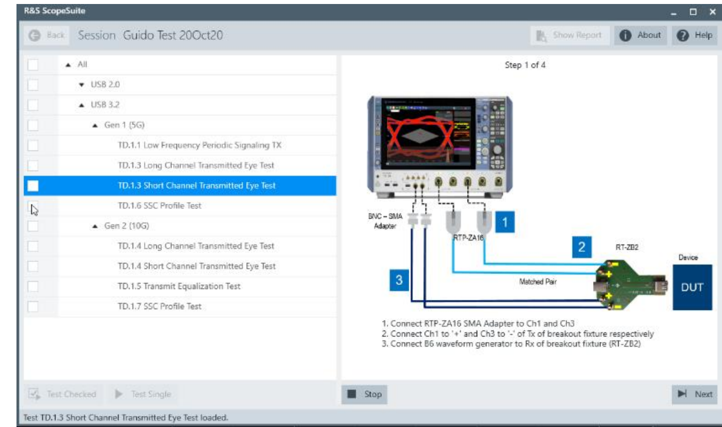
Electrical specifications in each standard committees covers all the measurement requirement but it will be difficult to manually execute all the requirements

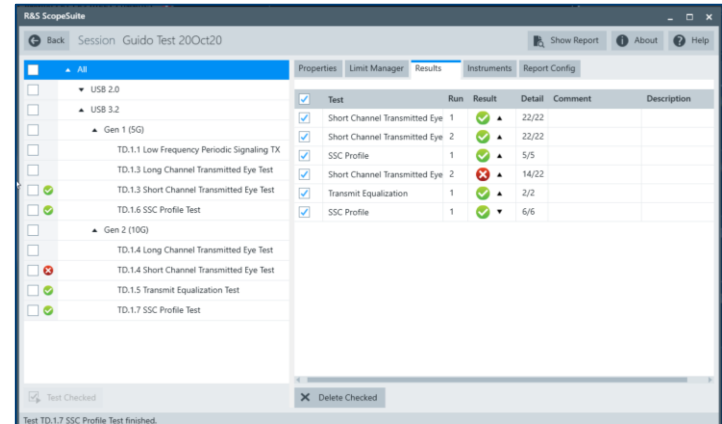
- ► Specified measurement algorithm and setup
- ► Additional signal processing as per required by standards (deembedding & CDR)
- ► Guidance to depict the set necessary test modes and fixtures setup

Most standard bodies still required DUT to be tested by official test house or allow submission of compliance report.

SCOPESUITE COMPLIANCE

- ▶ Automated Compliance Test following standards
- ▶ R&S ScopesSuite Wizard
  - – Guided test execution
  - – Flexible test operation (incl. re-tests)
  - – Limit manager
  - – Detailed test reports





POWER INTEGRITY

What are the right tools and analyzing functions for appropriate characterizing & debugging?

POWER INTEGRITY CHALLENGES

- Increasing number of power rails
- Lower margins due to lower supply voltages
- Interferences due to dense designs of mixed technologies

An optimal solution for characterizing and debugging DC power rails demands suitable probes & oscilloscopes.

POWER INTEGRITY
Requires Dedicated Tools for Verification & Debugging

The Right Scope

- ► Fast update rate
- ► Min. vertical scale: 1..2 mV/div in HW at full bandwidth
- ► Low noise
- ► Support of specialized probes also on high-performance class instruments

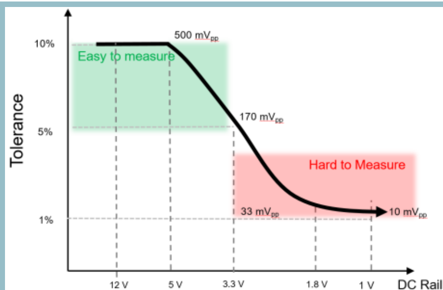
Specialized Probes

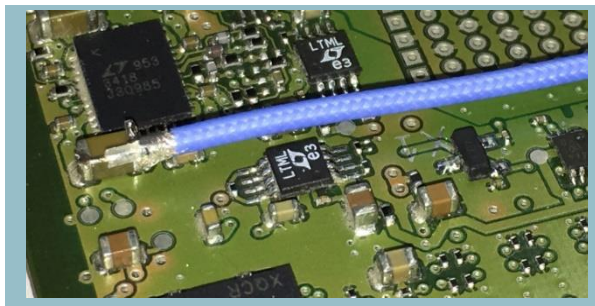
- ► Power Integrity Probe
  - Bandwidth >2 GHz
  - Low noise with 1:1 attenuation
  - Extended offset range
  - Connectivity
- ► Current probes, etc.

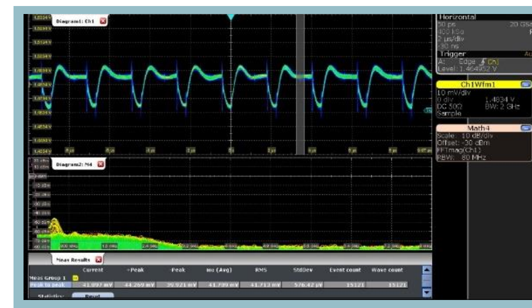
Dedicated Analysis Functions

Typical measurements

- ► Ripple, Load step response
- ► Power-up/down, Sequencing
- ► Drift over temperature and input voltage
- ► EMI debugging / harmonic analysis





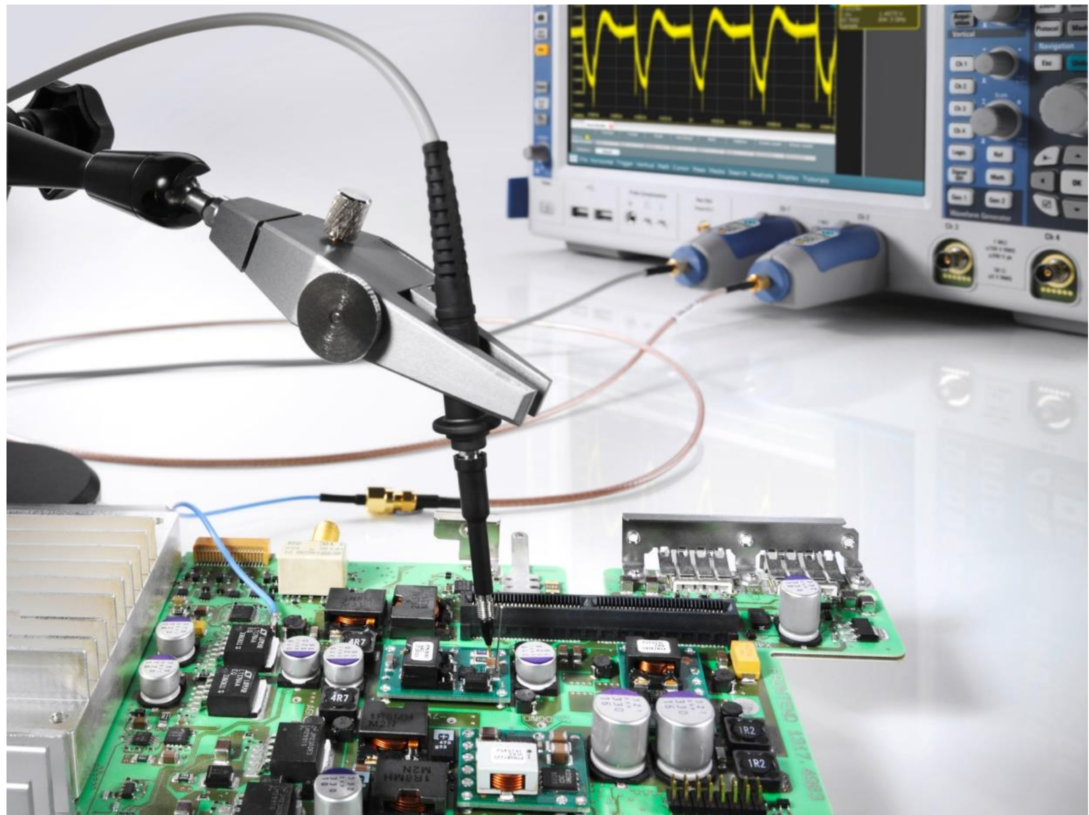


R&S POWER INTEGRITY SOLUTION

- ► Low Noise
- ► Fast FFT
- ► Fast Update Rate

- ► Low-Price Alternatives
  -RTM / RTA Oscilloscopes

- ► **Superior Power Rail Probes**

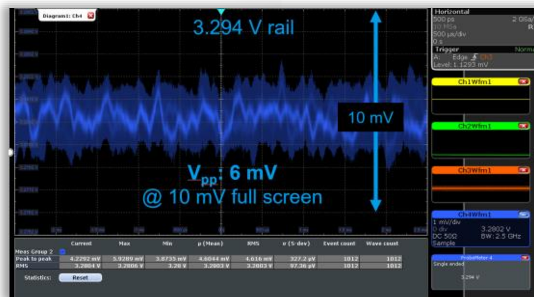


Providing Unique Power Integrity Analysis Functions

DEDICATED POWER RAIL PROBING SOLUTION

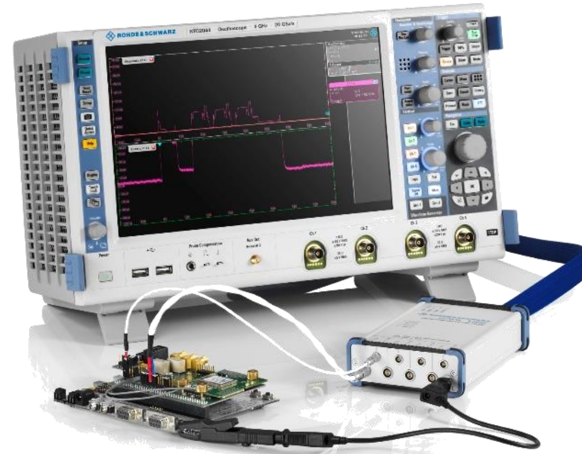
RT-ZPR20/40 Power Rail Probes

- Active, single-ended probe
- Very low noise with 1:1 attenuation
- Best in class offset compensation capability



RT-ZVC Probe for Power Consumption

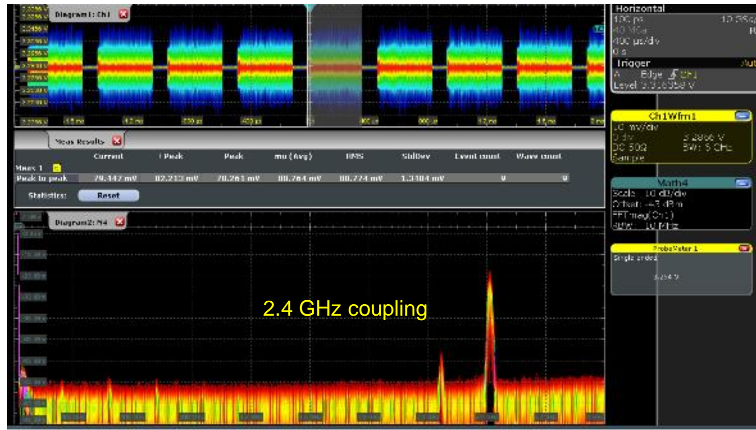
- 18-bit vertical resolutions for each channels
- 0.1% measurement accuracy
- <2 nA AC RMS noise



UNIQUE ANALYSIS FUNCTIONS IN ONE INSTRUMENT

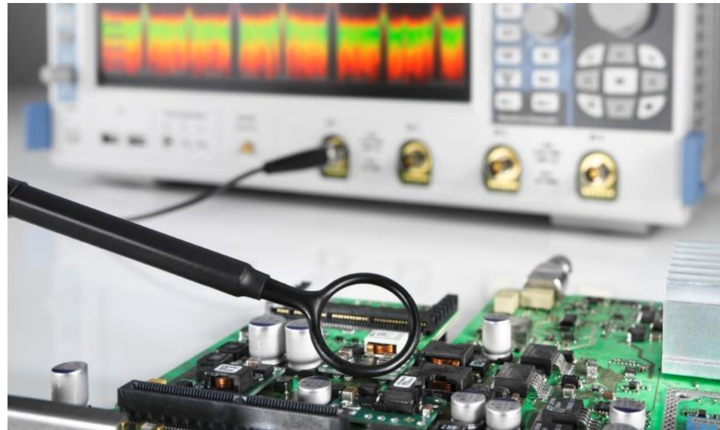
Superior FFT Performance

- Fast and responsive FFT to detect interferer
- Multi-channel Math FFT for comparison
- Time and frequency domain correlation



EMI Debugging Capability

- Log scale display to match Test Receiver presentation
- Limit line capability with zone trigger to detect violation
- Math on FFT for further EMI testing & analysis



DEDICATED INSTRUMENT FOR SPECIALIZED TESTING

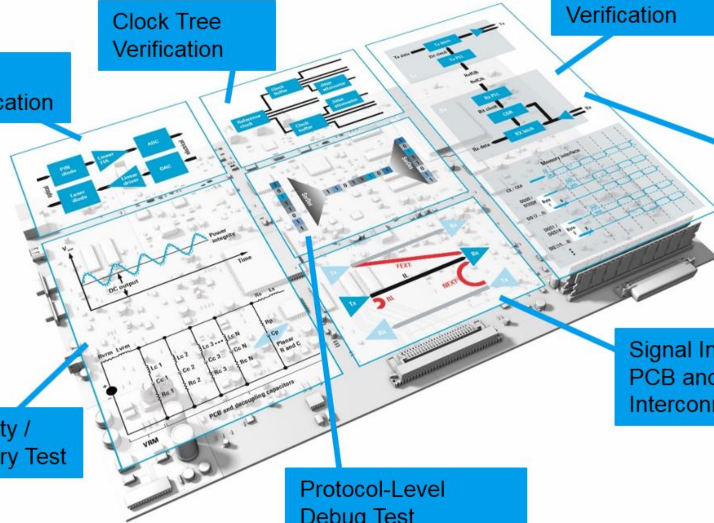
Using the best tool for specific measurements.

DIGITAL DESIGN TEST

Scopes
e.g. RTP, RTO, RTE

Network Analyzers
e.g. ZNA, ZNB, ZNL

Phase Noise Testers, Spectrum Analyzers
e.g. FSWP, FSW

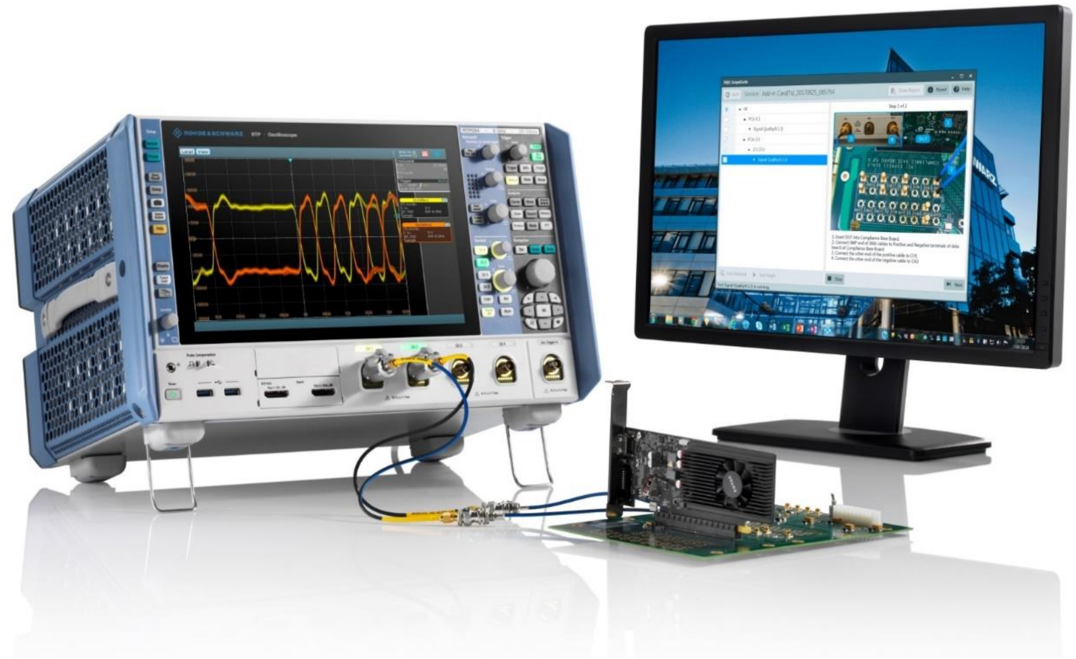


Power Supplies
e.g. HMP, NGL

Signal Generators
e.g. SMA100B, SMW

R&S RTP HIGH-PERFORMANCE OSCILLOSCOPE

- 4-16 GHz bandwidth
- Dedicated hardware for real-time Signal-Integrity
- Most compact & silent for everyday use in the lab

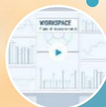


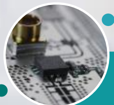
Providing Unique Signal Integrity Analysis Functions

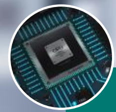
SUMMARY

- Digital design is the backbone for the next generation devices and infrastructures
- Technology advances push complexities into design as well as measurement requirements
- Signal integrity ensure best performance for design interconnects which need a versatile tool to help characterizing and debugging
- Power integrity is often forgotten but plays an important role that affects the design performance

Next generation build on the fundamental performance of the devices and infrastructure, making sure these designs works will be crucial for your 5G Testing Journey!







15th June — Production test strategies and smart solutions

8th June — Making 5G lab testing more realistic with R&S®CM360º

1st June — ONE tool for automated device testing

25th May — Simplifying 5G mobile device testing

11th May — Challenges to 5G mmWave component characterization

4th May — Validation of digital design of next gen devices

5G DEVICE TESTING JOURNEY

Webinar Series

5G Device testing journey

THANK YOU

MAY THE FORCE BE WITH YOU

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