返馳電源傳導電磁干擾抑制 Part 1
Conducted Emission EMI Reduction of Flyback Power Supplies

王信雄博士

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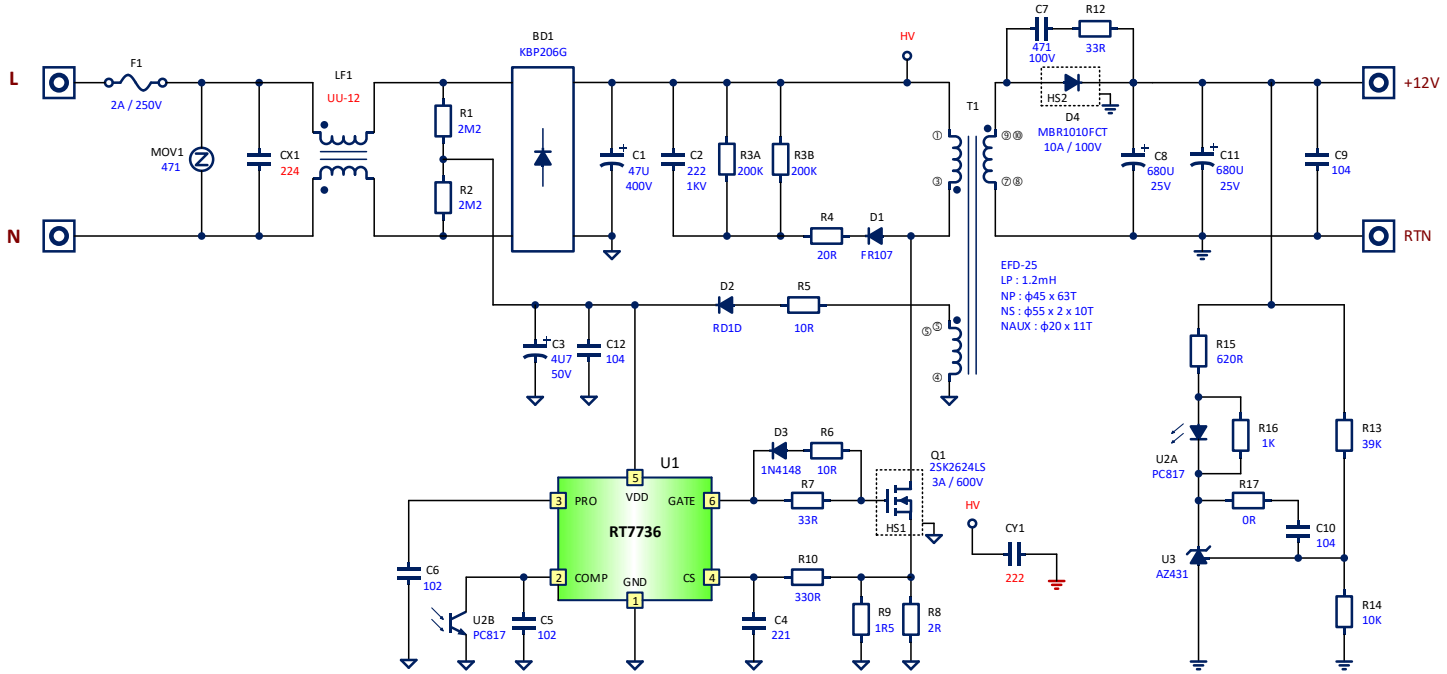
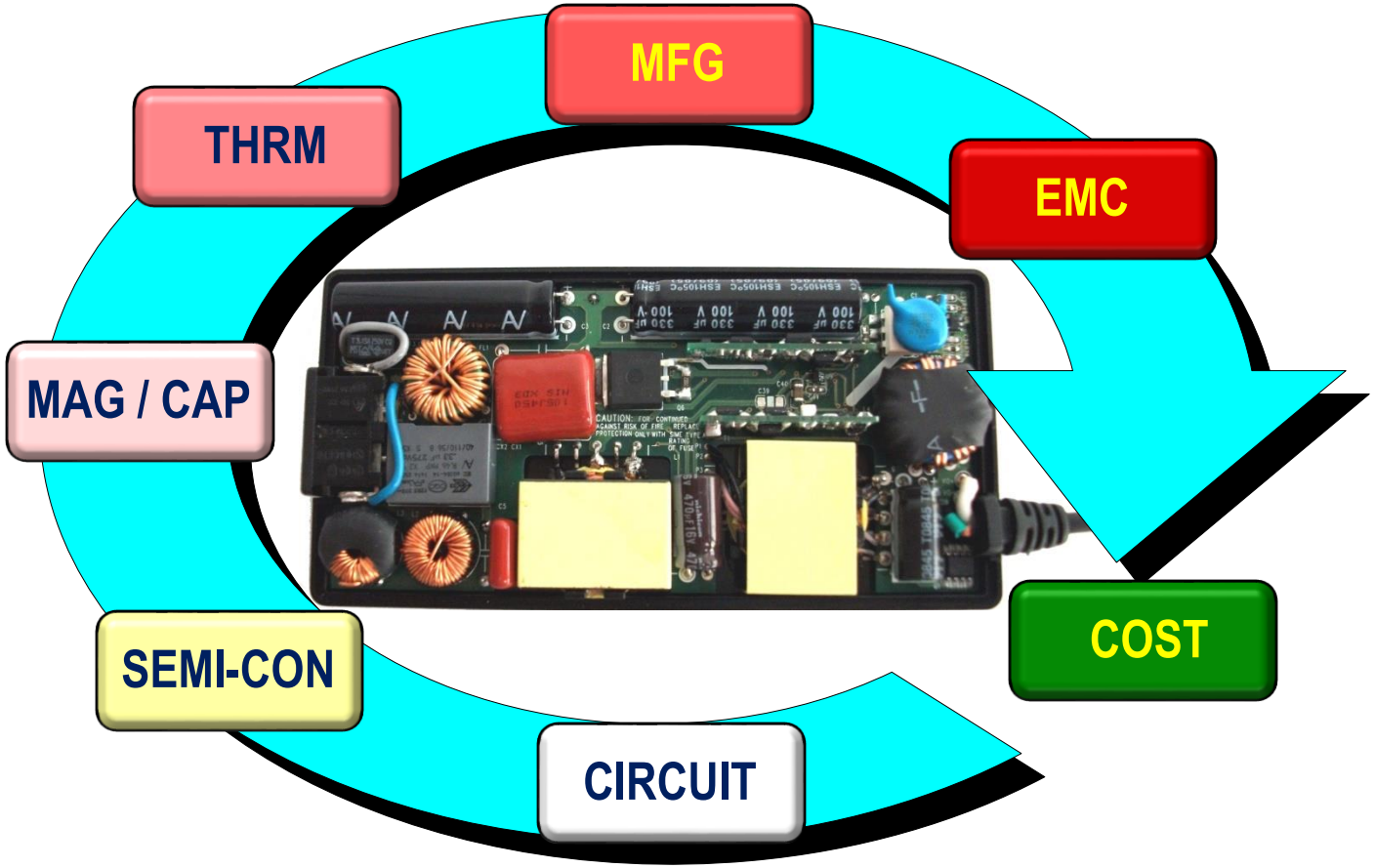
王 信 雄

March, 2022



切換式電源供應器技術



關於切換式電源電磁干擾的問題

- 為甚麼切換式轉換器是電磁干擾源 (Noise Source)？
- 甚麼是差模(DM)雜訊和共模(CM)雜訊？和法規標準有甚麼關係？
- 緩衝吸收(Snubber)電路與 EMI 有甚麼關係？
- 閘極電阻加大些，EMI 是不是就會好一些？
- 為甚麼稱 X 電容和Y電容，它們的功能為何？
- 共模電感多繞幾匝，是不是就可以解 EMI？
- 設計濾波器時要不要考濾電感、電容和 PCB 的寄生參數？
- 混成扼流器(Hybrid Choke)一個抵兩個用，真的這麼神奇？
- 次級負載接地與共模雜訊的傳遞有甚麼關係？
- 改變變壓器繞線結構，EMI 就改變了，為甚麼？
- 變壓器級間電容與共模雜訊有甚麼關係？怎麼繞製最好？
- 初次級間Y 電容的作用如何？ 怎麼接？ 能不能做到 NoY 的設計？
- EMI 可以用電腦軟體模擬分析嗎？

關於切換式電源電磁干擾的問題

還有 …

為甚麼EMI防制有那麼多設計準則，

但是，例外更多？

類比 + 非線性 + 高頻(雜散參數)

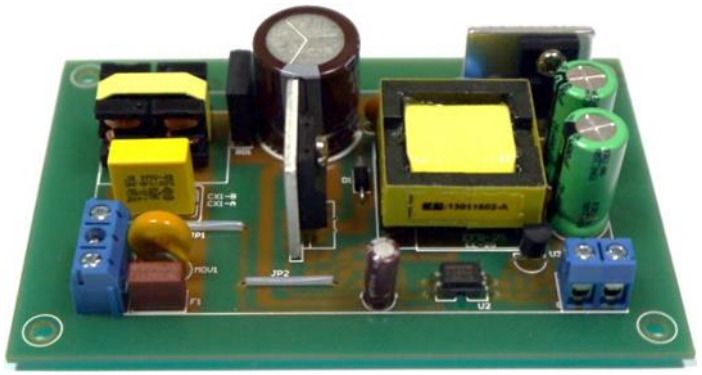
內容大綱：Part I

- 傳導 EMI 基礎介紹
- 雜訊頻譜與傅立葉轉換
- EMI 標準量測與國際法規
  - LISN、EMI 接收機
- 差模 / 共模雜訊與耦合途徑
- 雜訊受害者 / 檢知器 (LISN)
- 差模與共模雜訊分離器
- 濾波器特性分析與雜訊濾波器設計
  - EC Cap、X/Y Cap、DM/CM Choke 及 Hybrid Choke
- 範例
  - 19V/30W、12V/24W離線式Flyback 電源

內容大綱：Part II

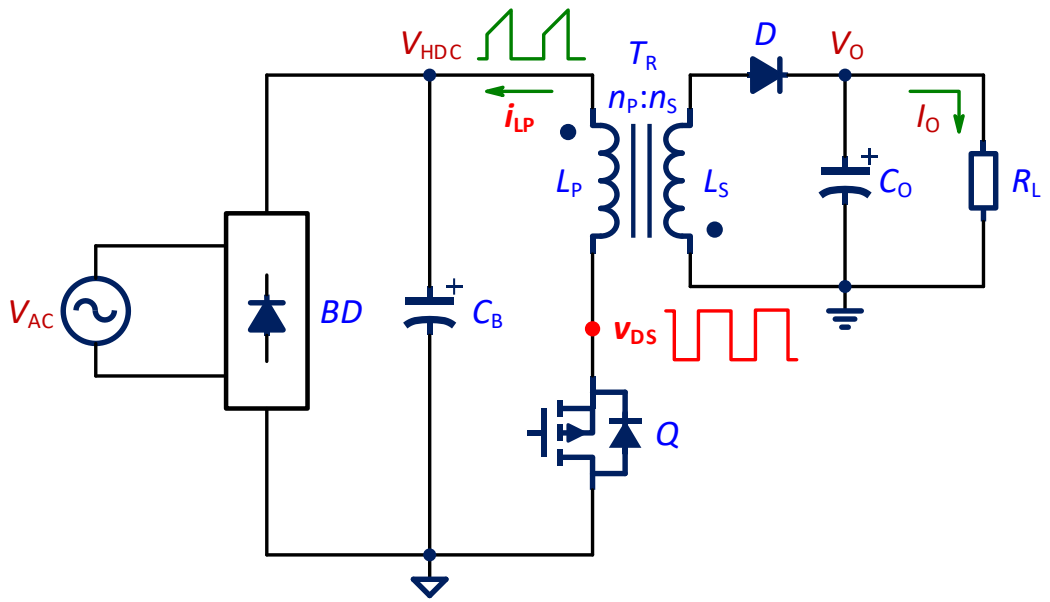
- Flyback 轉換器差模與共模雜訊傳遞模型
- Flyback變壓器繞組與共模雜訊傳遞
- 負載接地與共模雜訊傳遞
- 初次級間Y 電容的角色
- 濾波器特性分析與雜訊濾波器設計
- 變壓器繞製與EMI表現範例
  - 12V/24W 離線式Flyback 電源
- 傳導雜訊 SIMPLIS 模擬
  - 阻抗、插入損失、Flyback 模擬
- 示波器 FFT 量測傳導 EMI 頻譜 (視頻演示)

離線24W返馳式電源供應器電路圖



EMI 量測時常規的頻譜

- 測試條件
  - 輸入電壓：110V/60Hz
  - 輸出電壓：32V
  - 輸出功率：20W
  - 無接地線 (負載回線地不接大地)

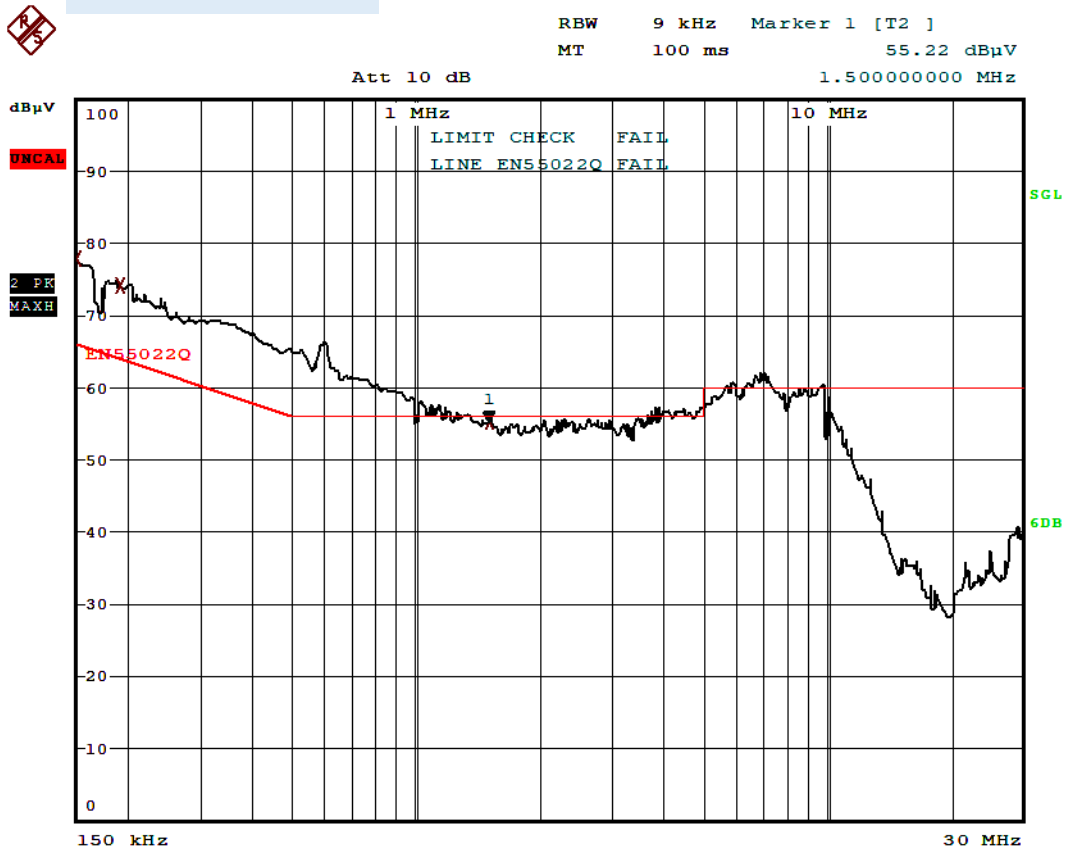


- 測試項目，PK (Max Peak)
  - L (Line, L1)
  - N (Neutral, L2)
  - CM (Common Mode)
  - DM (Differential Mode)

- 脈衝型電流 $i_{LP}(t)$
- 脈衝型電壓 $v_{DS}(t)$

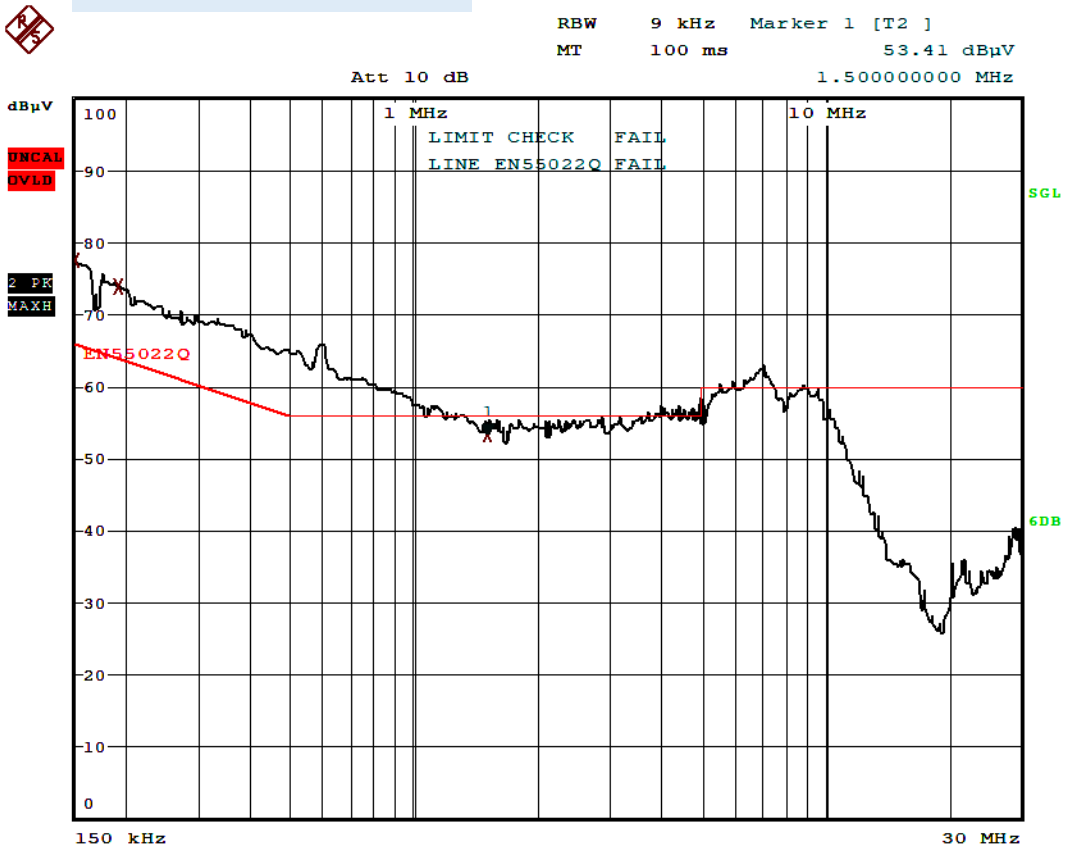
EMI 量測時常規的頻譜

L1 : L (Line)



TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2 Max Peak	150 kHz	77.79	11.79
2 Max Peak	190 kHz	74.16	10.12
2 Max Peak	1.5 MHz	55.22	-0.77

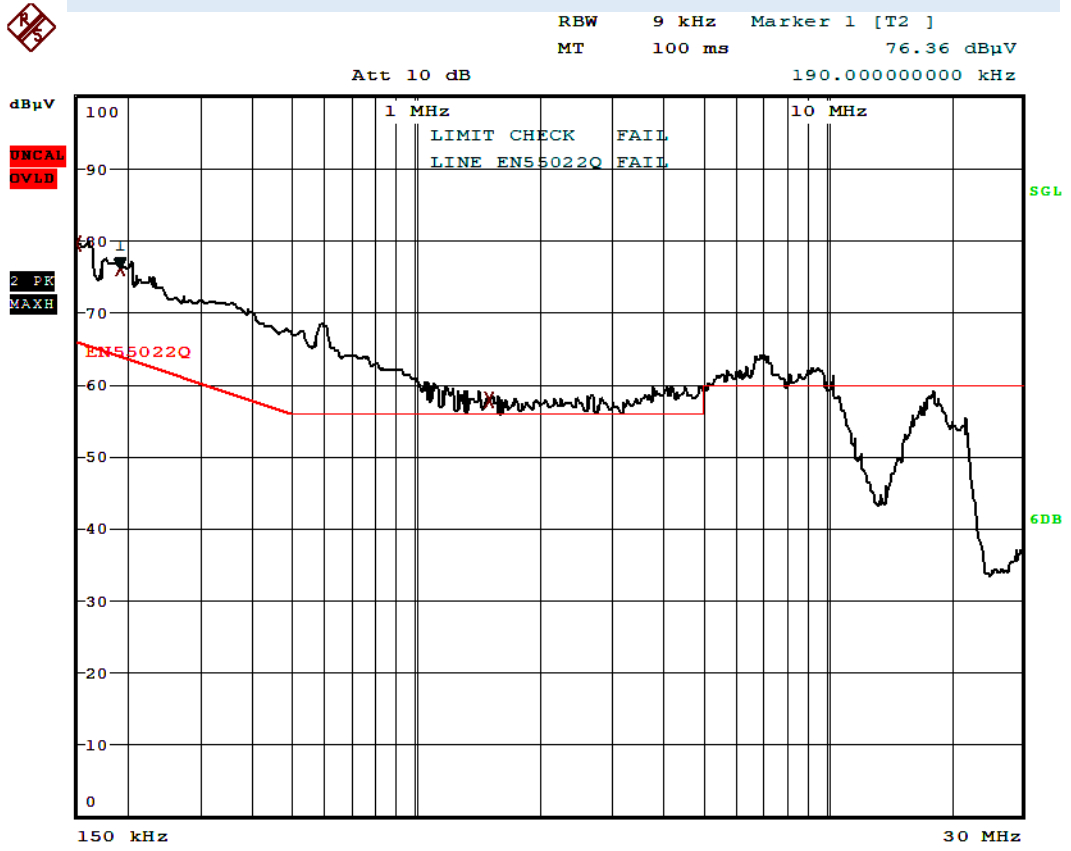
L2 : N (Neutral)



TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2 Max Peak	150.5 kHz	77.48	11.51
2 Max Peak	191 kHz	73.99	10.00
2 Max Peak	1.5 MHz	53.41	-2.58

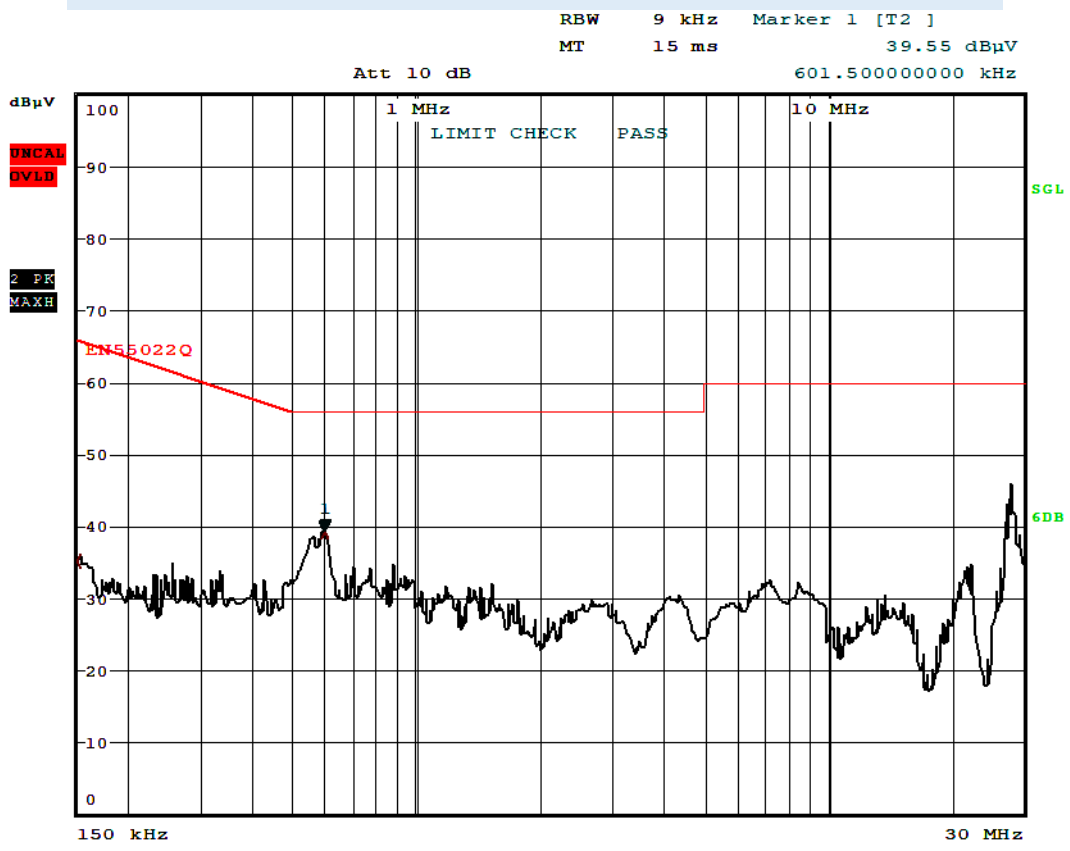
EMI 量測時常規的頻譜

DM (差模雜訊，Differential Mode Noise)



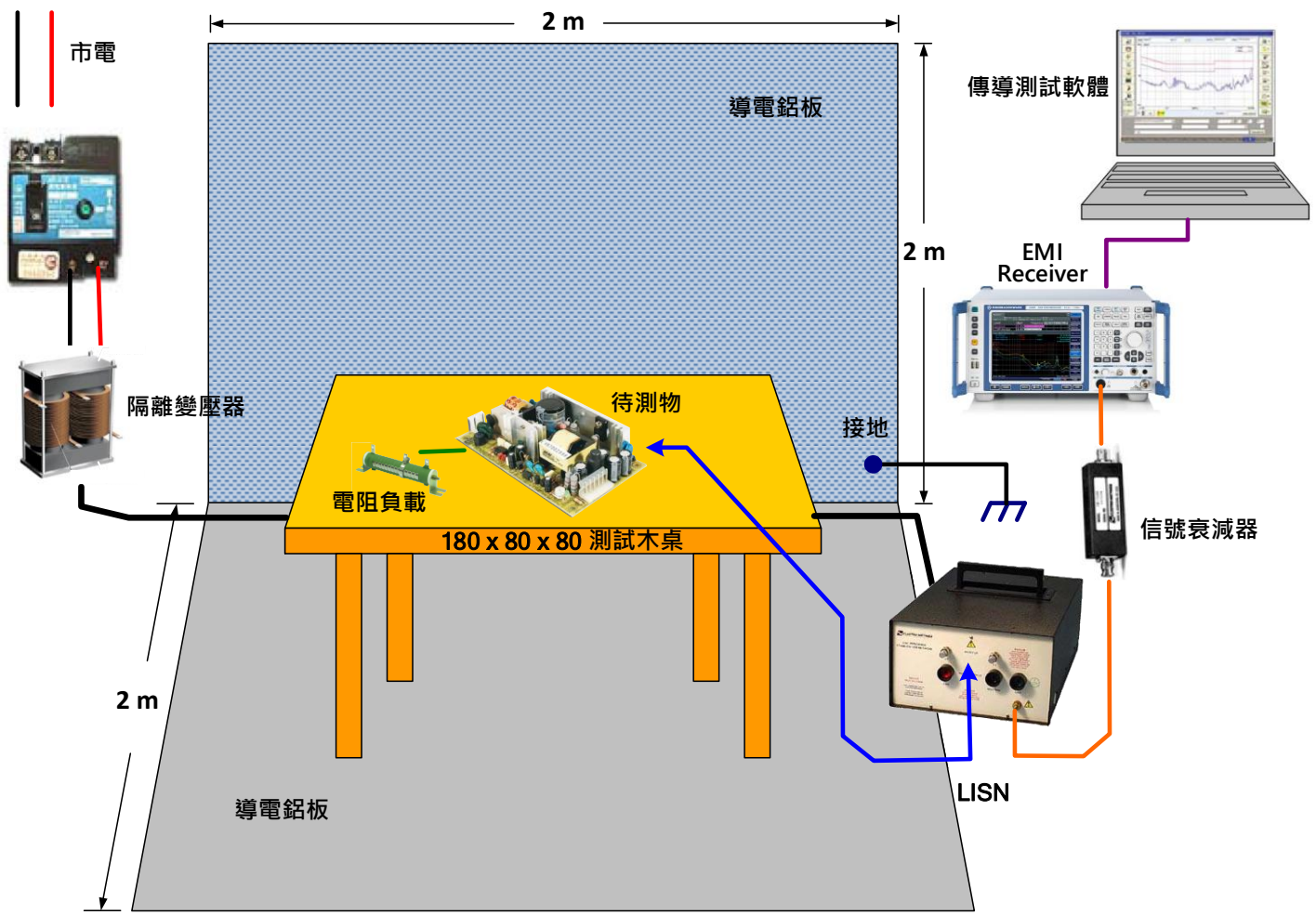
TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2 Max Peak	150 kHz	79.78	13.78
2 Max Peak	190 kHz	76.36	12.32
2 Max Peak	1.5 MHz	57.80	1.80

CM (共模雜訊，Common Mode Noise)



TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2 Max Peak	150 kHz	35.32	-30.67
2 Max Peak	601.5 kHz	39.54	-16.45

傳導 EMI 量測標準配置



頻譜分析儀

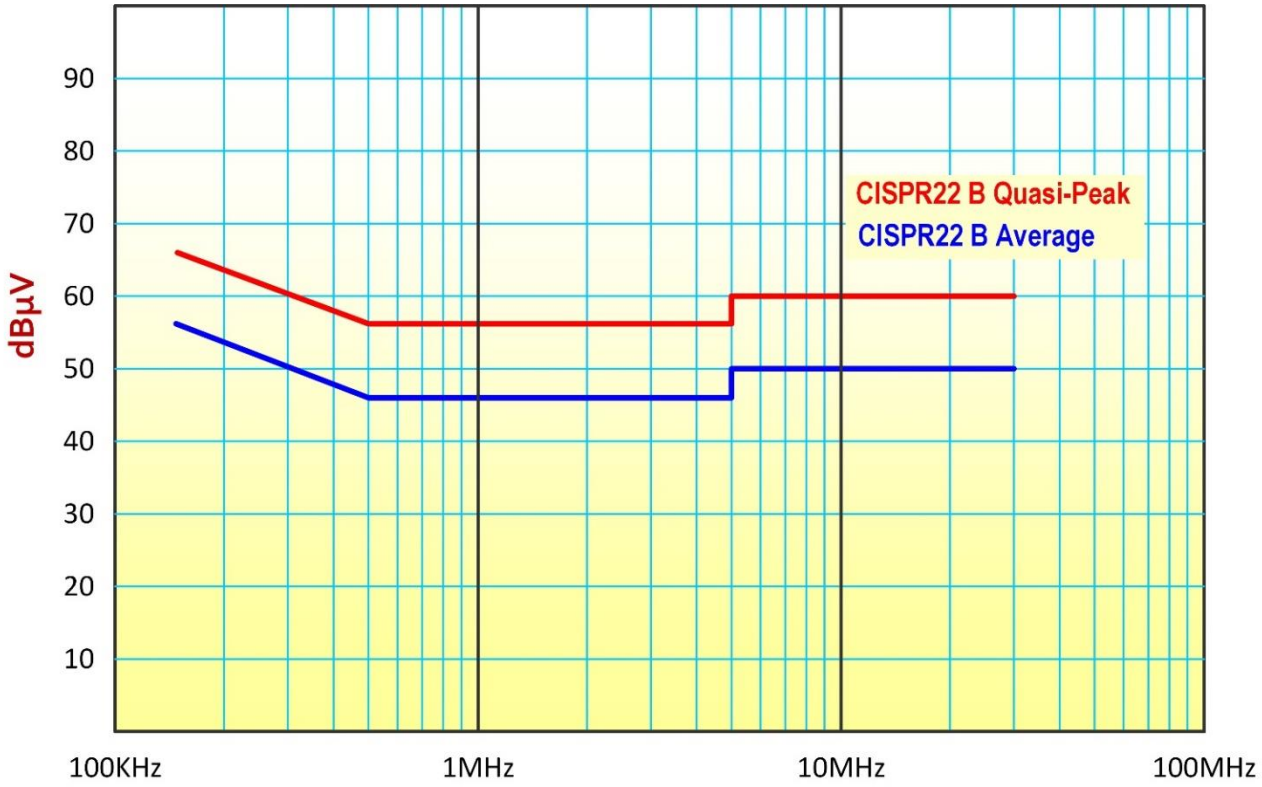
EMI 接收機

LISN
(ETS EMCO 3810)

LISN (EM-7820)

信號衰減器

傳導 EMI 法規 (EN55022 / EN55032)



CLASS A (Industrial)								
Frequency (MHz)	FCC Part 15				CISPR 22			
	Quasi-Peak		Average		Quasi-Peak		Average	
	dBuV	mV	dBuV	mV	dBuV	mV	dBuV	mV
0.15 ~ 0.45	NA	NA	NA	NA	79	9.0	66	2.0
0.45 ~ 0.5	60	1.0	NA	NA	79	9.0	66	2.0
0.5 ~ 1.705	60	1.0	NA	NA	73	4.5	60	1.0
1.705 ~ 30	69.5	3.0	NA	NA	73	4.5	60	1.0

CLASS B (Residential)								
Frequency (MHz)	FCC Part 15				CISPR 22			
	Quasi-Peak		Average		Quasi-Peak		Average	
	dBuV	mV	dBuV	mV	dBuV	mV	dBuV	mV
0.15 ~ 0.45	NA	NA	NA	NA	66-56.9[1]	2.0-0.7[1]	56-46.9[1]	0.63-0.22[1]
0.45 ~ 0.5	48	0.25	NA	NA	56.9-56[1]	0.7-0.63[1]	46.9-46[1]	0.22-0.2[1]
0.5 ~ 5	48	0.25	NA	NA	56	0.63	46	0.2
5 ~ 30	48	0.25	NA	NA	60	1.0	50	0.32

[1] This is a straight line on the standard dBuV vs. log (*f*) plot.

單位: dBμV

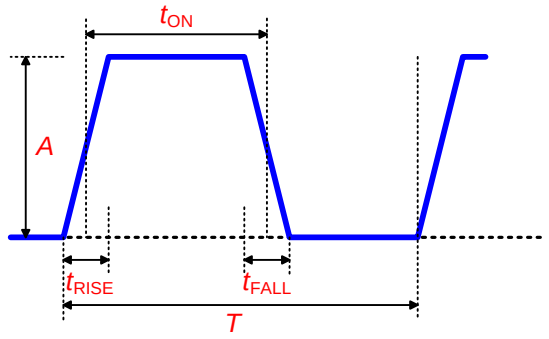
$$dB\mu V = 20 \times \log_{10}\left(\frac{V}{1\,\mu V}\right)$$

120 dBμV = 1 V

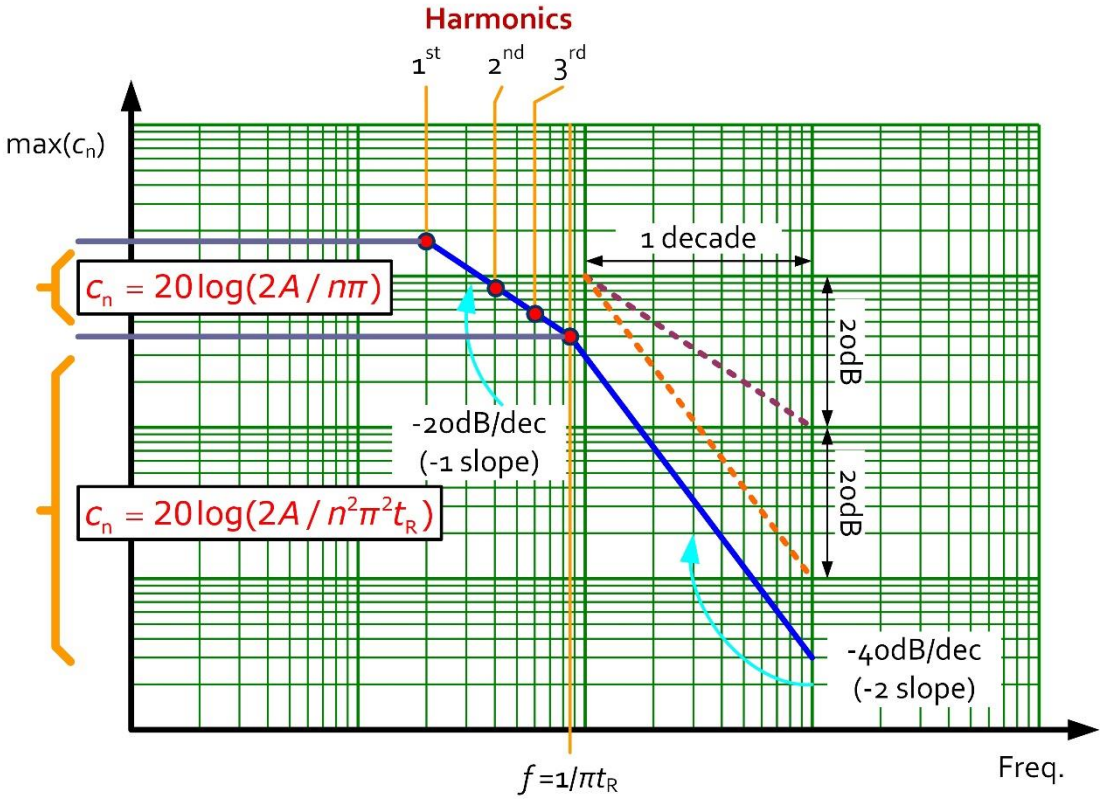
60 dBμV = 1 mV

0 dBμV = 1 μV

週期性方波傅立業級數展開

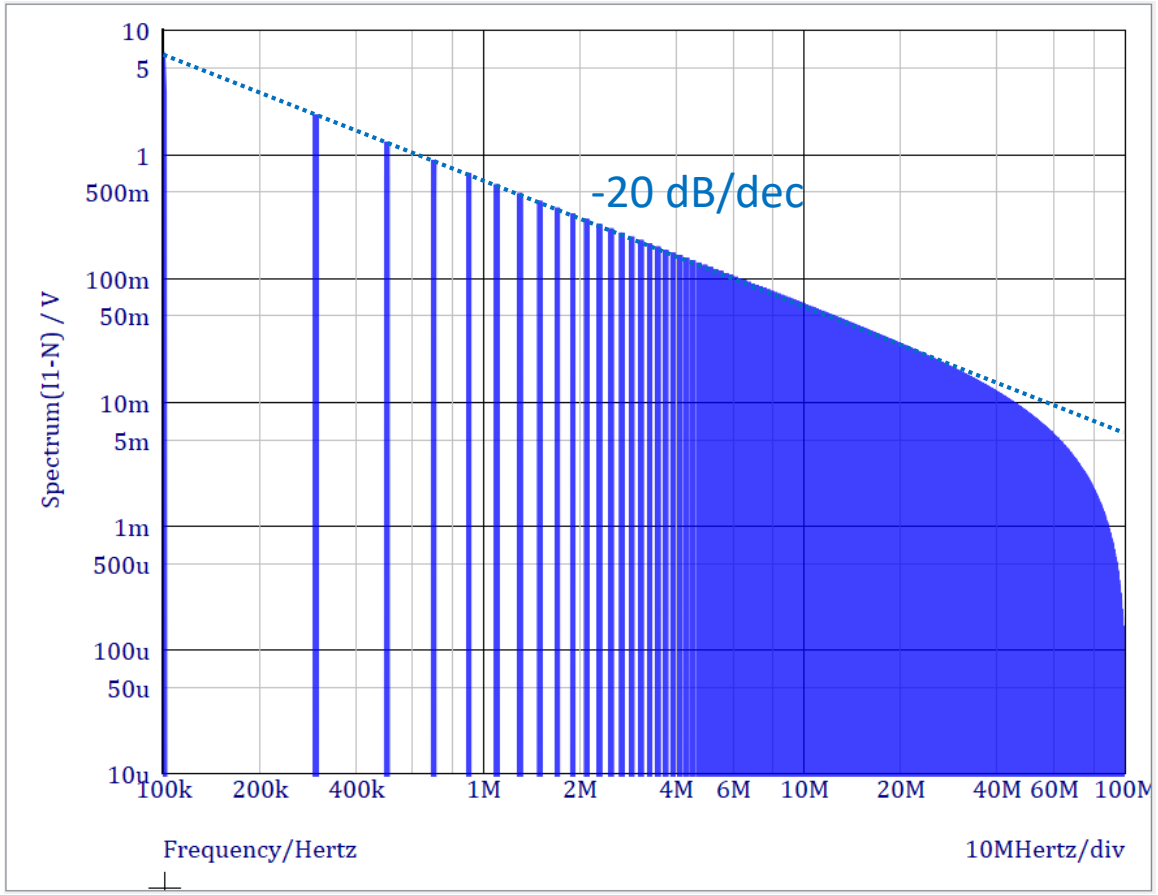


$$f(t) = A\frac{t_{ON}}{T} + 2A\frac{t_{ON}}{T}\sum_{n=1}^{\infty}\left[\frac{\sin\left(\frac{n\pi t_{ON}}{T}\right)}{\frac{n\pi t_{ON}}{T}}\right]\left[\frac{\sin\left(\frac{n\pi t_{R}}{T}\right)}{\frac{n\pi t_{R}}{T}}\right]\cos\left[\frac{2\pi n}{T}t - \frac{\pi n\left(t_{ON}-t_{R}\right)}{T}\right]$$

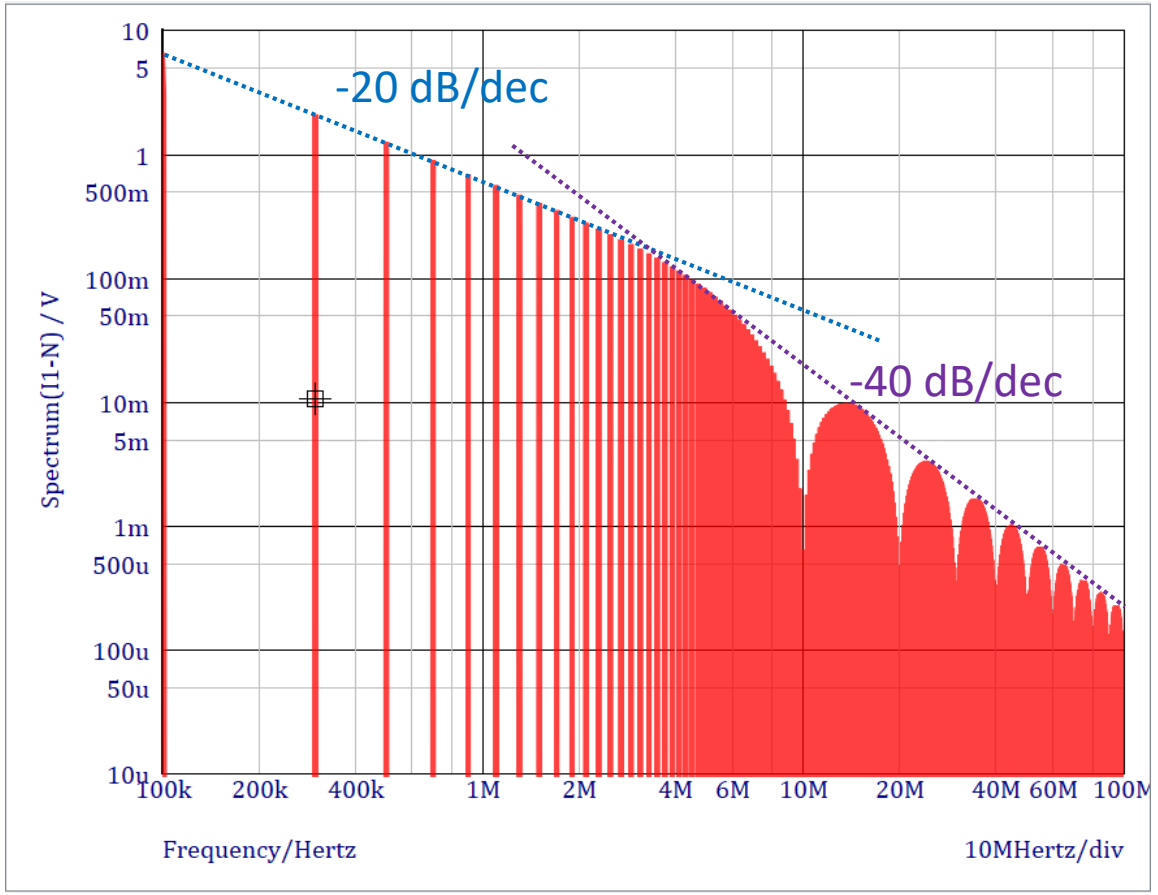


諧波係數： $$c_n = A\cdot\frac{2\cdot t_{ON}}{T}\cdot\left[\frac{\sin\left\{\frac{n\pi\cdot t_{ON}}{T}\right\}}{\frac{n\pi\cdot t_{ON}}{T}}\right]\cdot\left[\frac{\sin\left\{\frac{n\pi\cdot t_{R}}{T}\right\}}{\frac{n\pi\cdot t_{R}}{T}}\right]$$

週期方波頻譜比較



A=10V, T = 10µs, t_{ON} = 4.99µs, $t_R = t_F$ = 10ns

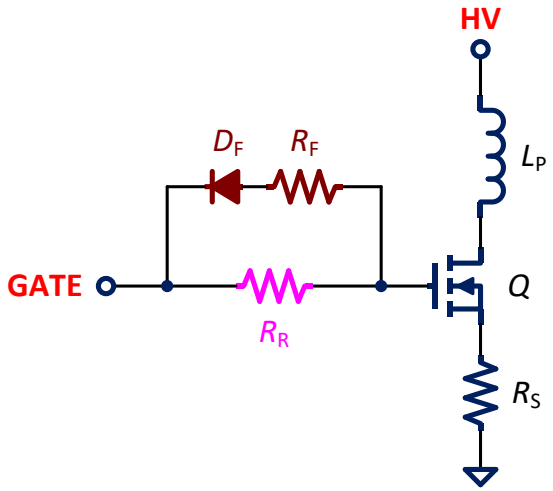


A=10V, T = 10µs, t_{ON} = 4.9µs, $t_R = t_F$ = 100ns

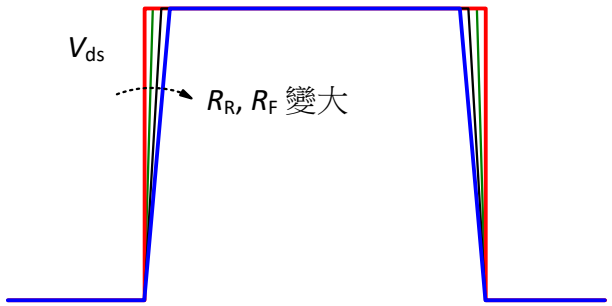
- 上升與下降時間長，則高頻頻譜較低，說明開關晶體閘極驅動快慢將影響雜訊源頻譜。

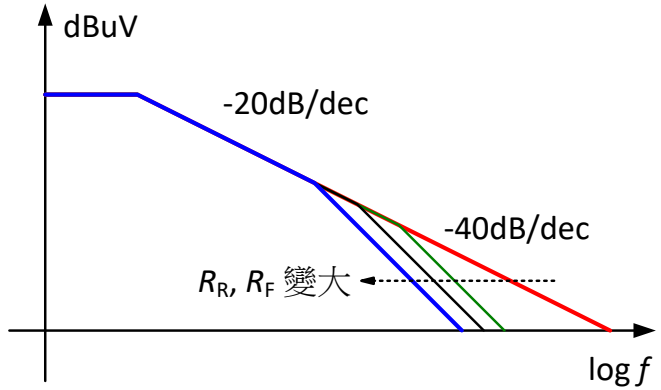
改變雜訊源頻譜

閘極電阻與開關速度

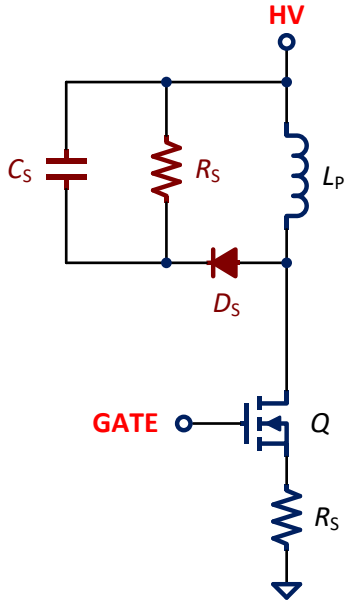


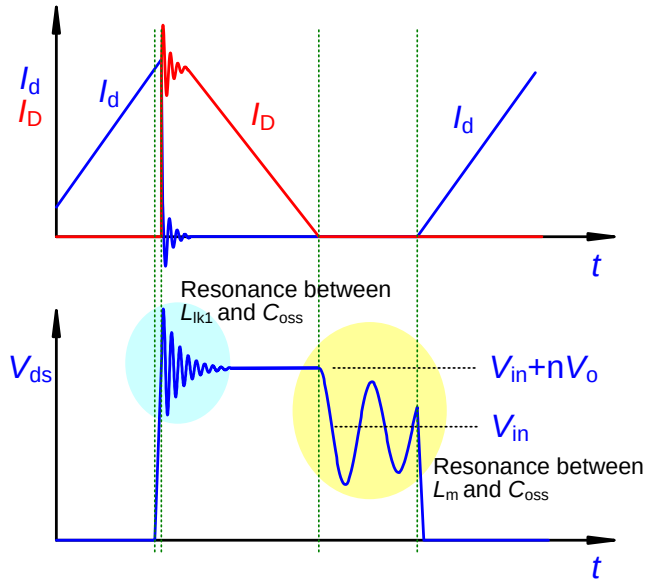
- 閘極電阻值大小，會影響MOSFET 上升與下降速度(τ_r, τ_f)，(R_R主管上升，R_F主管下降) 也就影響了雜訊源的頻譜。
- 速度慢有助於降低雜訊大小，但可能增加了MOSFET 切換損失。





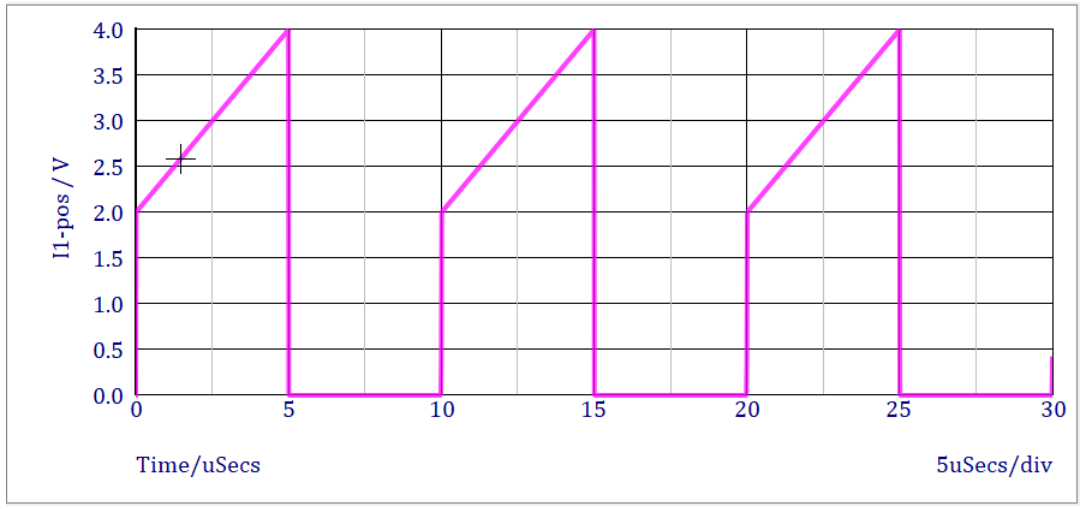
減振吸收(Snubber)電路

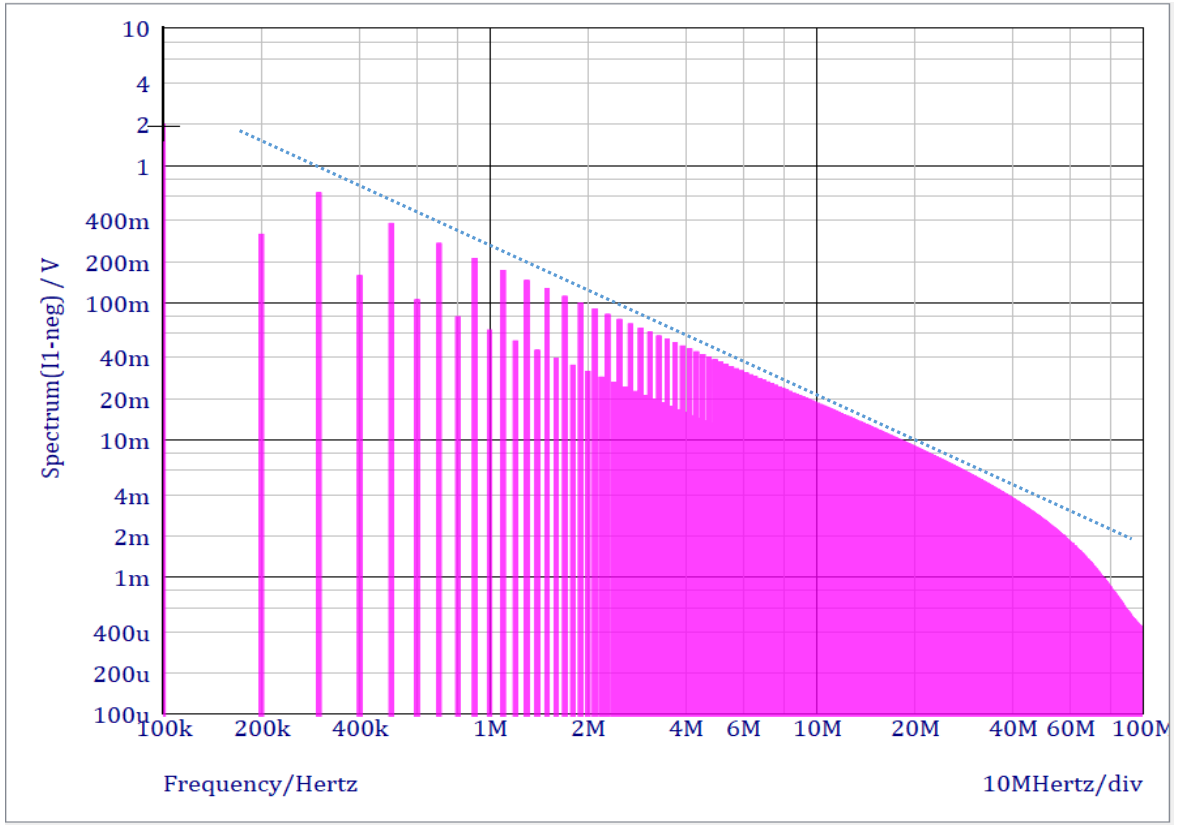




- 減振吸收電路 (D_S, C_S, R_S) 將改變MOSFET關斷時的突波振幅與振盪頻率，進而改變了雜訊頻譜。
- 電壓V_{ds} 波形改變了共模雜訊，電流I_D波形改變了差模雜訊。

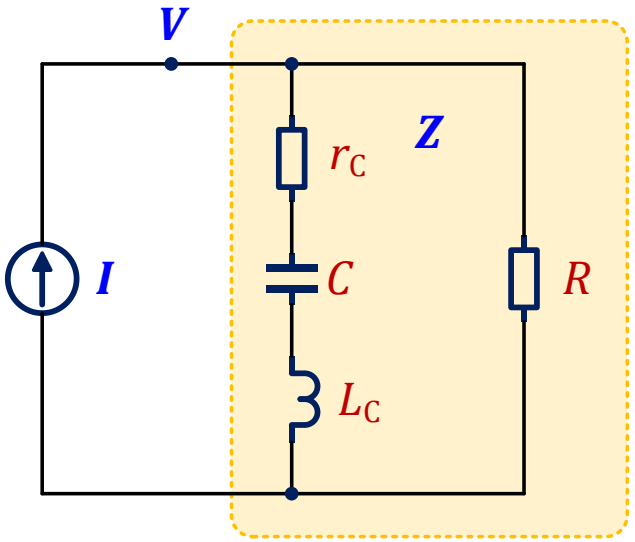
週期梯形波頻譜 (電感電流)





- 梯形電感電流的頻譜包絡線斜率為-20dB/dec.，可視為雜訊電流源的頻譜。
- 梯形電感電流的頻譜與電流大小、漣波、工作週期，甚至上升下降速度有關。
- 大電容 C_B 將提供第一級濾波，將電流雜訊轉換成電壓雜訊。所以 C_B 的阻抗影響 EMI 很大。

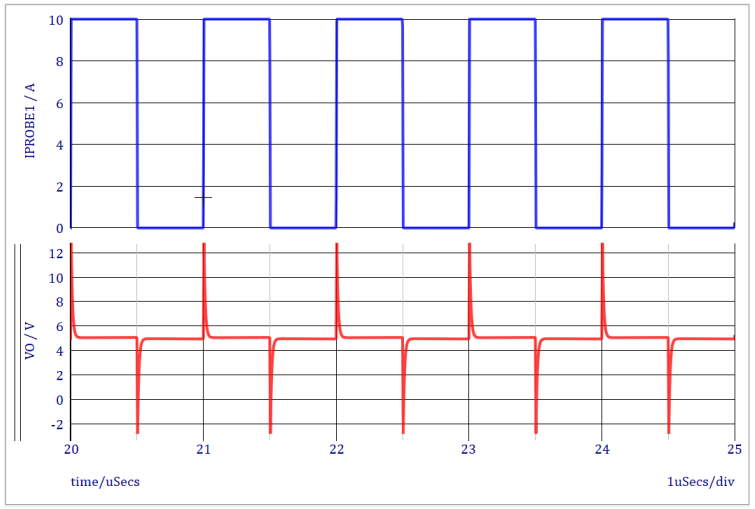
時域響應與頻域頻譜

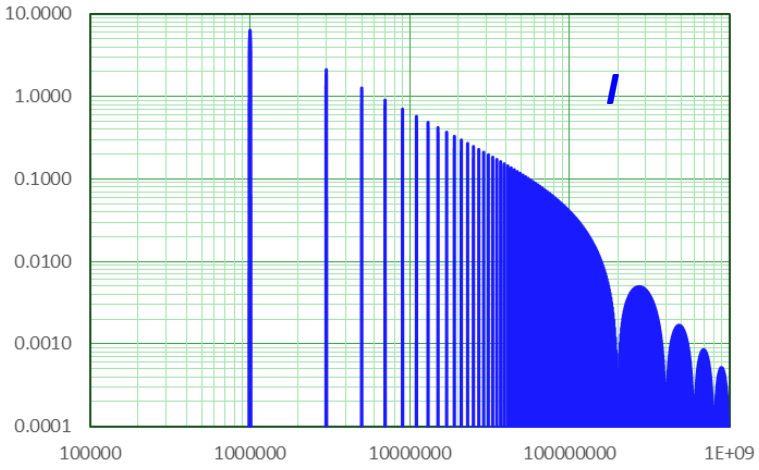


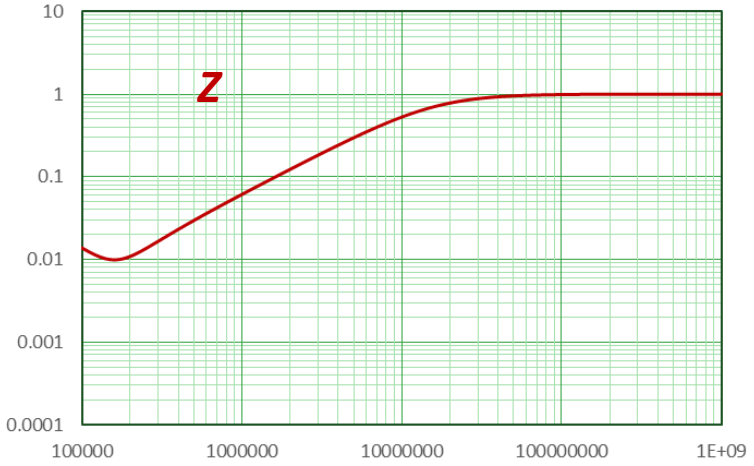
I : Pulse, T_S=1μs, A=10, T_{ON}=0.5μs,
$t_r = t_f$ = 5ns.

C : r_C = 10mΩ, C = 100μF, L_C = 10nH.

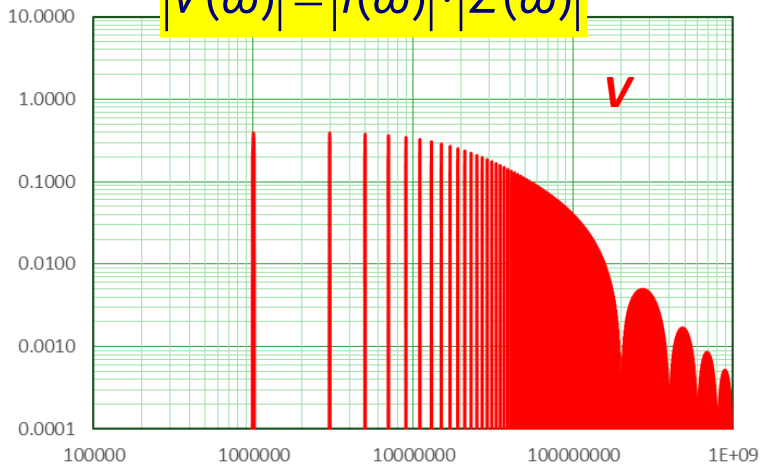
R = 1Ω.



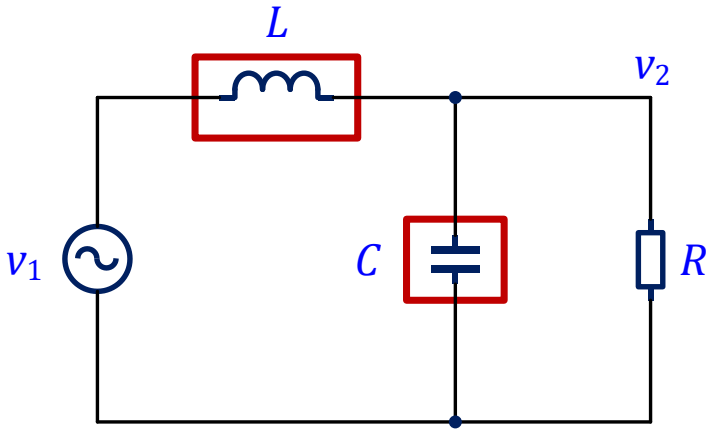




$$|V(\omega)| = |I(\omega)| \cdot |Z(\omega)|$$

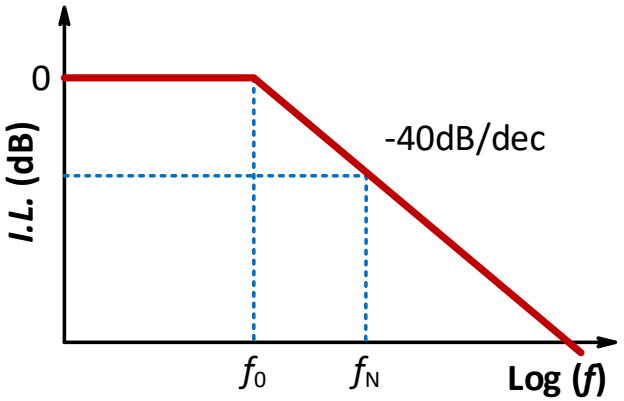


LC 低通濾波器的插入損失

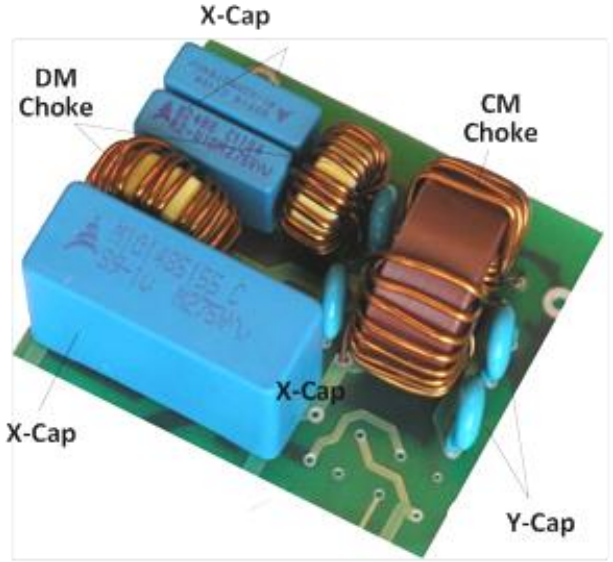


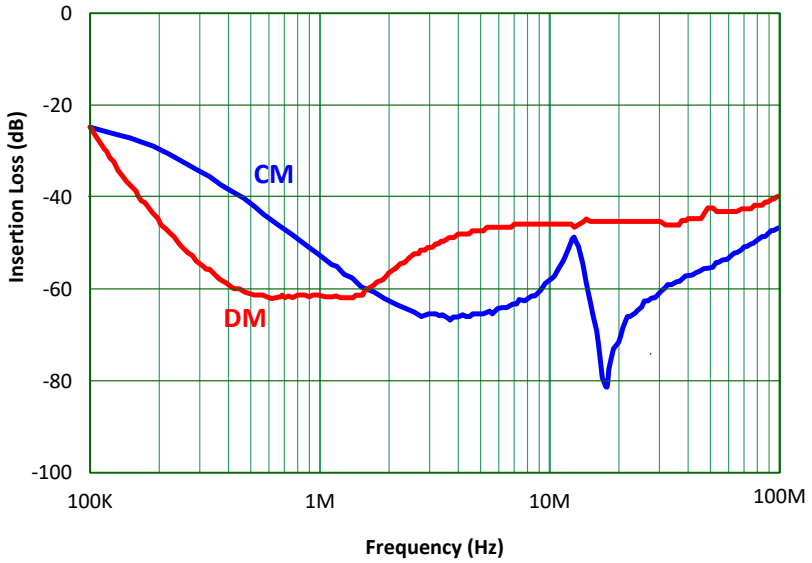
$$\frac{V_2(s)}{V_1(s)} = \frac{R \,//\, \frac{1}{sC}}{sL + \left(R \,//\, \frac{1}{sC}\right)} = \frac{1}{1 + s\frac{L}{R} + s^2 LC}$$

$$I.L.(\text{dB}) = 20 \cdot \log\left|\frac{V_2(j\omega)}{V_1(j\omega)}\right| = -20 \cdot \log\left|1 + j\omega\frac{L}{R} + (j\omega)^2 LC\right|$$

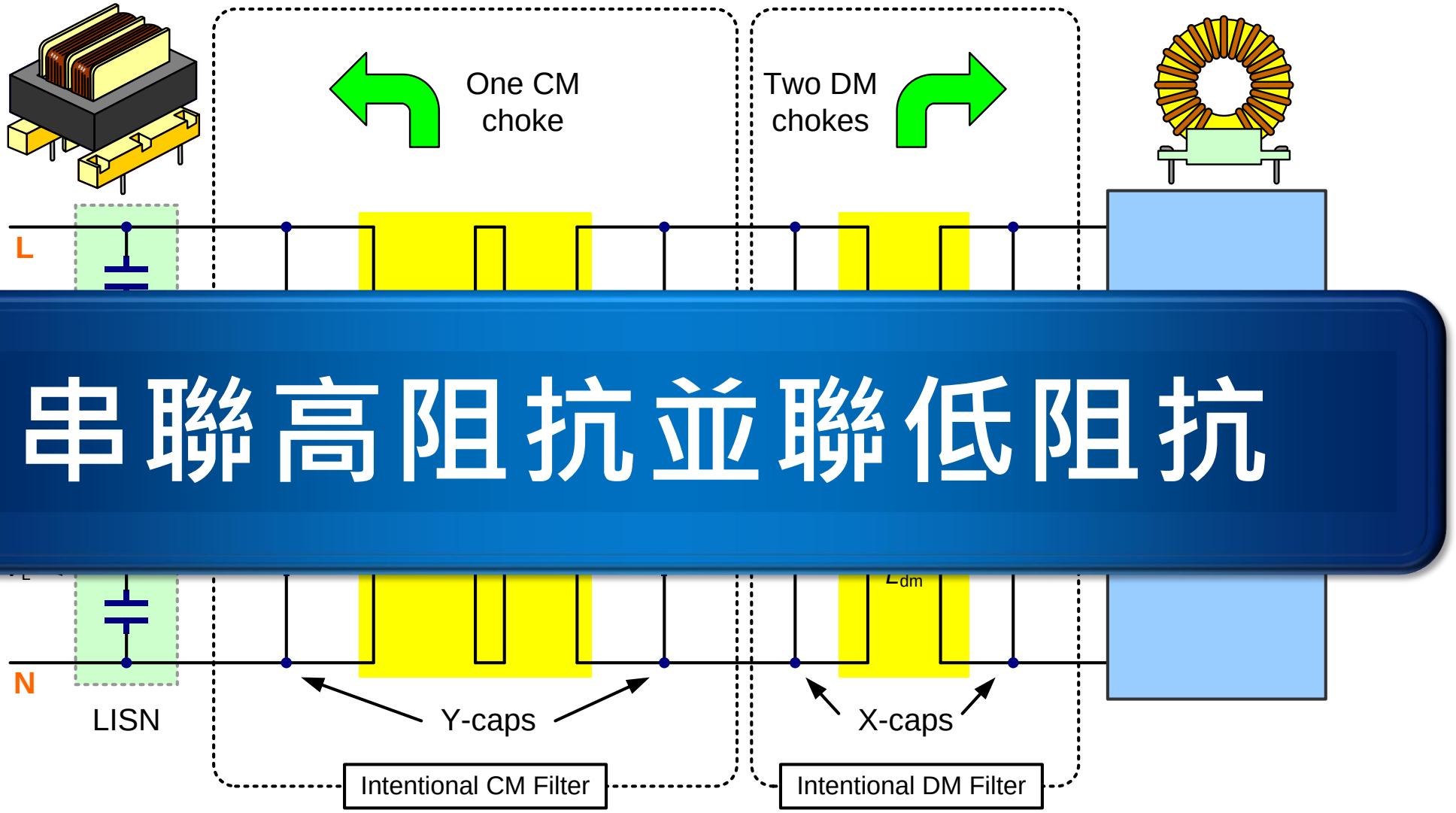


- 電阻 *R* 扮演的角色？





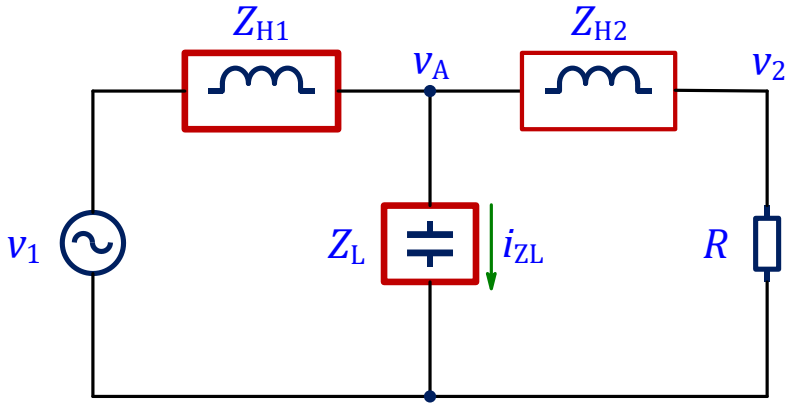
開關電源的差模(DM)與共模(CM)濾波器



串聯高阻抗並聯低阻抗

高階濾波器解耦簡化

T-type filter



$f >> 150kHz$

$Z_{Hn} > 50\Omega$, say 500Ω,

$Z_{Ln} < 50\Omega$, say 5Ω

$$L > \frac{500}{2\pi \cdot 150k} \approx 500\,(\mu H)$$

$$C > \frac{1}{2\pi \cdot 150k \cdot 5} = 0.2\,(\mu F)$$

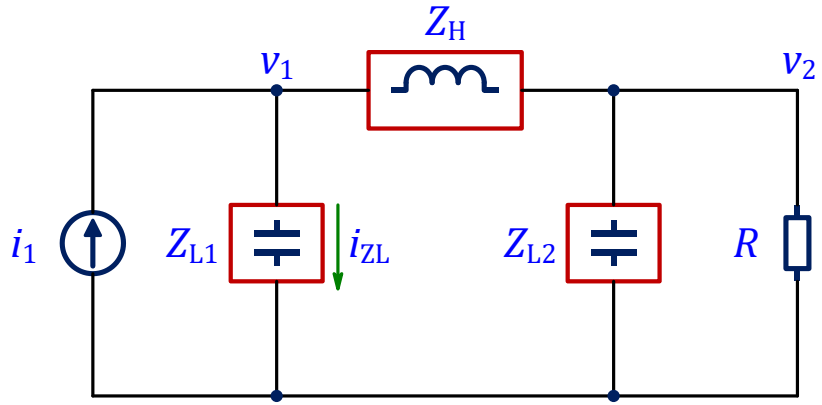
$$v_A \approx \frac{Z_L}{Z_{H1} + Z_L} \cdot v_1 \approx \frac{Z_L}{Z_{H1}} \cdot v_1$$

$$v_2 = v_A \cdot \frac{R}{Z_{H2} + R} \cdot v_1 \approx \frac{Z_L}{Z_{H1}} \cdot \frac{R}{Z_{H2}} v_1$$

$$I.L. \approx 20 \cdot \log \left| \frac{Z_L}{Z_{H1}} \cdot \frac{R}{Z_{H2}} \right| \approx 20 \cdot \log \left| \frac{R}{\omega^3 L_1 L_2 C} \right| dB$$

(< -60 dB @150kHz)

π-type filter



$$v_1 \approx Z_{L1} \cdot i_1$$

$$v_2 = v_1 \cdot \frac{Z_{L2}}{Z_H + Z_{L2}} \approx \frac{Z_{L2}}{Z_H} v_1$$

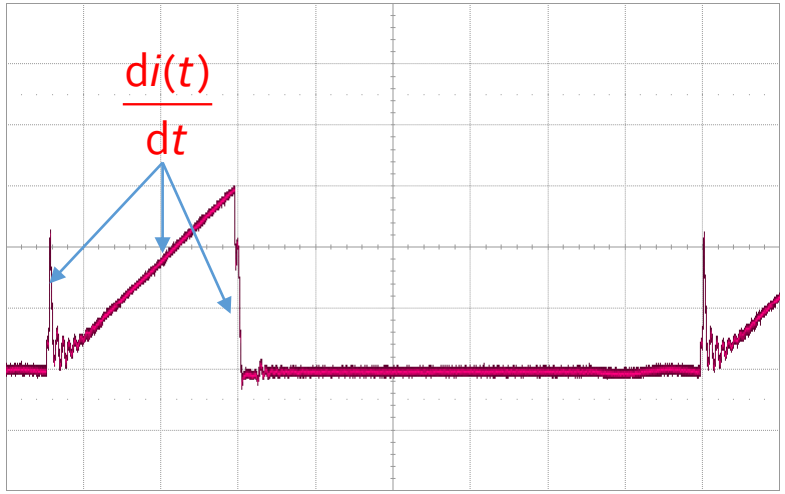
$$i_2 = \frac{v_2}{R} = \frac{Z_{L1} \cdot Z_{L2}}{Z_H \cdot R} \cdot i_1$$

$$I.L. \approx 20 \cdot \log \left| \frac{Z_{L1}}{Z_H} \cdot \frac{Z_{L2}}{R} \right| = 20 \cdot \log \left| \frac{1}{\omega^3 L R C_1 C_2} \right| dB$$

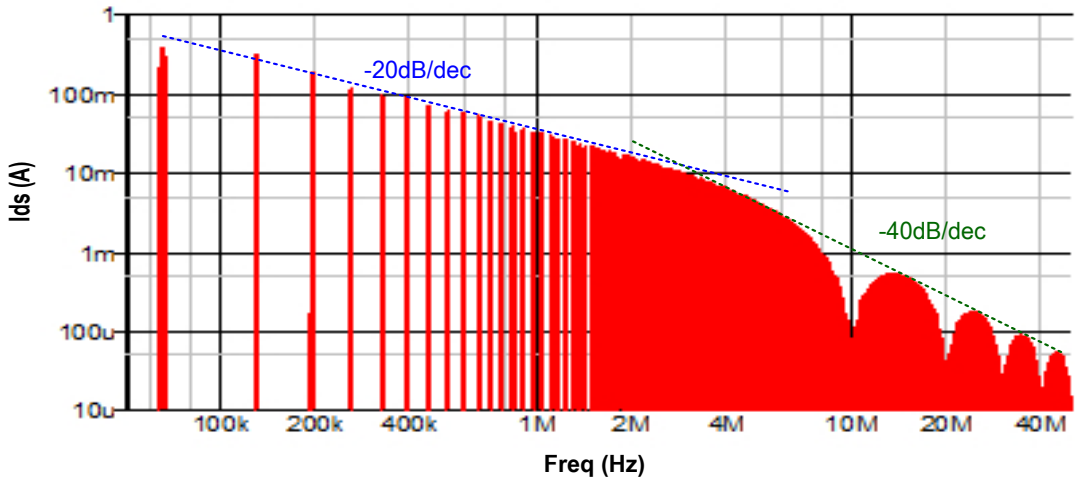
(< -60 dB @150kHz)

雜訊源的頻譜

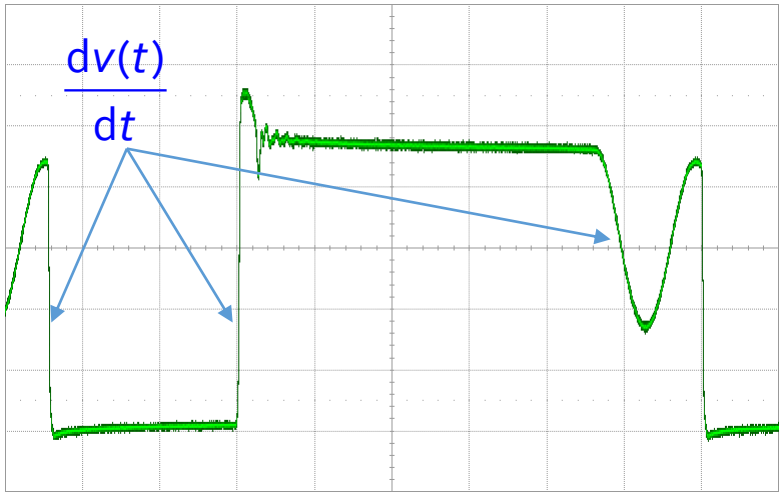
開關電流波形



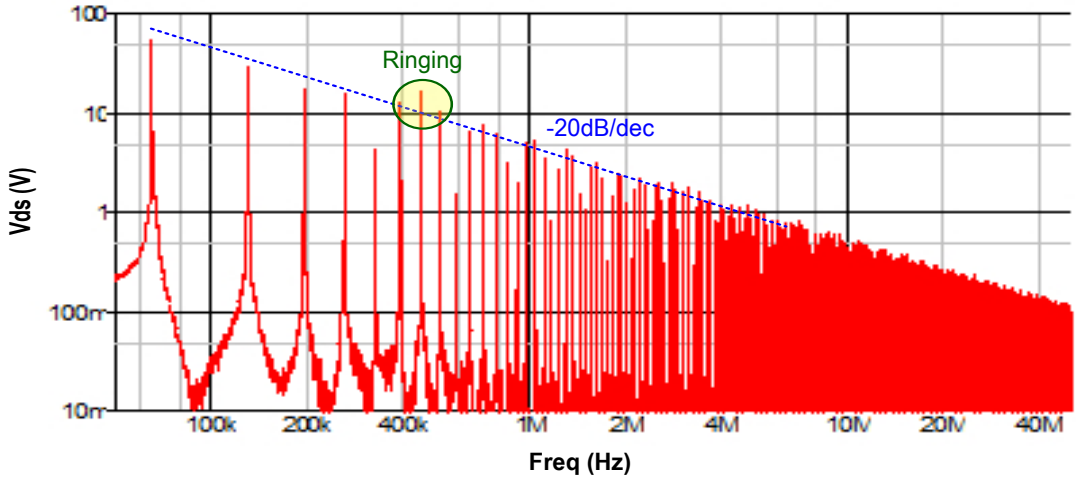
開關電流頻譜



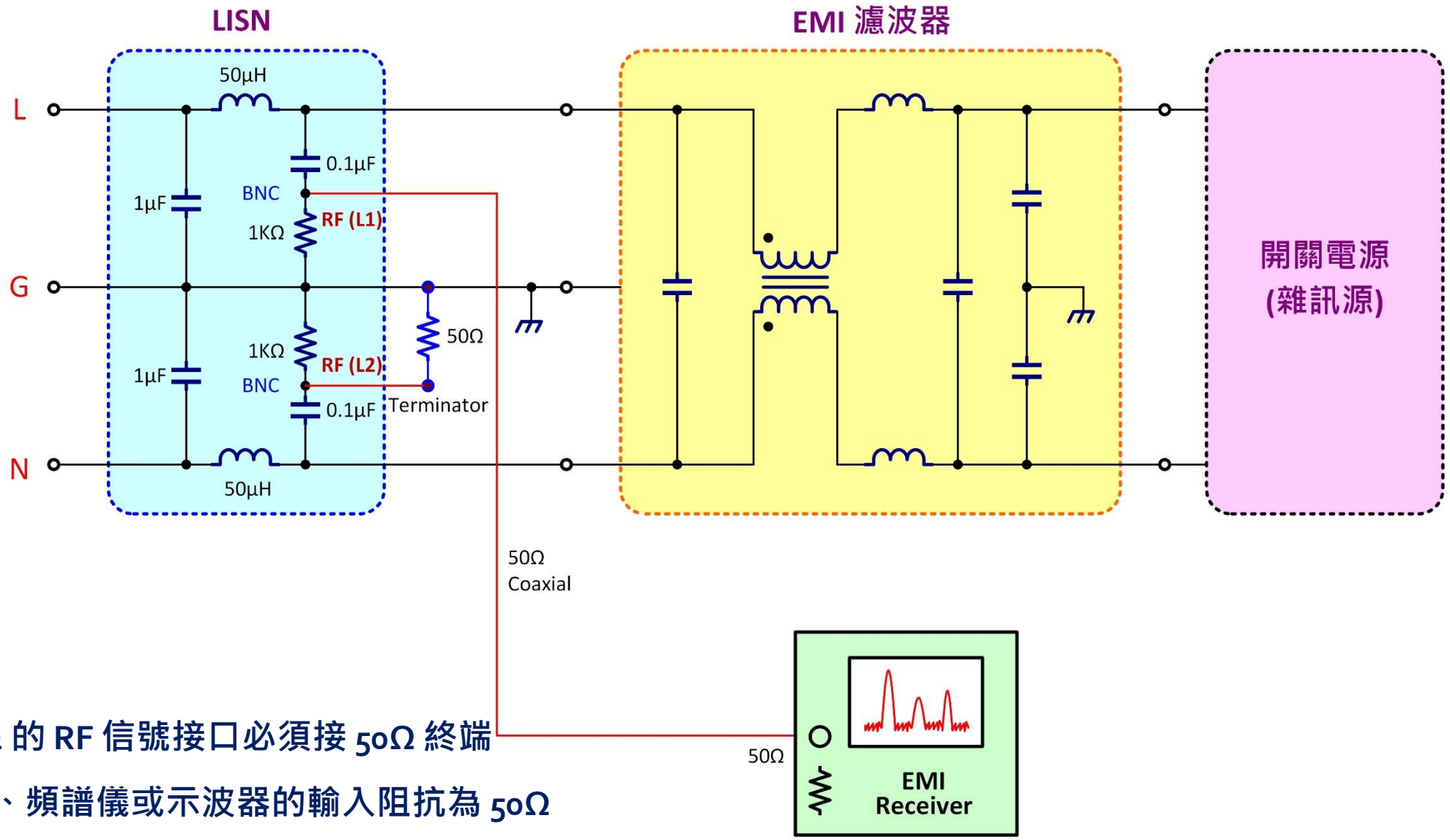
開關電壓波形



開關電壓頻譜

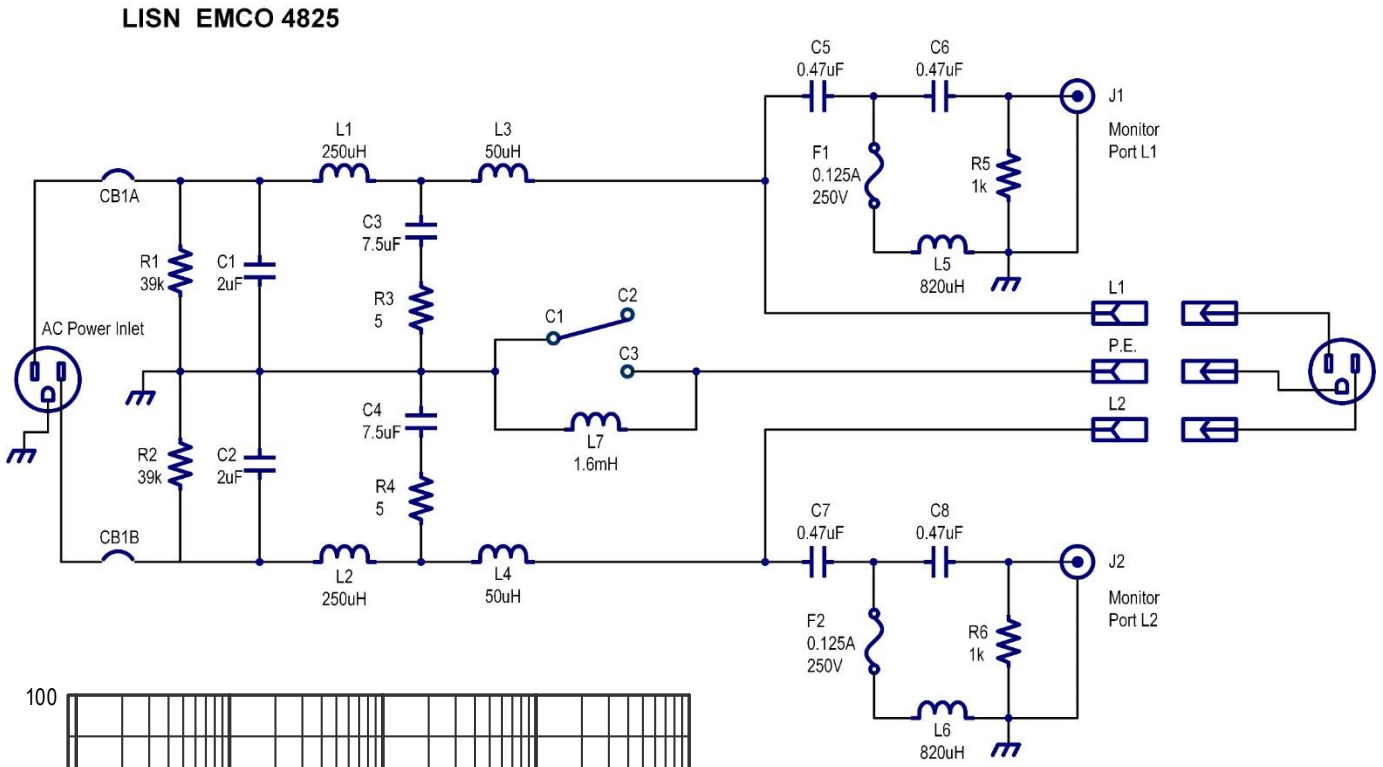


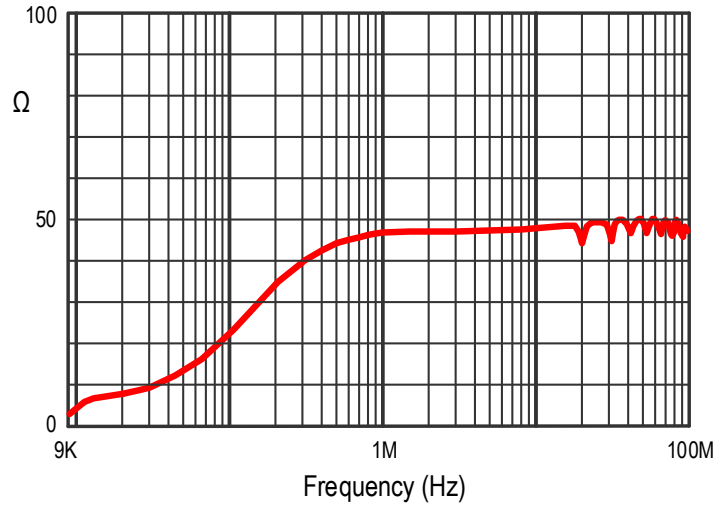
傳導EMI量測接線圖



- L1 量測：L2 的 RF 信號接口必須接 50Ω 終端
- EMI 接收機、頻譜儀或示波器的輸入阻抗為 50Ω

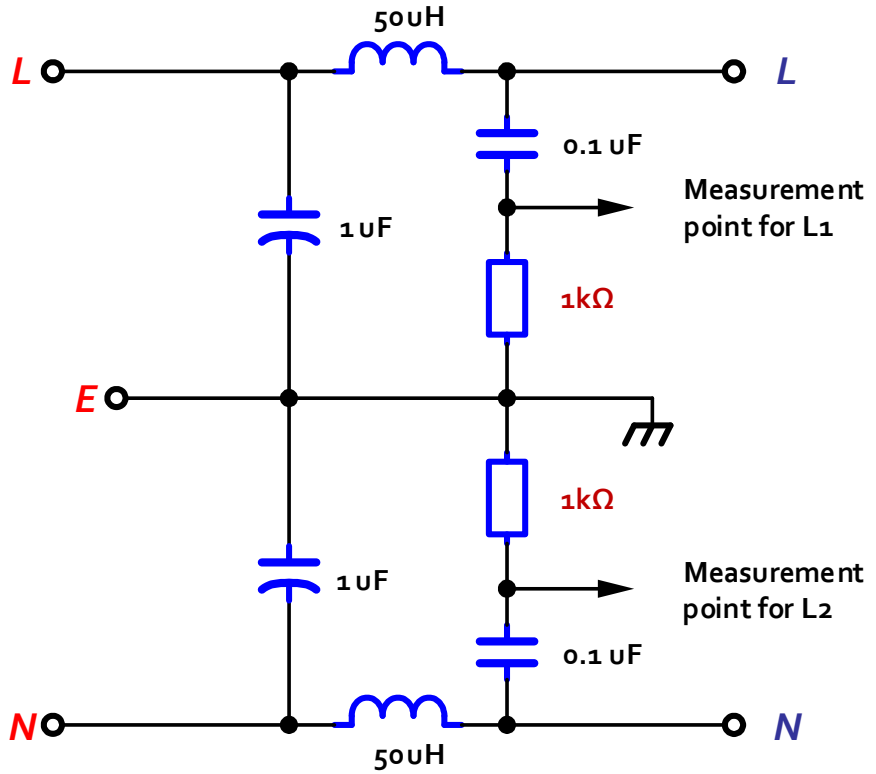
線阻抗穩定網路 (LISN)



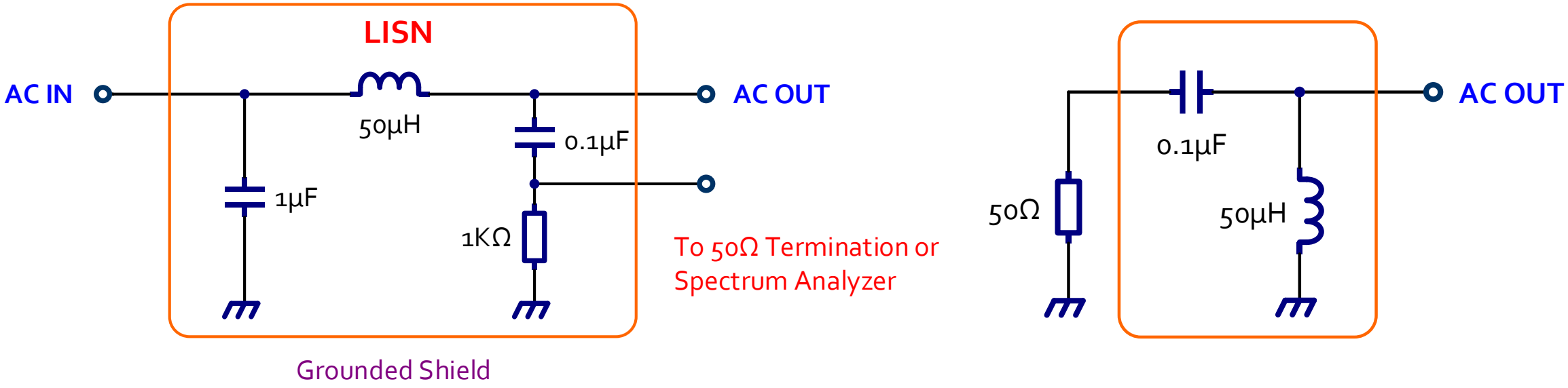


LISN 阻抗圖 (50Ω系統)

LISN 簡化電路



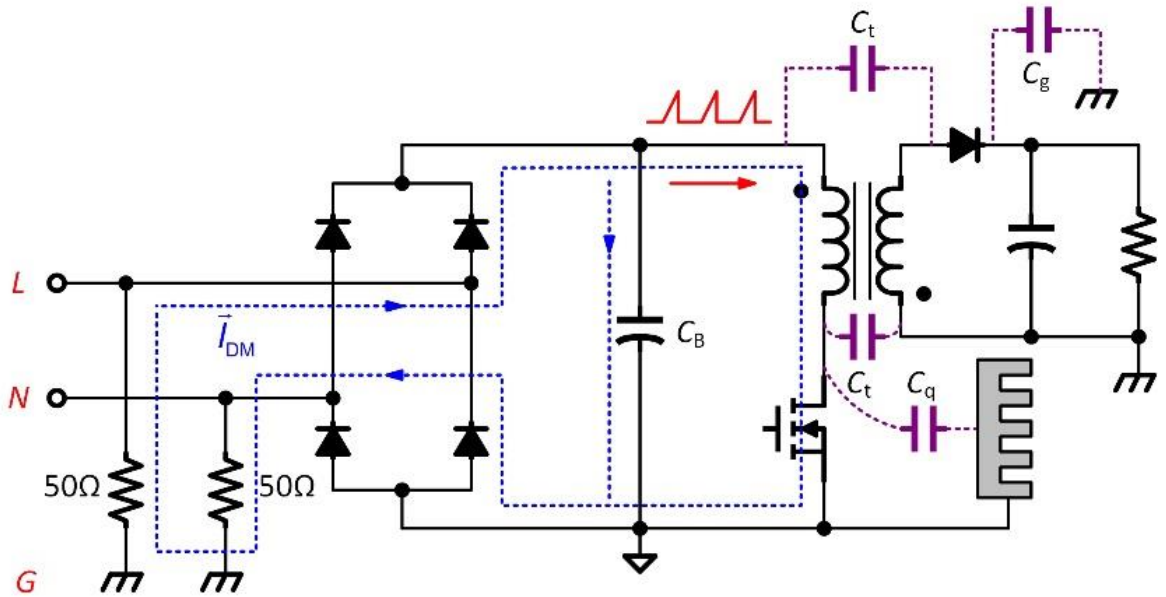
LISN 工作原理



- 對於低頻的運行電流，電感視為低阻抗，電容視為高阻抗。所以LISN的加入，對於電源供應器的正常運轉，沒有改變。
- 對於自電源供應器產生的高頻雜訊，電感視為高阻抗，電容視為低阻抗，所以雜訊大多流到1kΩ電阻與頻譜儀輸入阻抗並聯的等效檢知電阻上。

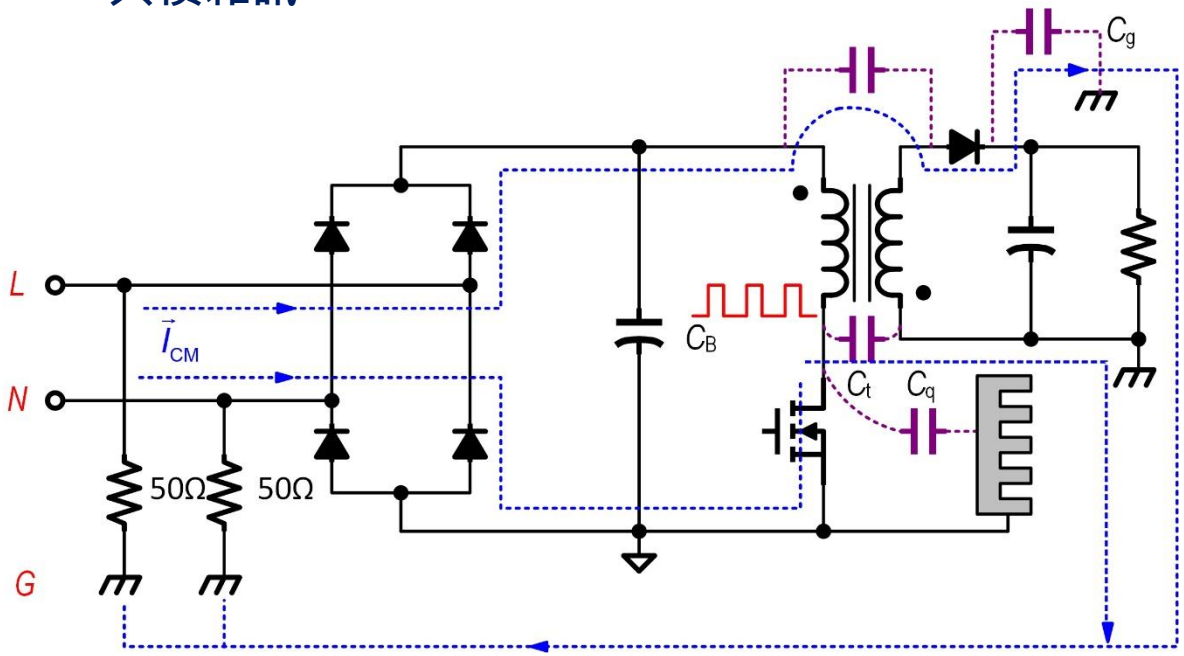
雜訊耦合途逕

差模雜訊



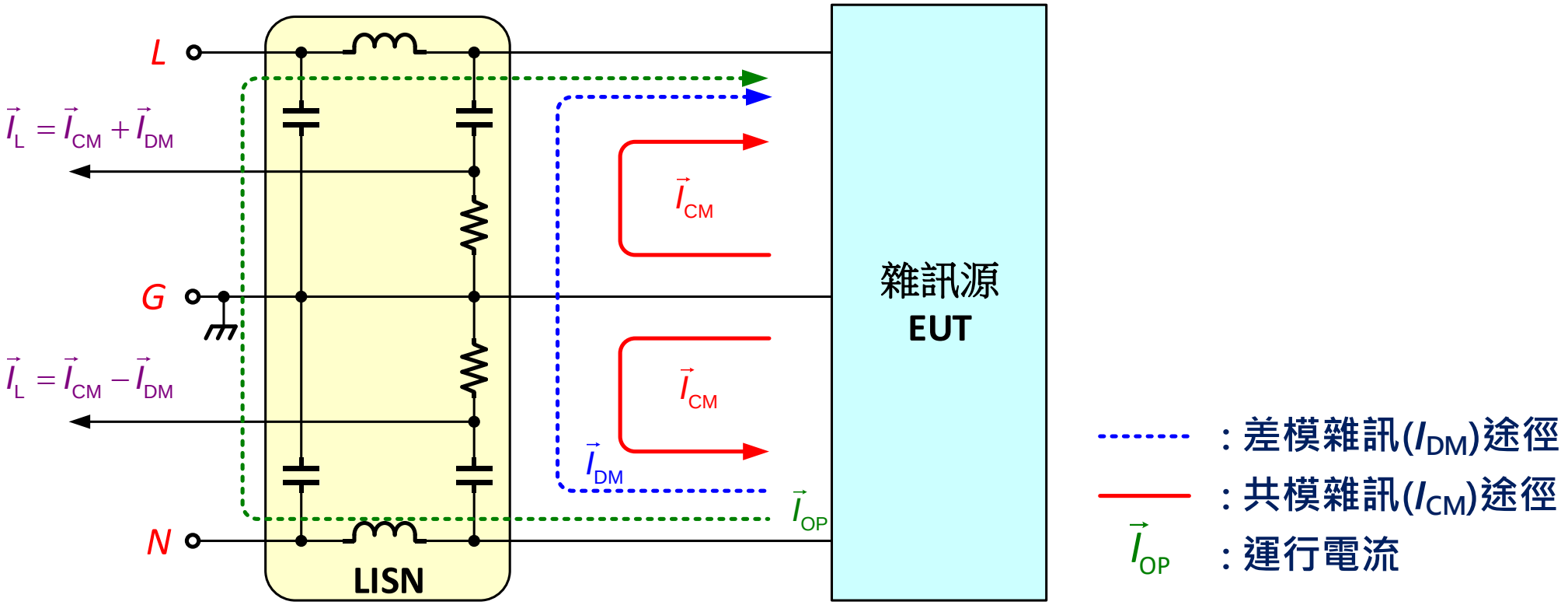
- 以Flyback為例，初級開關電流為脈衝(Pulsating)型式，大電容C_B不僅為橋整濾波用，也是傳導雜訊濾波的第一站。
- 因為電路正常運行而有的脈衝電流，對傳導干擾而言，卻是「雜訊」的最大源頭。

共模雜訊



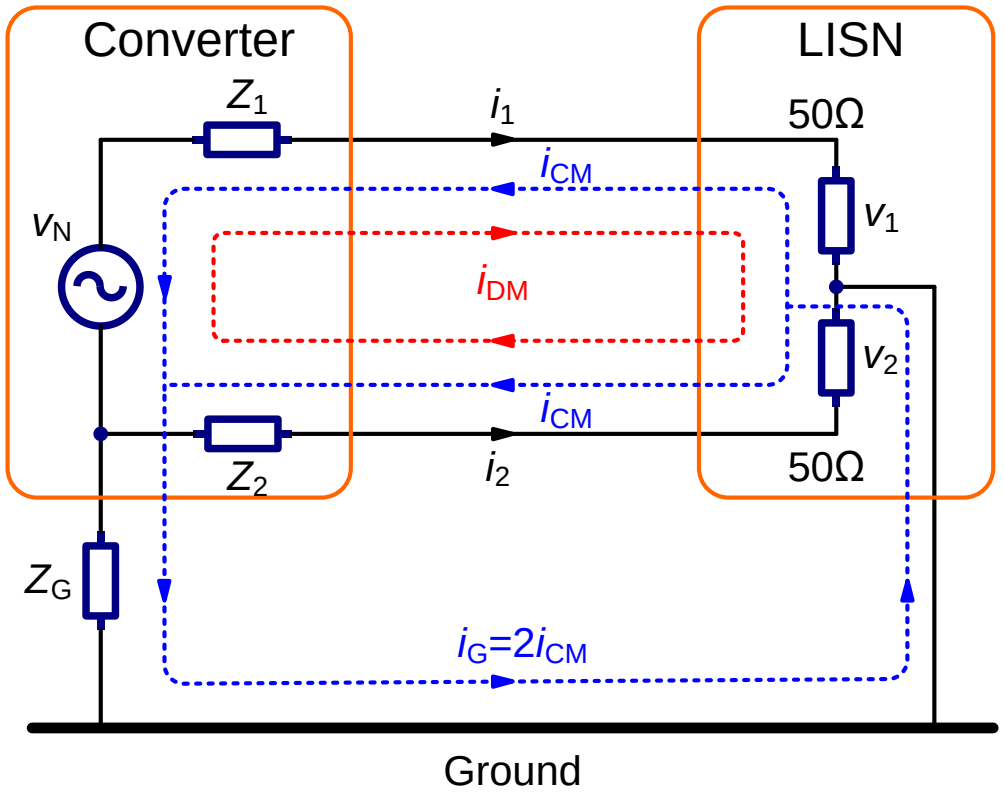
- 共模雜訊必須經由地迴路，多半是因為有電壓陡變(d*v*/d*t*) 的節點與對地雜散電容構成雜訊電流迴路。

LISN與雜訊路徑



- 運行電流：熟知的工作電流，由火線(L) 經電源供應器、負載，再流回中性線(N)。
- 差模雜訊：與運行電流方向一樣(一去一回)，但最後由 LISN 檢知。
- 共模雜訊：藉由地線(G)回流，在L與N線上是大小一樣，相位相同；最後也是由LISN檢知。

DM/CM雜訊分離



$$i_1 = -i_{CM} + i_{DM}$$
$$i_2 = -i_{CM} - i_{DM}$$
$$i_G = 2\,i_{CM}$$

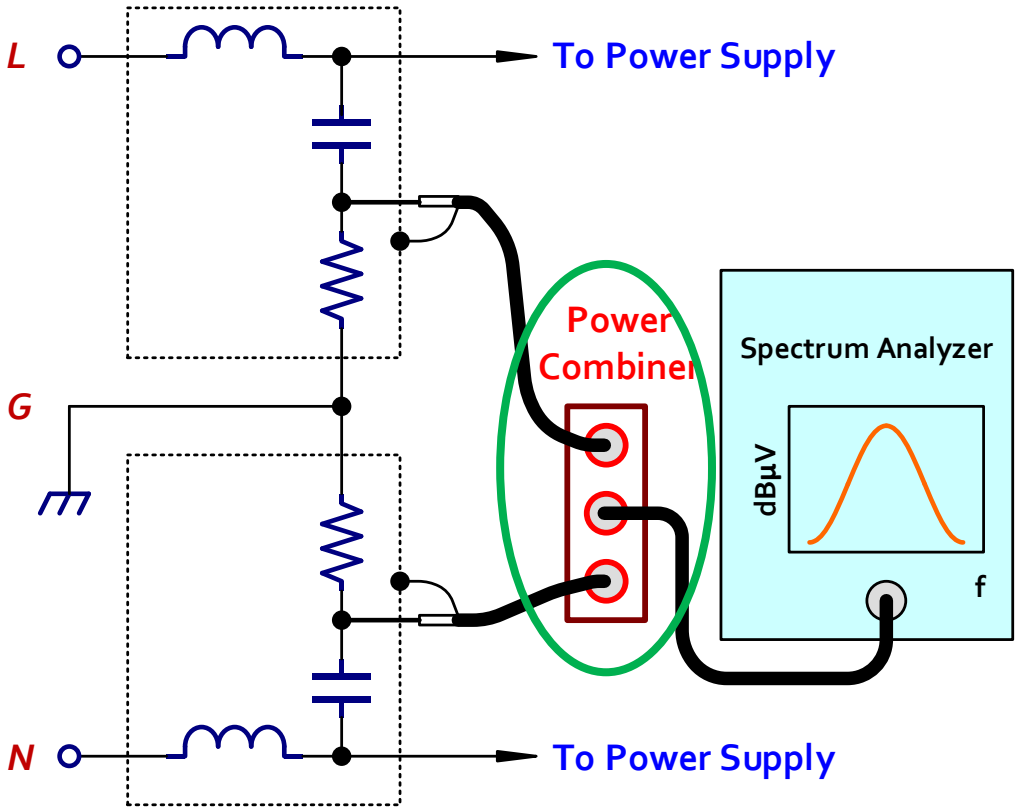
$$v_1 = 50\cdot(-i_{CM} + i_{DM})$$
$$v_2 = 50\cdot(-i_{CM} - i_{DM})$$

$$v_1 = v_{CM} + v_{DM}$$
$$v_2 = v_{CM} - v_{DM}$$

$$v_{CM} = -50 i_{CM} = \frac{v_1 + v_2}{2}$$
$$v_{DM} = 50 i_{DM} = \frac{v_1 - v_2}{2}$$

- v_1 和 v_2 就是法規上要求的 L_1 與 L_2 量測到的雜訊大小。
- 如果能同時量到 v_1 與 v_2，就能夠分別量出共模與差模雜訊。
- 共模雜訊用共模濾波器對策，差模雜訊用差模濾波器解決。

DM/CM 雜訊分離器



EMI Analyzer

EA-2100 EMCIS

Power Splitter / Combiner

180° 0°

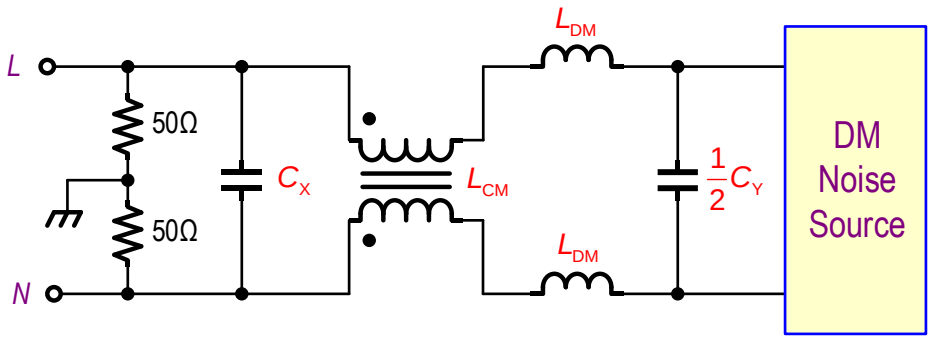
ZSC-2-2 and ZSCJ-2-2 Mini-circuits

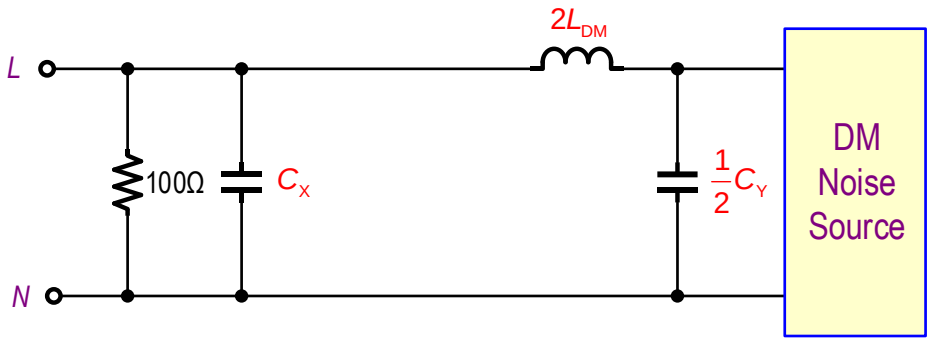
LISN Mate

TBLM1 Tekbox

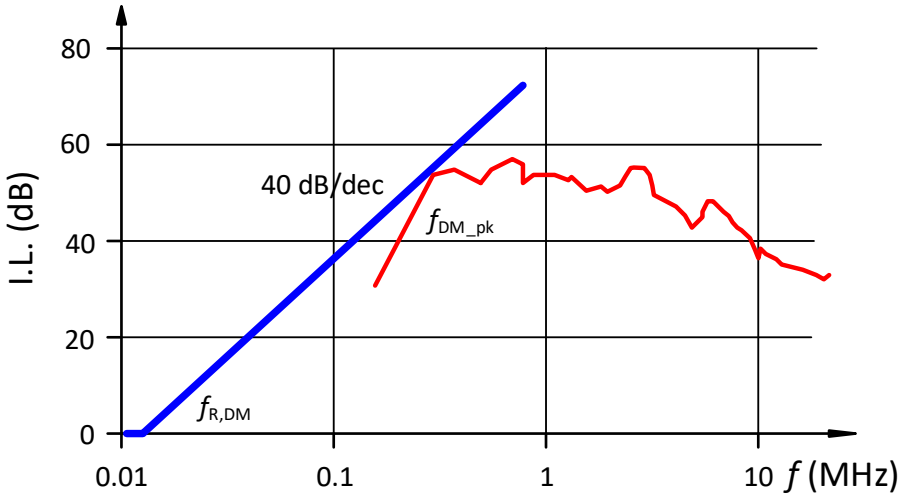
DM 雜訊衰減與簡化濾波器設計

差模等效迴路





$C_{X1} >> C_Y \rightarrow$ $f_{RDM} = \frac{1}{2\pi\sqrt{2L_{DM} \cdot C_X}}$



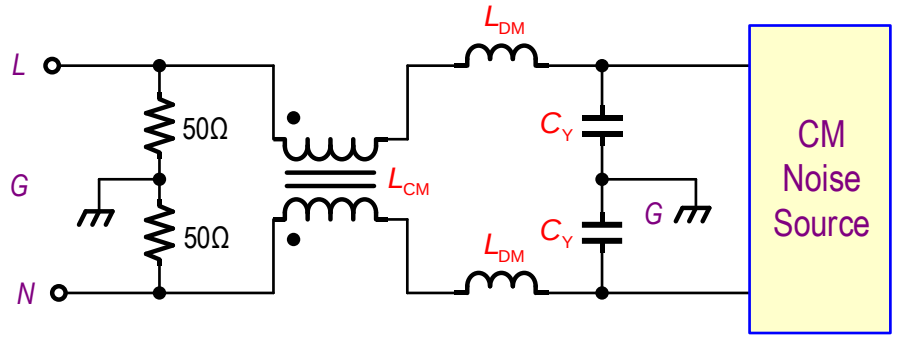
$f_{RDM} = \frac{f_{DM\_pk}}{10^{\frac{I.L.}{40}}}$ (衰減量決定角頻率)

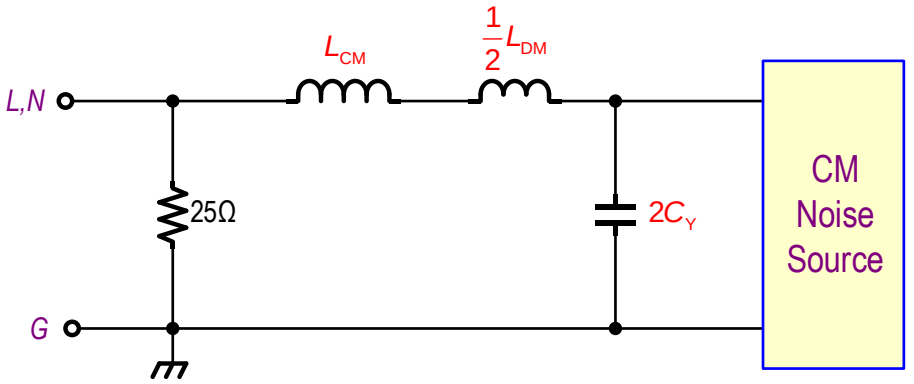
$L_{DM} = \frac{1}{(2\pi \cdot f_{RDM})^2 \cdot C_X}$ (選擇適當X-cap後決定電感值)

特別注意電感飽和問題！

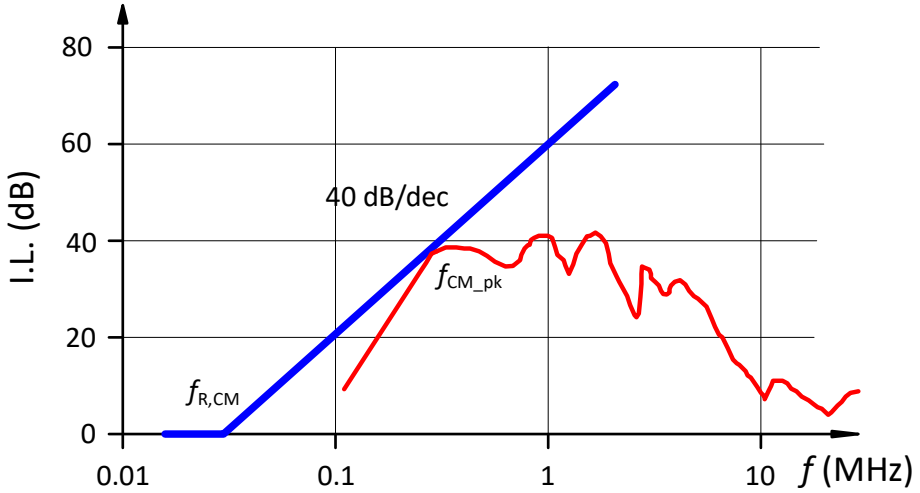
CM 雜訊衰減與簡化濾波器設計

共模等效迴路





$L_{CM} >> L_{DM} \rightarrow \quad f_{RCM} = \dfrac{1}{2\pi\sqrt{L_{CM} \cdot 2C_Y}}$



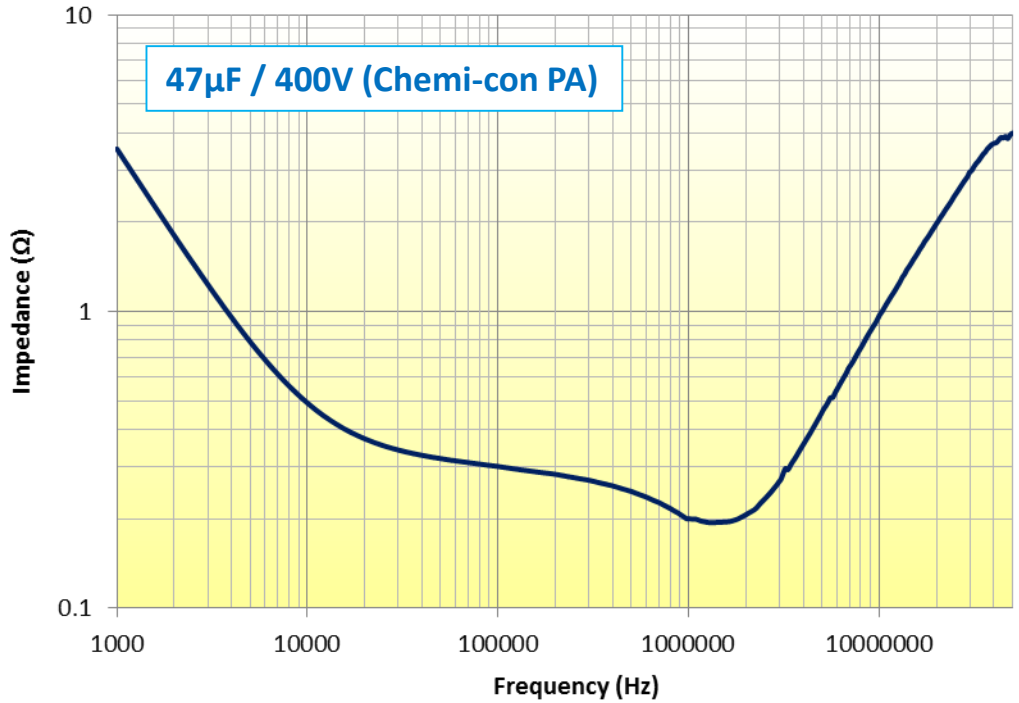
$$f_{CM\_filter} = \frac{f_{CM\_pk}}{10^{\frac{I.L.}{40}}} \quad \text{(衰減量決定角頻率)}$$

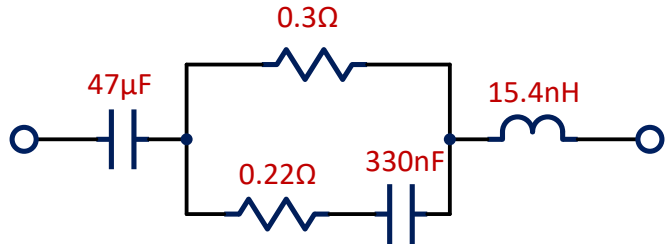
$$C_Y = \frac{I_{Leak}}{2\pi \cdot f_L \cdot V_{in}} \quad \text{(安規漏電流限制)}$$

$$L_{CM} = \frac{1}{(2\pi \cdot f_{CM\_filter})^2 \cdot C_Y}$$

特別注意鐵芯材質與繞製 方法!

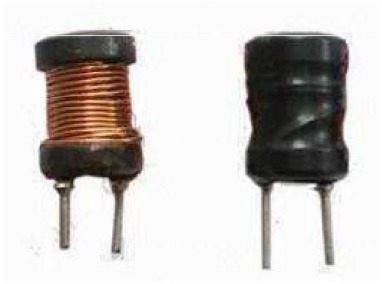
電解電容高頻特性





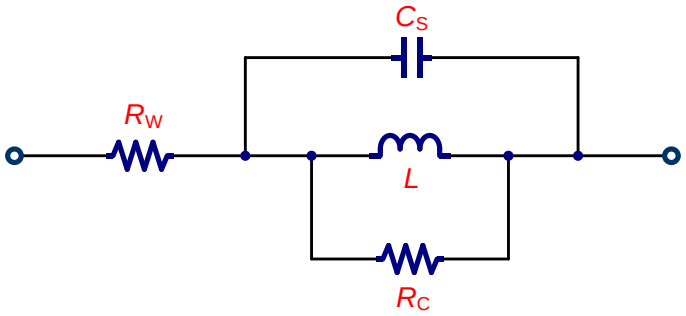
- 接於橋式整流器後方儲能濾波用
- 與Hold-up 時間最相關
- 低阻抗(ESR)用以抑制差模雜訊

差模電感 (Differential-mode Choke)

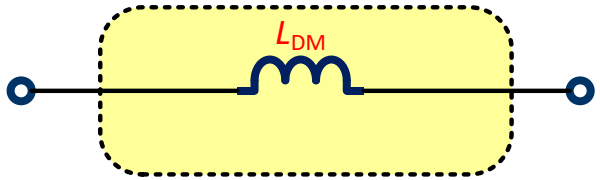


DM 電感 (T68 Sendust)

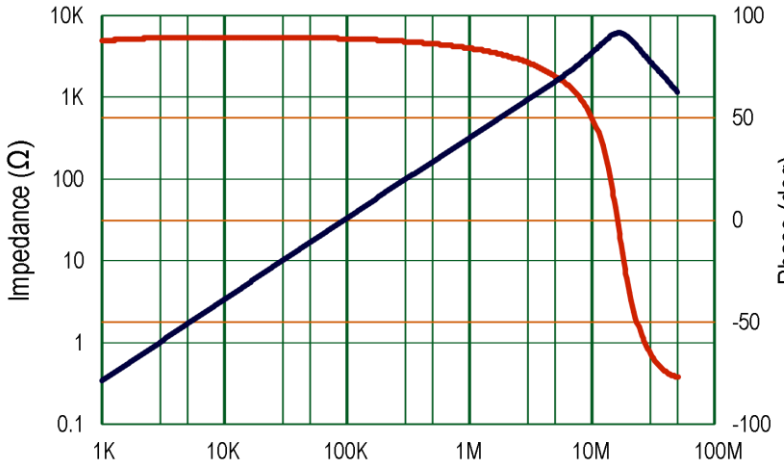
55uH 環型電感

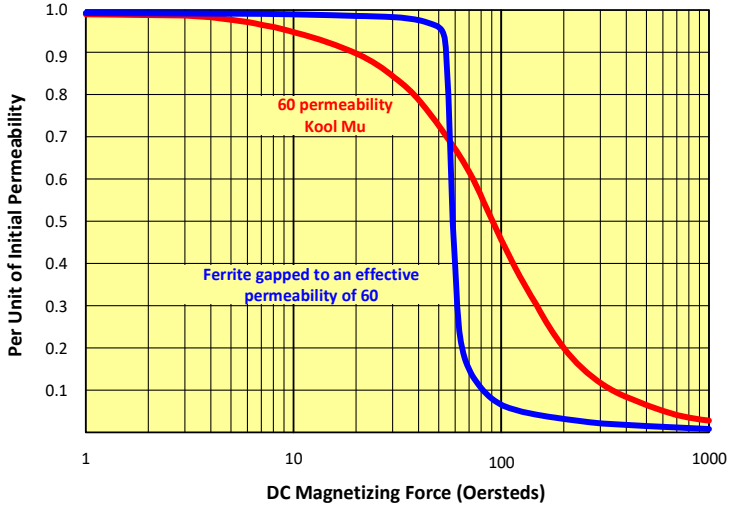


L	R_C	R_W	C_S
53.3uH	6.13KΩ	10mΩ	18.1pF

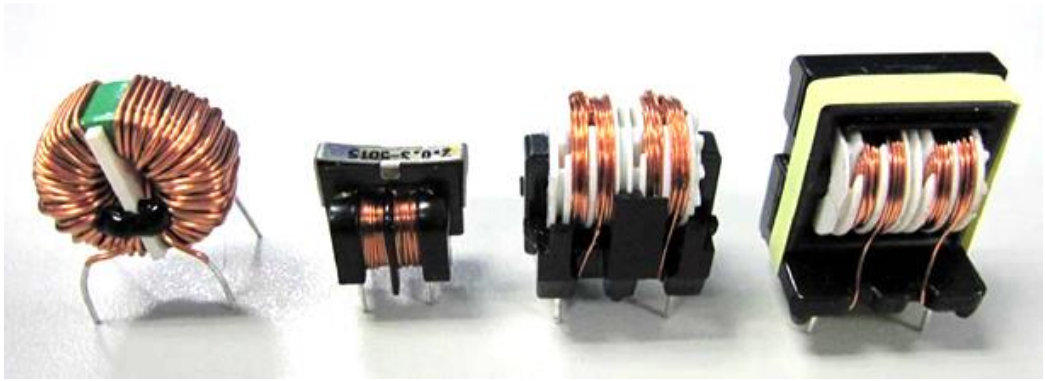


- 串接於 L 或 N
- 鐵粉芯或氣隙鐵氧體
- 差模電感流過負載電流，必須確定飽和與否

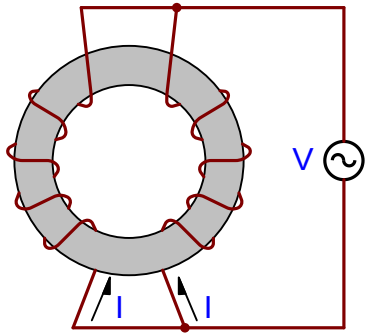




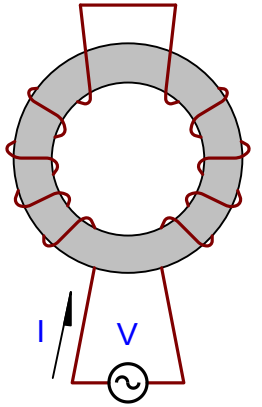
共模電感 (Common-mode Choke)

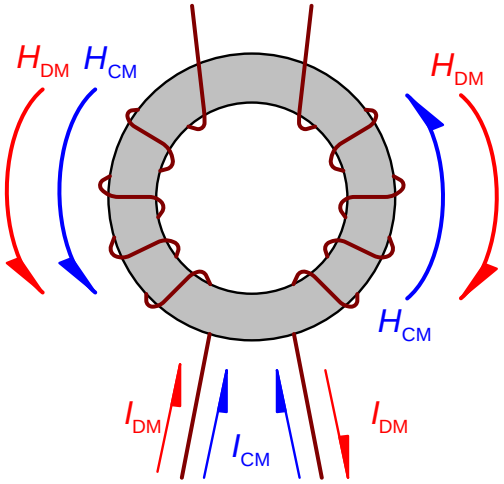


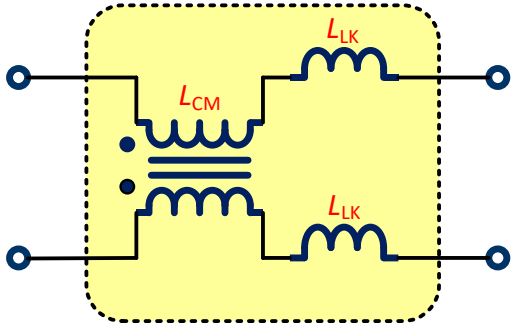
共模感值量測

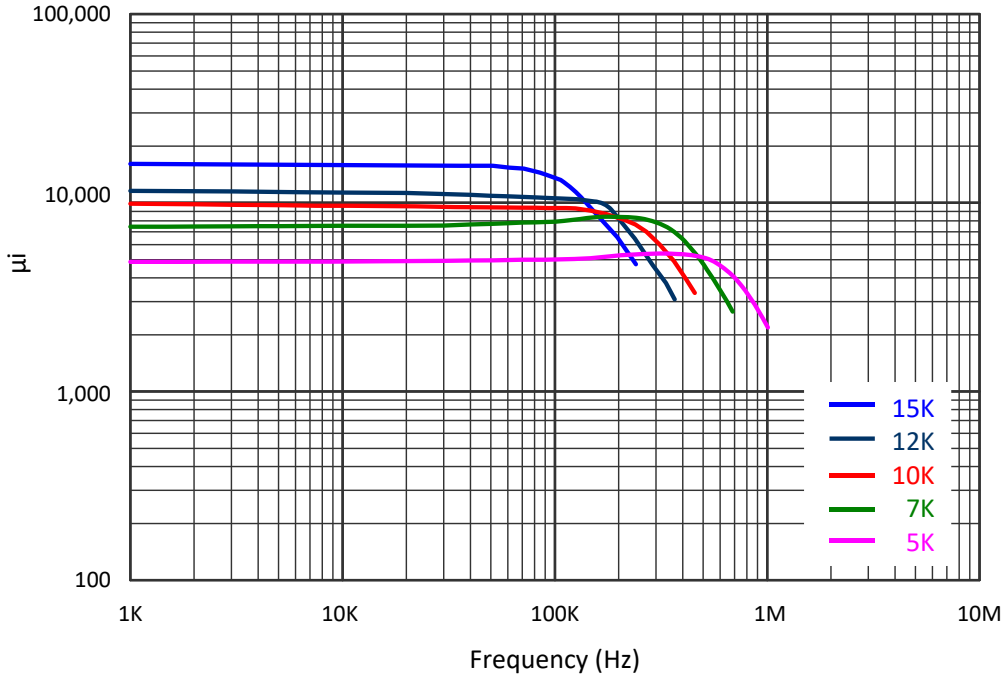


差模感值量測



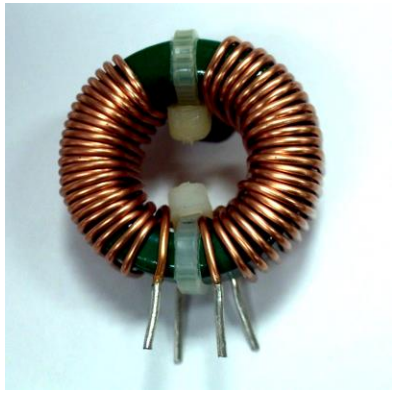




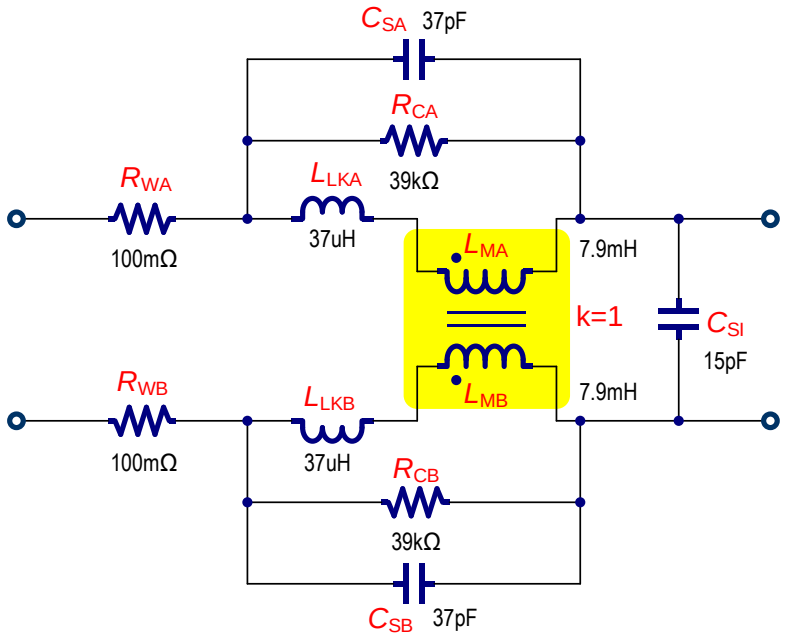


- CM Choke 差模部份的磁通相互抵消，沒有飽和問題
- 漏電感部份形成差模電感，大電流下依然有飽和問題

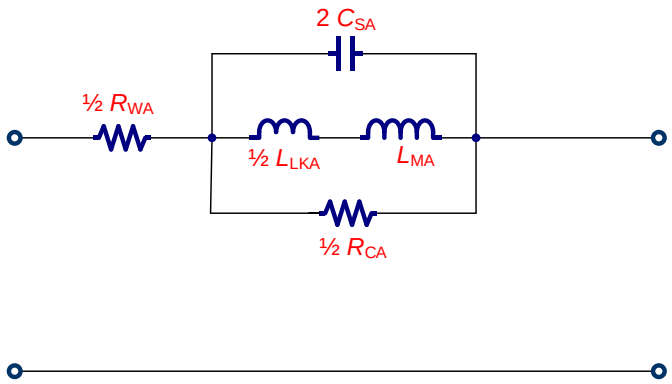
共模電感的參數萃取

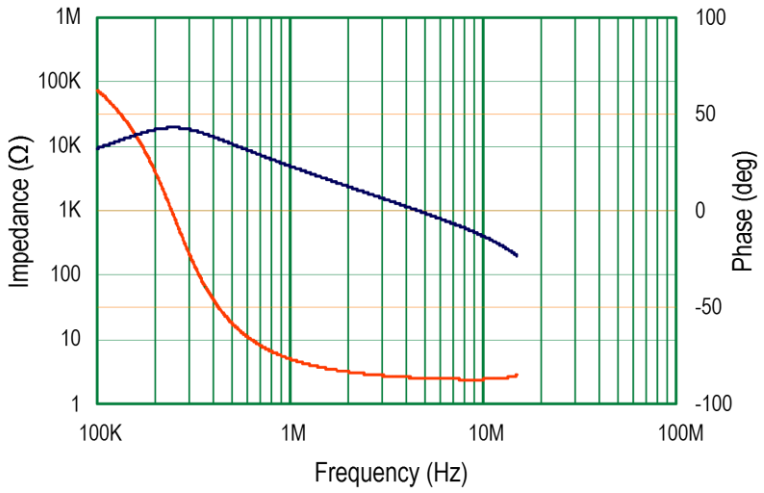


T18 共模電感等效電路

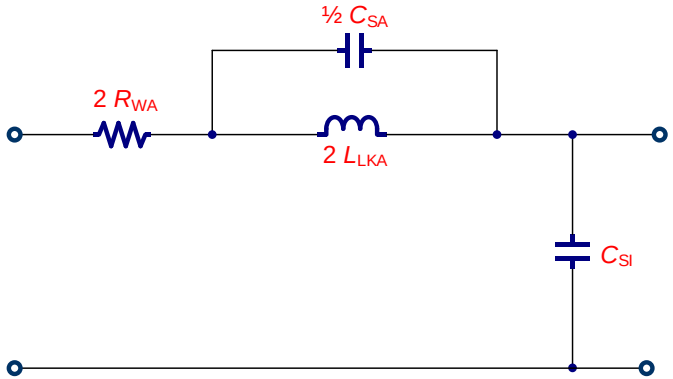


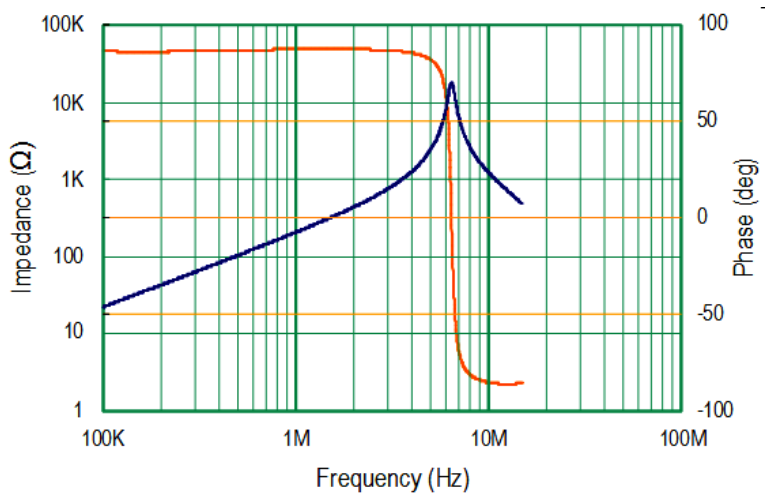
共模參數模型





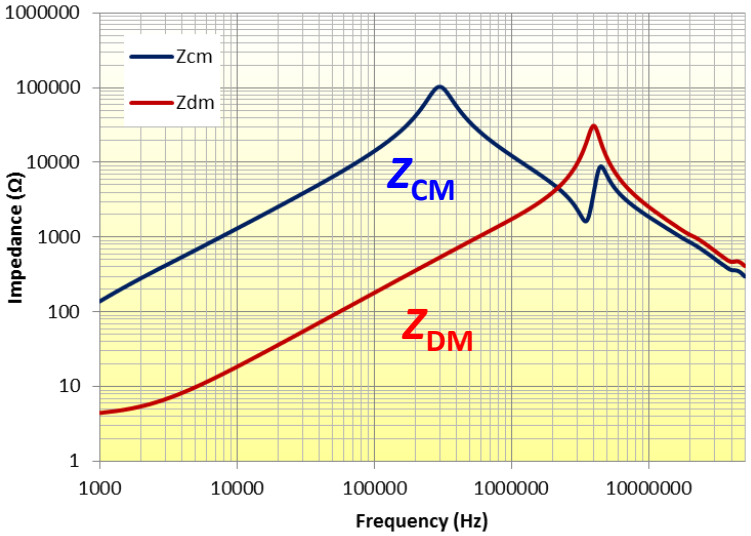
差模參數模型





鐵芯與繞製

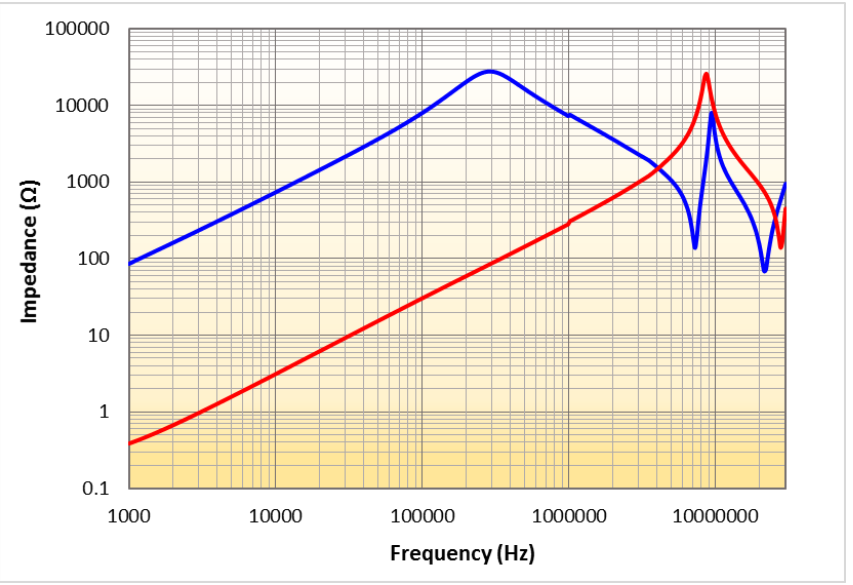
CM電感 (UU9.8)



L_{CM} = 22.2 mH, L_{DM} = 285 µH @ 1V/100kHz

$$\frac{L_{DM}}{L_{CM}} = \frac{285\mu}{22.2m} = 1.28\%$$

CM電感 (T14)

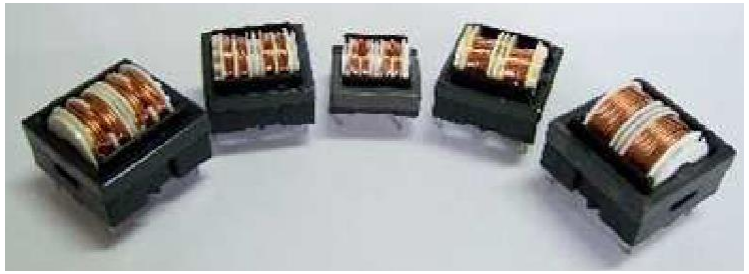


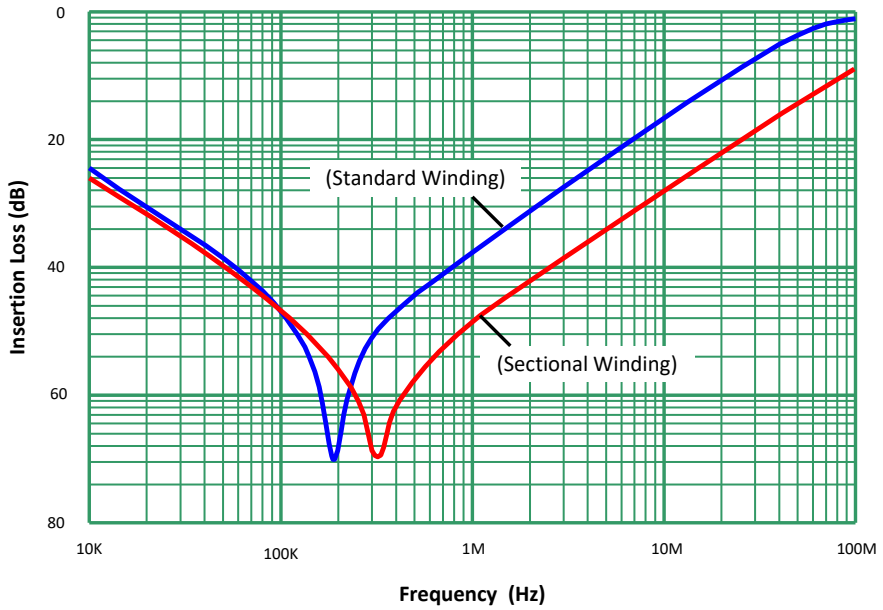
L_{CM} = 11.7 mH, L_{DM} = 50 µH @ 1V/10kHz

$$\frac{L_{DM}}{L_{CM}} = \frac{50\mu}{11.7m} = 0.43\%$$

降低層間雜散電容的共模電感

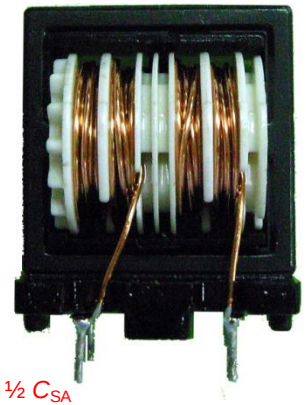
分區/槽繞 (Sectional Winding)



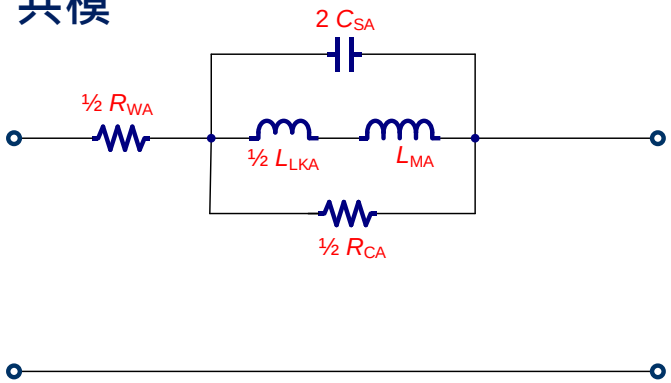


ET28 共模電感參數萃取

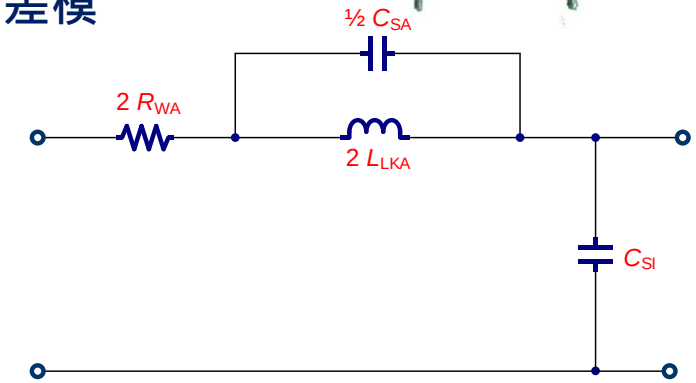
L_{MA}	L_{LKA}	R_{CA}	C_{SA}	R_{WA}
10mH	29uH	24KΩ	4pF	26mΩ



共模



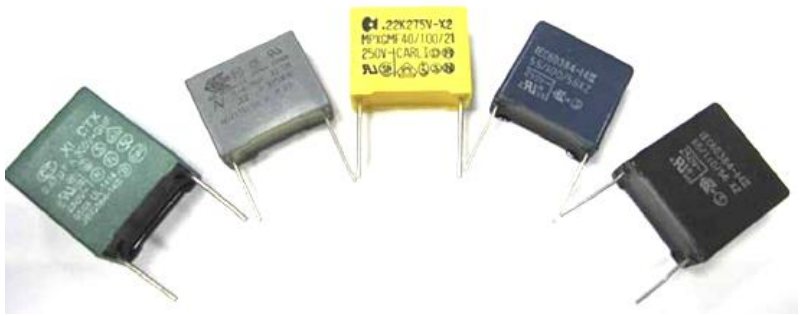
差模



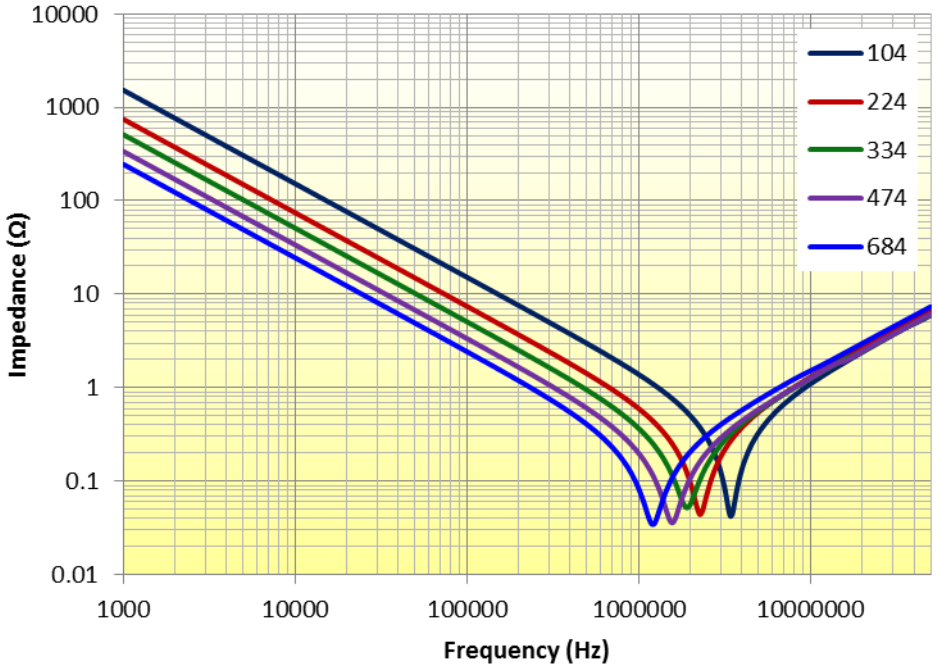
- 雜散電容 C_{SA} = 4pF

$$\frac{L_{DM}}{L_{CM}} = \frac{2 \times 29\mu}{10m} = 0.58\%$$

X-電容 (X-Cap)



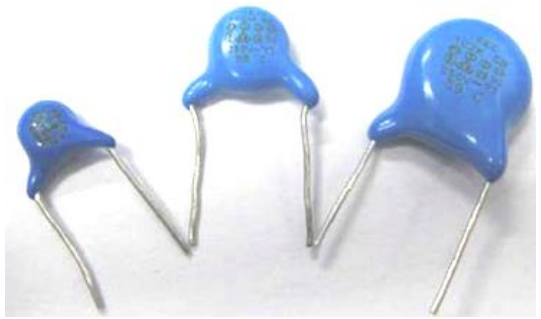
$$R + sL + \frac{1}{SC} = \frac{1 + s^2LC + sRC}{SC}$$



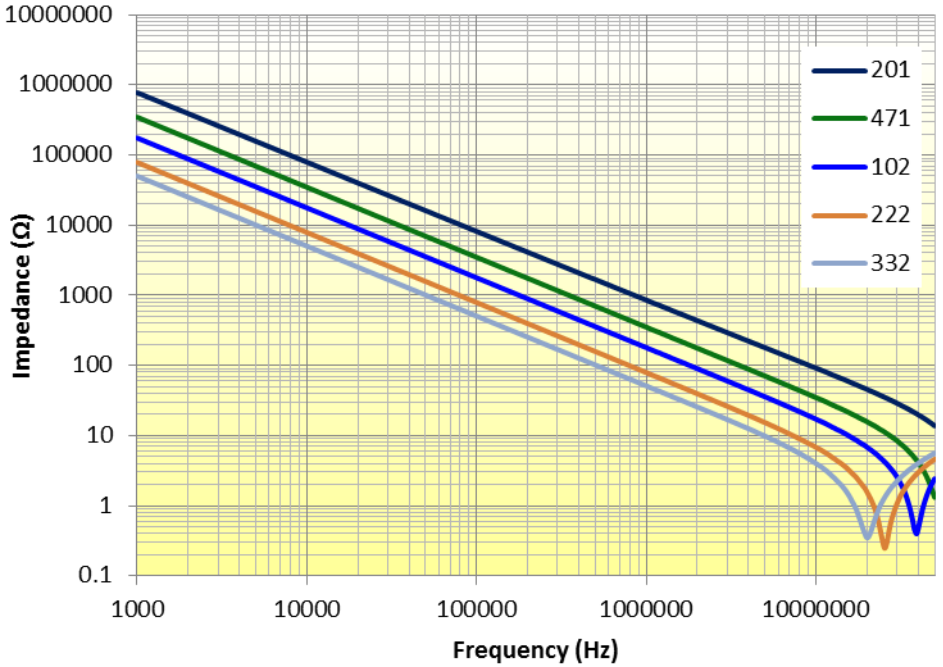
- 安規電容 (X1, X2)
- 跨接於L與N, 0.1μF - 1μF
- 關機放電問題(放電電阻功耗)

- 與 LISN 100Ω 並聯
- 常與差模電感形成二階濾波器

Y-電容 (Y-Cap)

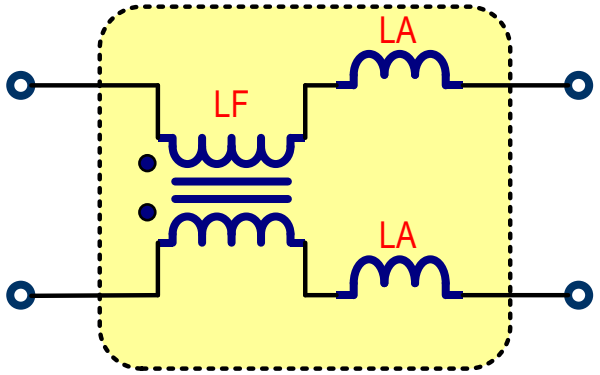


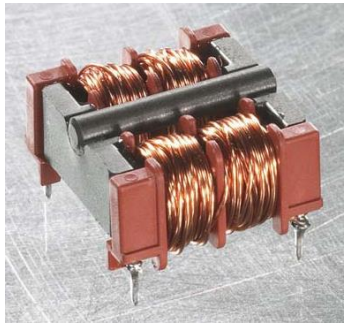
$$R + sL + \frac{1}{SC} = \frac{1 + s^2LC + sRC}{SC}$$

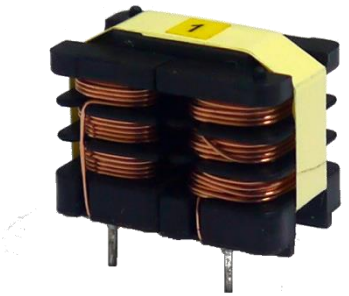


- 安規電容 (Y1, Y2)
- 分別跨接於L、N對G 或初次級靜點
- 安規漏電流限制，一般容值小於3300pF
- 非常好的頻率特性

混成扼流電感 (Hybrid Choke)



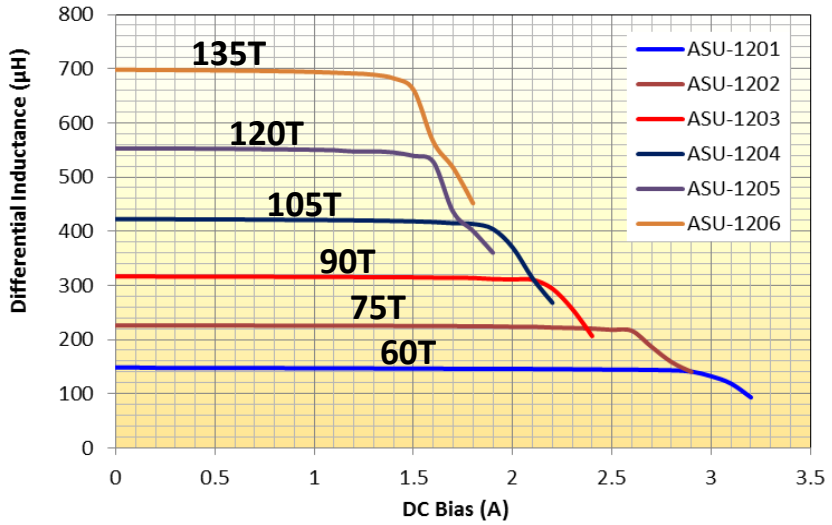




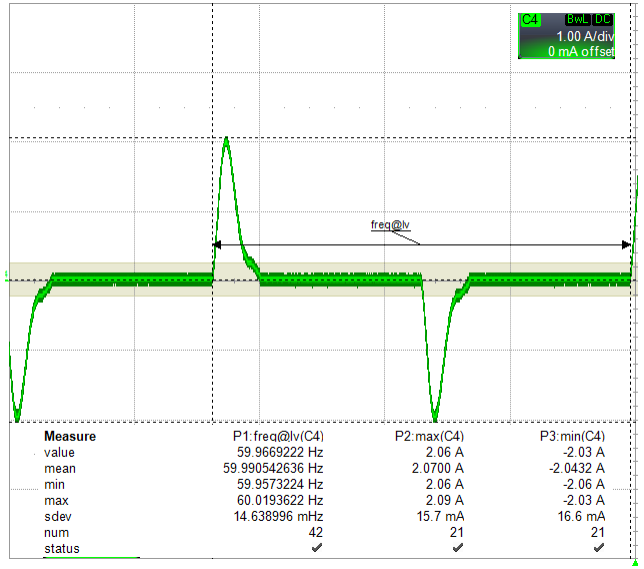
- 利用鐵芯的特性、形狀，配合線架設計，讓共模電感器有相對高的漏電感。漏電感就是等效的差模電感。
- 結合共模與差模電感的新雜訊濾波電感(可稱為混成扼流電感或集成共模電感)不僅可以節省PCB 空間，可以省下成本。

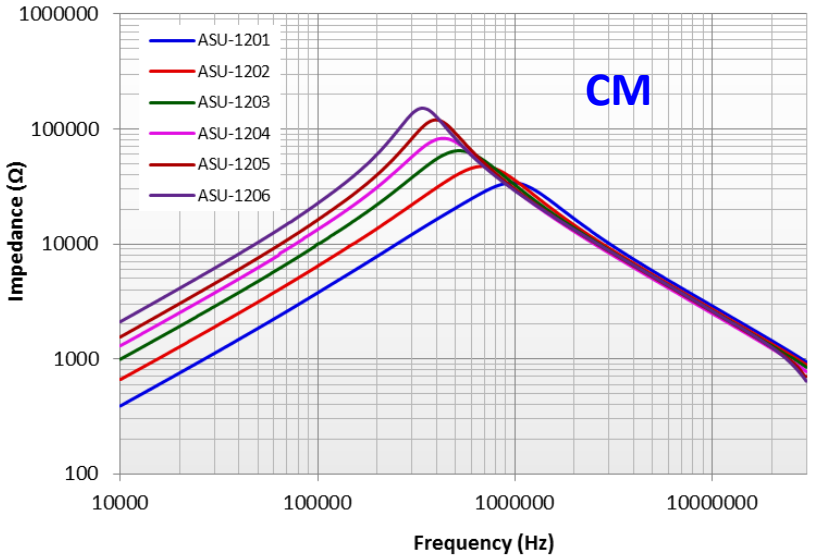
混成扼流電感 ASU1200系列 (7000μ)

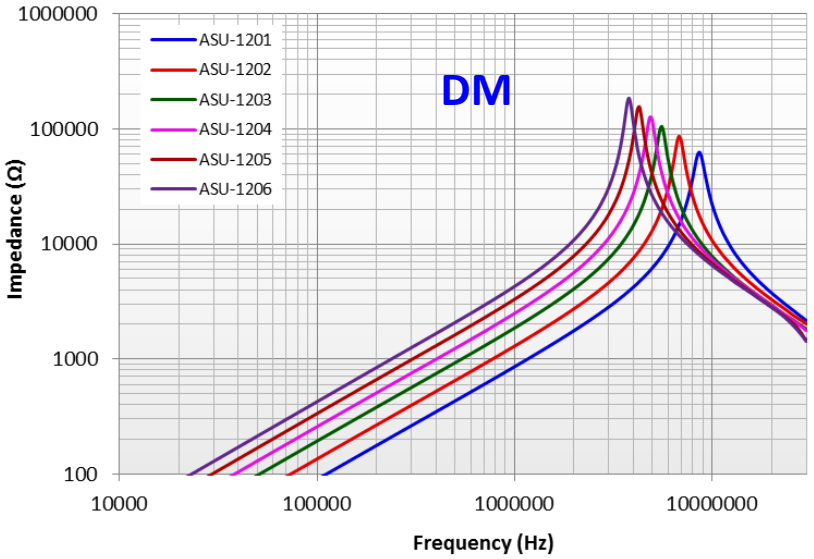
$$\frac{L_{DM}}{L_{CM}} = 3.5\%$$



輸入電流波形







- 全橋整流濾波常規波形
- 115 Vac 輸入電壓下，峰值電流約 1A/12W
- 流經所有串聯阻抗(差模電感)，特別注意磁飽和問題

小結

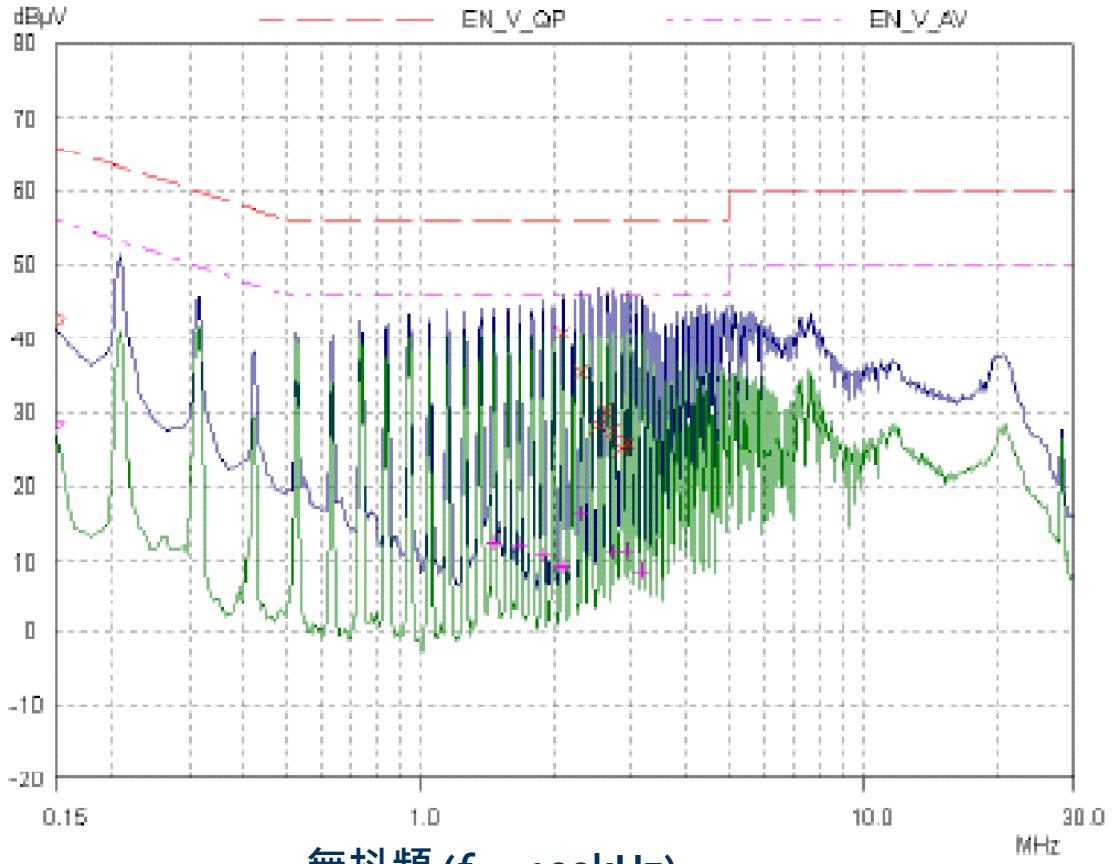
- 差模與共模雜訊可以藉由量測技巧加以分離。濾波器的設計可依差模或或共模分別對策。
- 差模電感除電感值外特別注意鐵芯一旦飽和，濾波效果必然折扣。
- 共模電感除感值外特別注意其頻寬問題。同時其漏電感成為差模電感，有助於降低差模雜訊。混成扼流圈為一項可以降低成本與濾波器體積的技術，值得關注。
- 不論電感或電容均非理想元件，藉由高頻阻抗分析儀，才可以準確預估其濾波效能。
- 掌握了雜訊源、檢知(LISN)與濾波器特性，就可以輕易的解決傳導EMI 問題，解省時間與成本。

範例1：19V/30W 返馳 (Flyback) 電源適配器

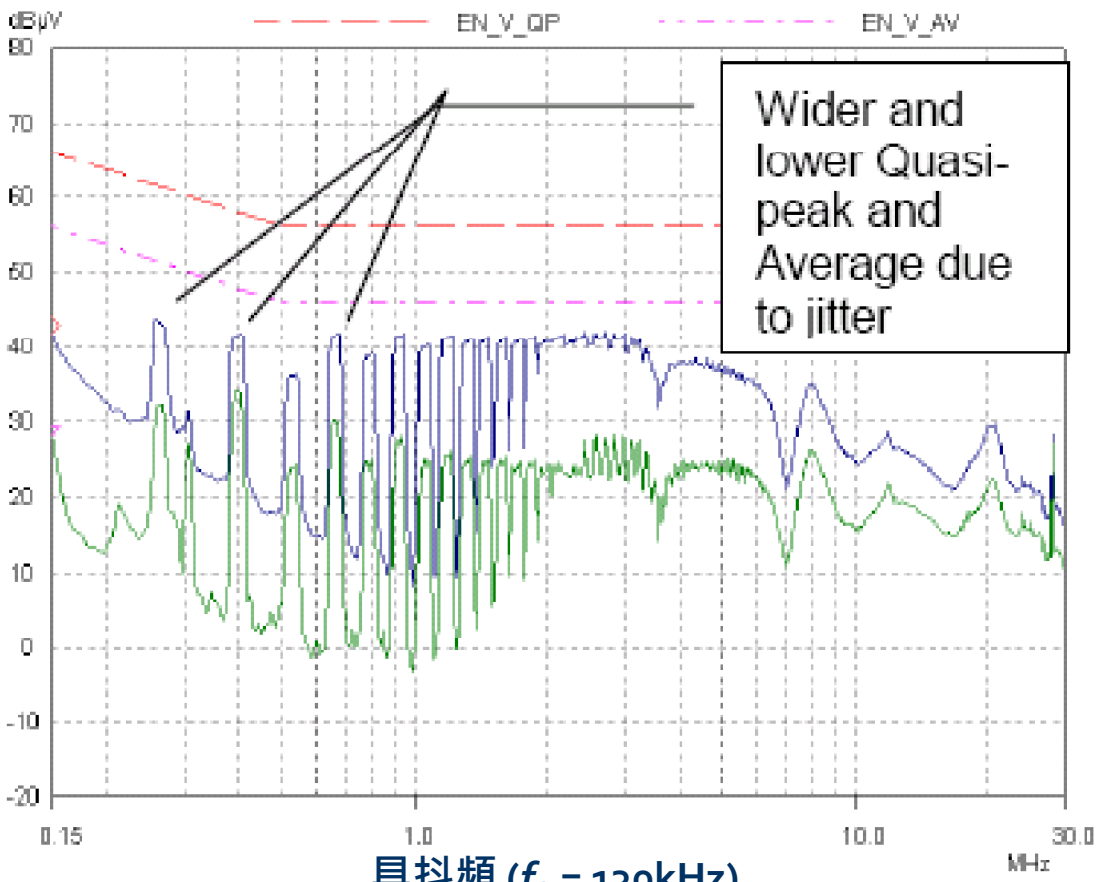
輸入電壓 V_{IN}	110 Vac/60Hz
輸出電壓 V_O	19 V
輸出功率 P_O	30 W
開關頻率 f_S	65 kHz (抖頻)
控制 IC	RT7736
激磁電感 L_P	1mH
輸入電容 C_O	82 µF/400V
輸入電容 ESR	700 mΩ

- 兩線輸入，輸出不接大地
- RT7736 新型抖頻(Frequency Dithering)功能
- T14x9x8 (µ=10,000) 共模電感
- X2電容 0.22µF

抖頻與 EMI 頻譜



無抖頻 (f_S = 100kHz)

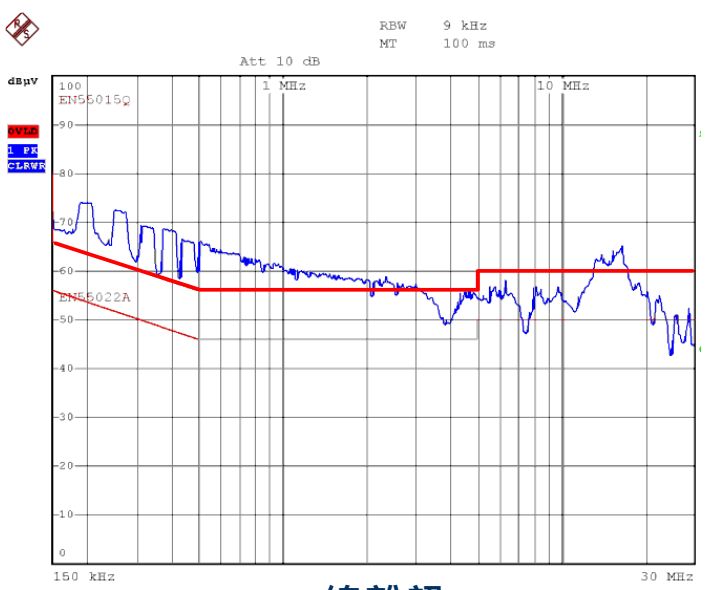


具抖頻 (f_S = 130kHz)

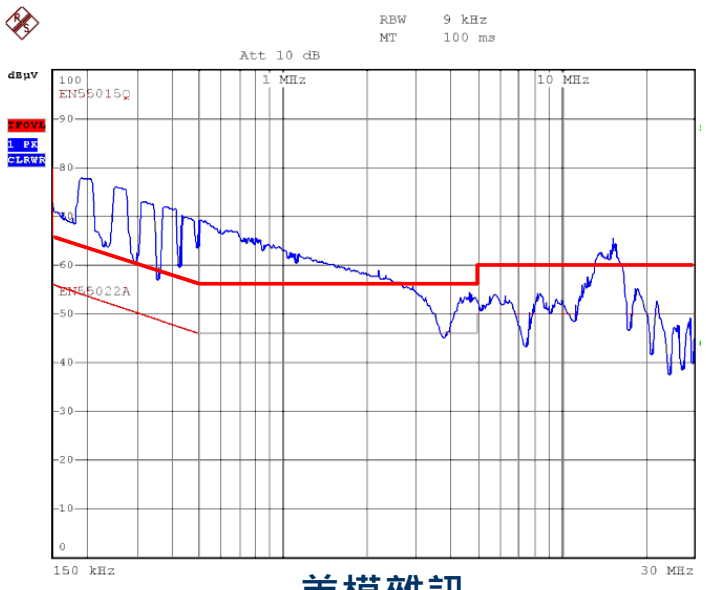
QP, AVG

- 抖頻可以降低約5到15dB的雜訊頻譜。(視抖頻技術而定)
- 約略可以縮小EMI 濾波器一個等級 (L與C 各小一半)。(12dB)

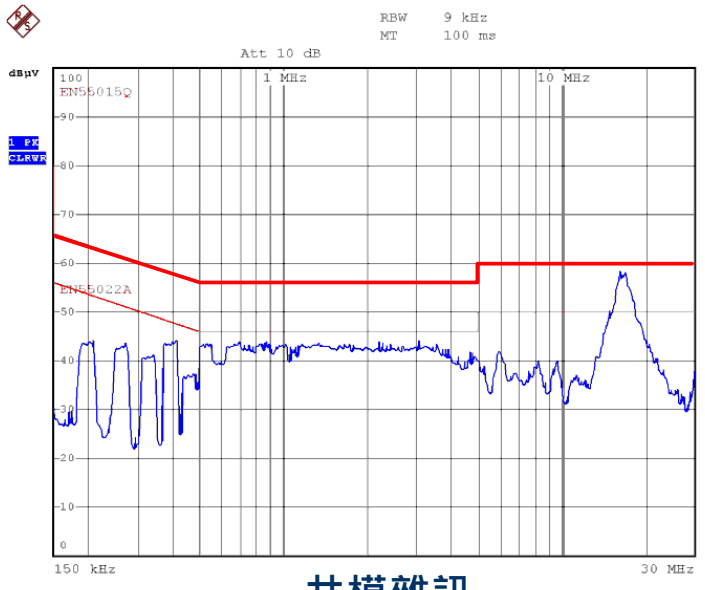
拆除濾波器的雜訊源頻譜



L1總雜訊



差模雜訊

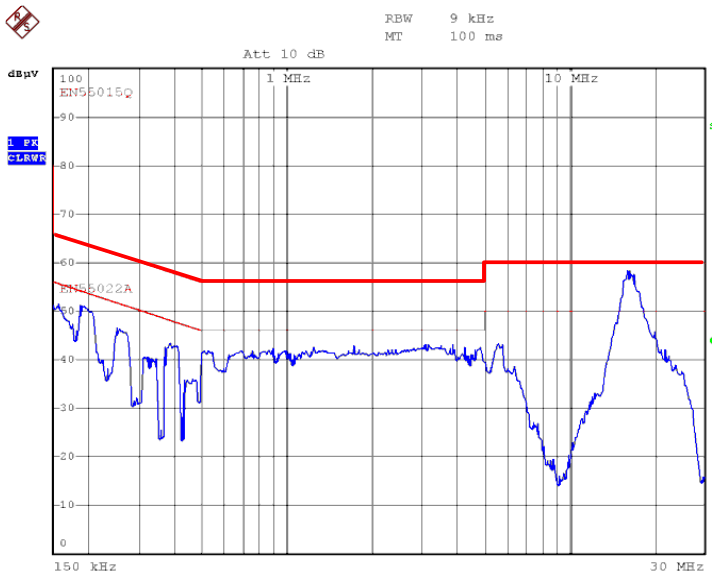


共模雜訊

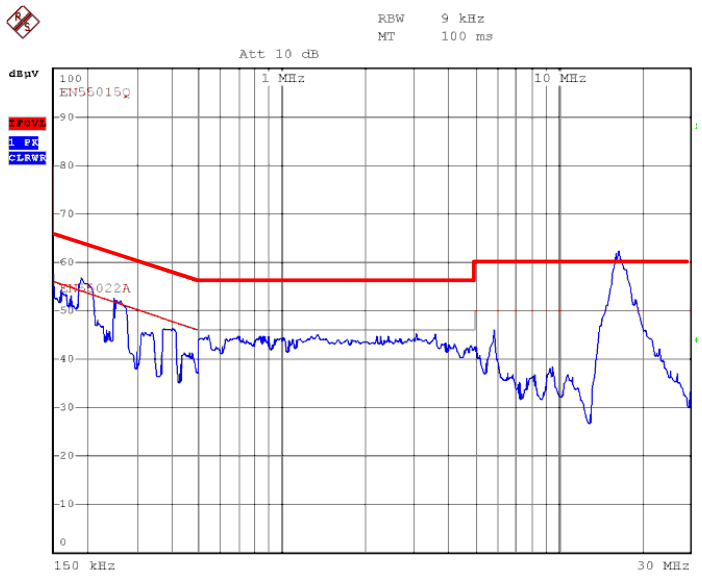
- 抖頻效果十分明顯(降低雜訊頻譜)
- 差模雜訊主宰低頻總雜訊頻譜
- 差模雜訊：-20dB/dec
- 共模雜訊也有抖頻效果

因為量測設備接地不佳，高頻(>10MHz) 受到其他電器影響。

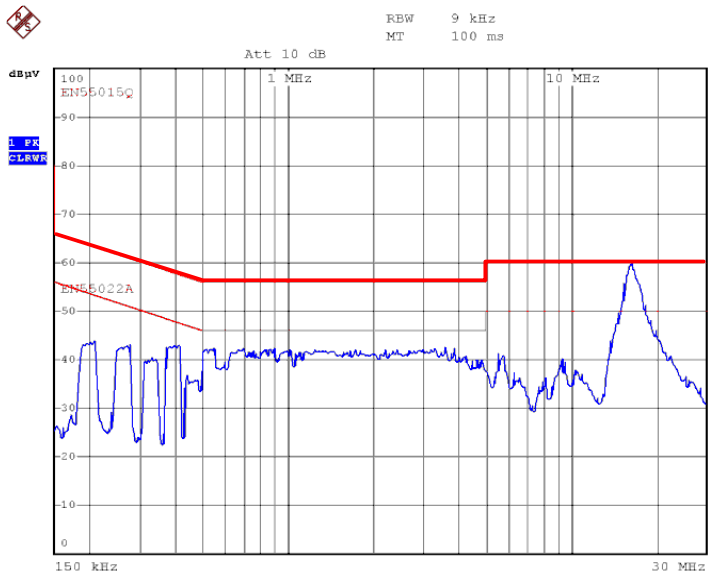
演示板的EMI效能呈現



L1總雜訊



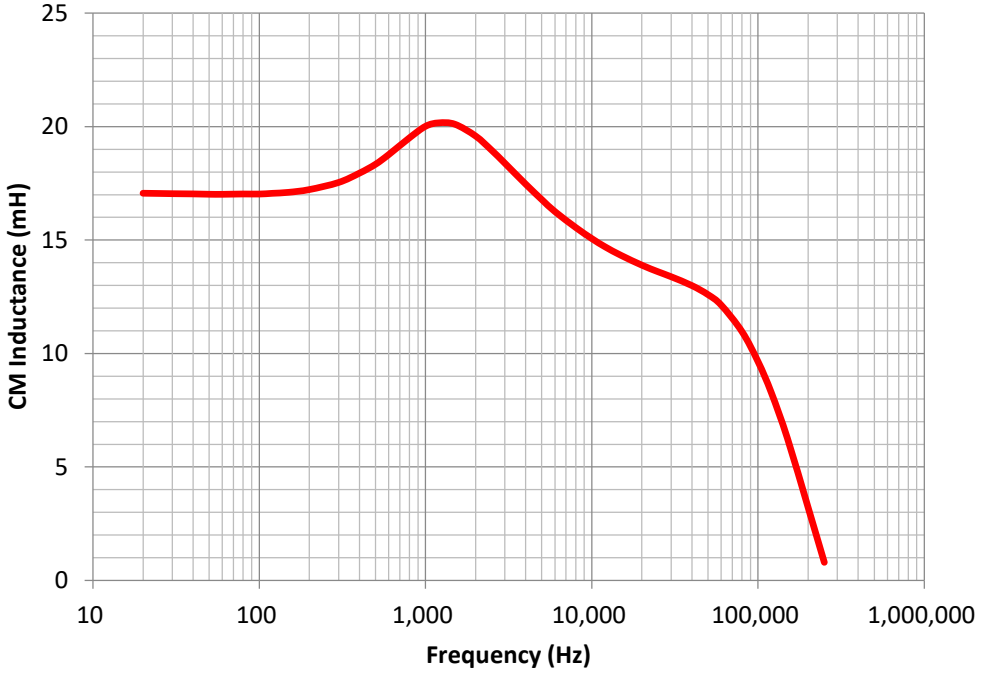
差模雜訊

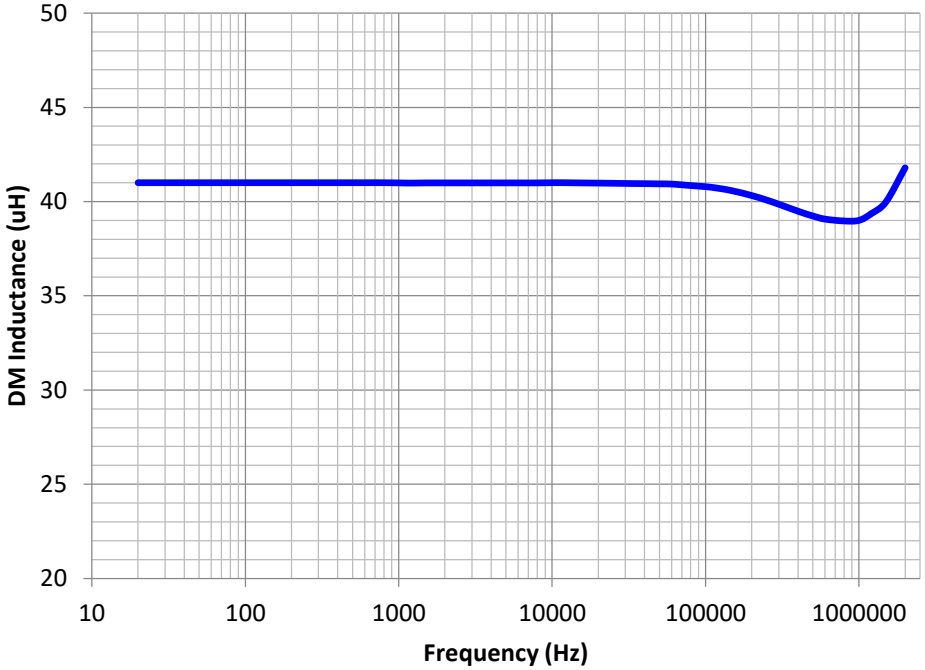


共模雜訊

- 差模有很好的效果，共模的效果不明顯 (為甚麼 ?)
- 差模@200kHz約為55dBµV (未裝濾波器為78dBµV，約降低23dB)

T14x 9x8 (μ_r=10k) 共模電感量測





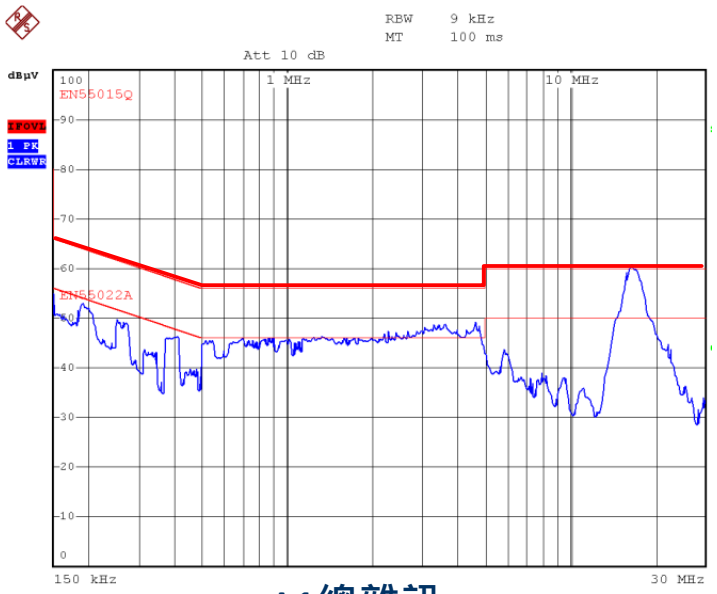
- 共模電感值在100KHz 時已衰減至10mH，約280KHz 時變成電容性。
- 差模電感(漏電感)在2MHz 以下約略成常數(41μH)

$$f_{RDM} = \frac{1}{2\pi\sqrt{L_{DM} \cdot C_X}} = \frac{1}{2\pi\sqrt{41\mu \cdot 0.22\mu}} = 53\,\text{kHz}$$

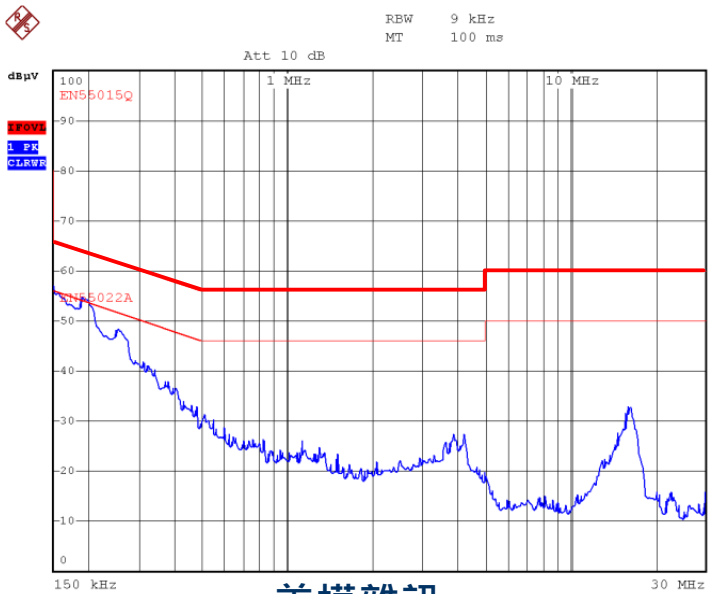
$$\text{ATTN} = 40 \cdot \log\left(\frac{200k}{53k}\right) = 23\,\text{dB}$$

只裝差模濾波器 (差模電感和 X 電容)

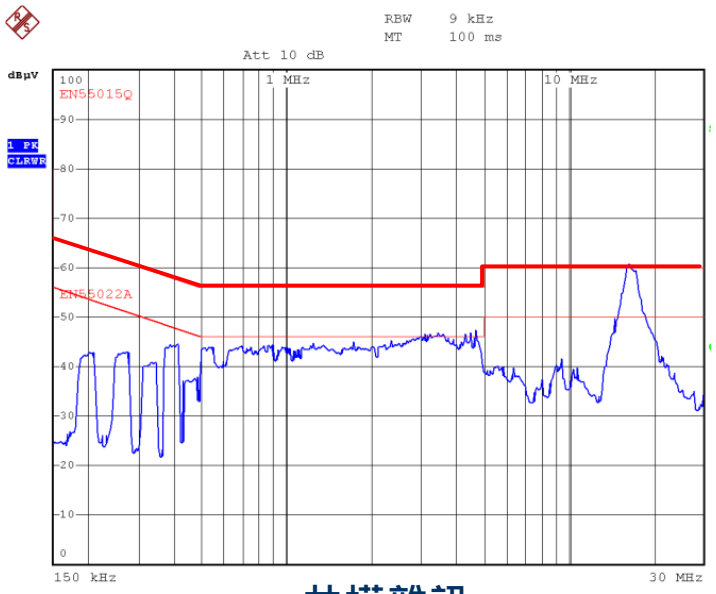
- 用一個便宜的差模電感(53μH)取代共模電感。
- 如預期的結果：差模頻譜更低，共模不變。



L1總雜訊



差模雜訊

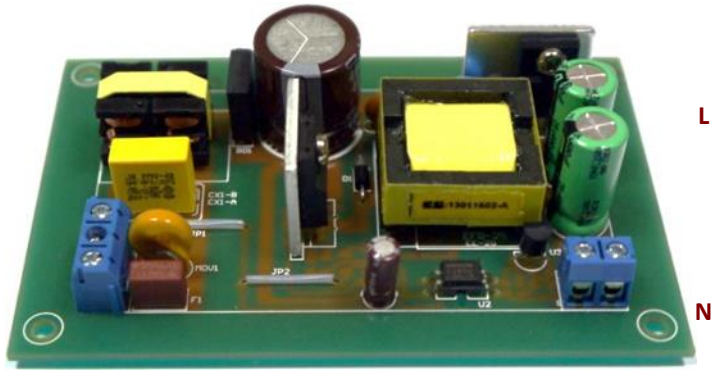


共模雜訊

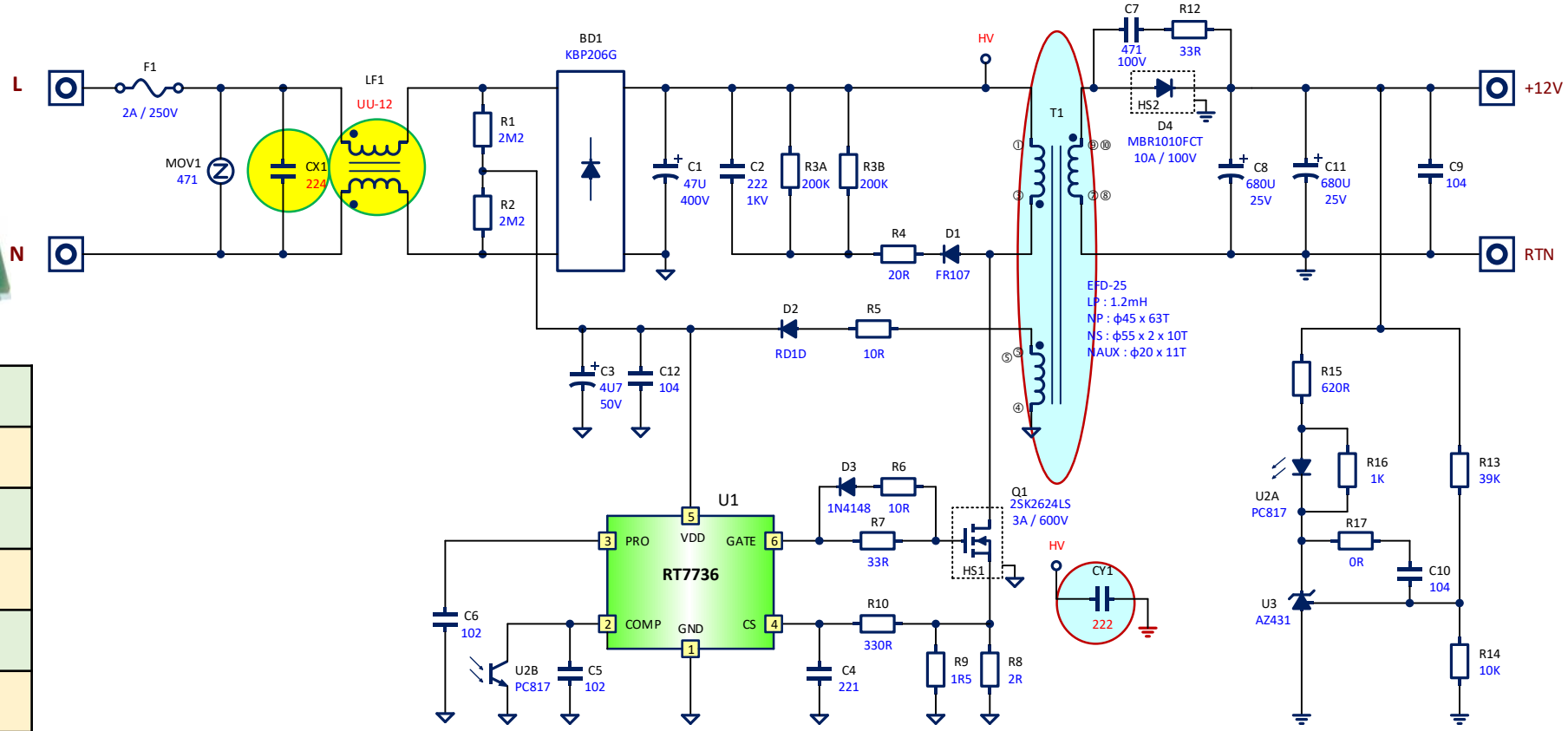
小結

- 輸出端不接大地(LISN GND)，共模雜訊僅靠電路對大地的雜散電容耦合，阻抗很大，所以在LISN檢知的共模雜訊很低。
- 共模雜訊原本已經很低，利用CM Choke 濾雜訊的用處不大，徒浪費成本。
- 濾除差模雜訊完全倚賴CM Choke 的漏感和X-Cap形成的二階LC濾波器。
- 將CM Choke 改成低成本的DM Choke 也可得到一樣的效果。

範例2：離線24W返馳式電源供應器電路圖

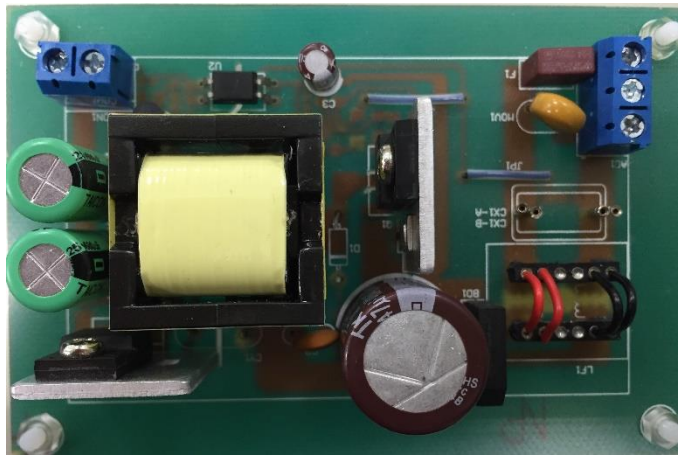


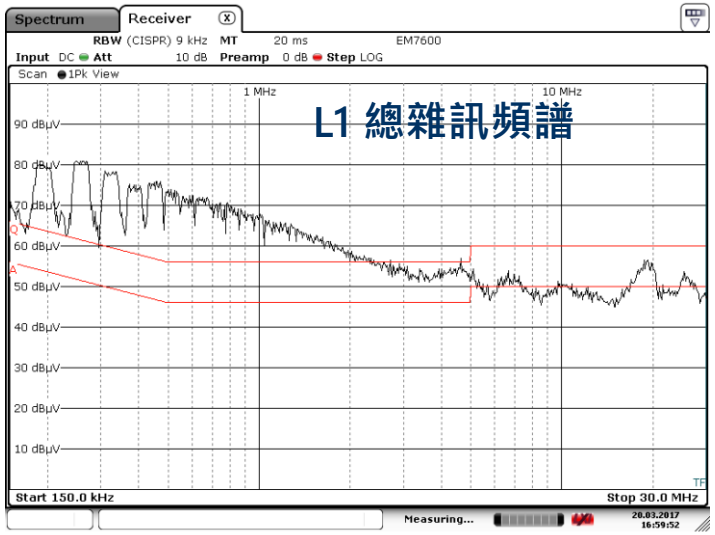
輸入電壓 V_{IN}	110 Vac/60Hz
輸出電壓 V_O	12 V
輸出功率 P_O	24 W
開關頻率 f_S	65 kHz (抖頻)
控制 IC	RT7736
變壓器 EFD-25	1.2mH
輸入電容 C_O	47 μF/400V
輸入電容 ESR	250 mΩ

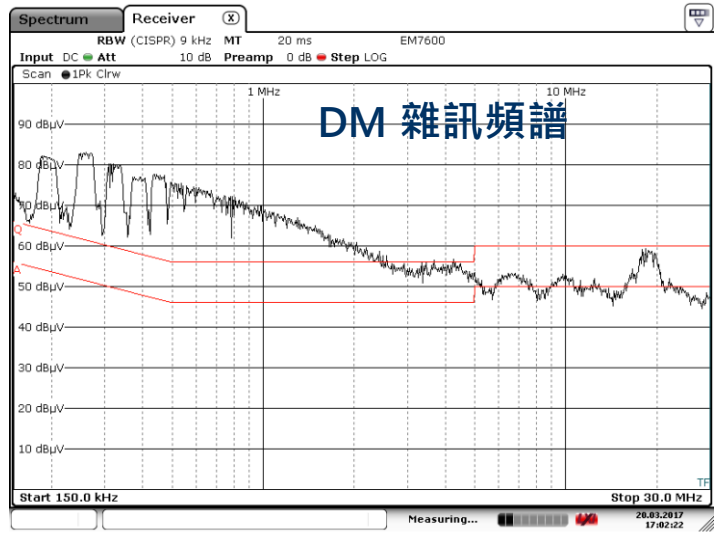


L,N 兩線輸入 (撤除慮波器，負載不接地)

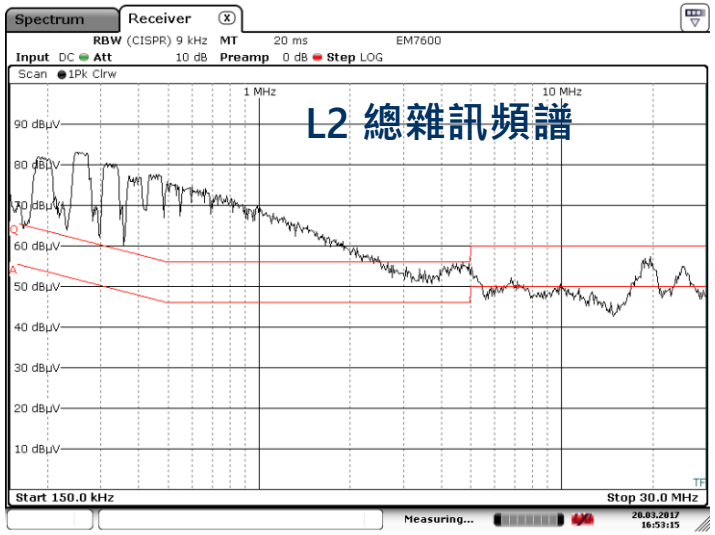
Peak 量測

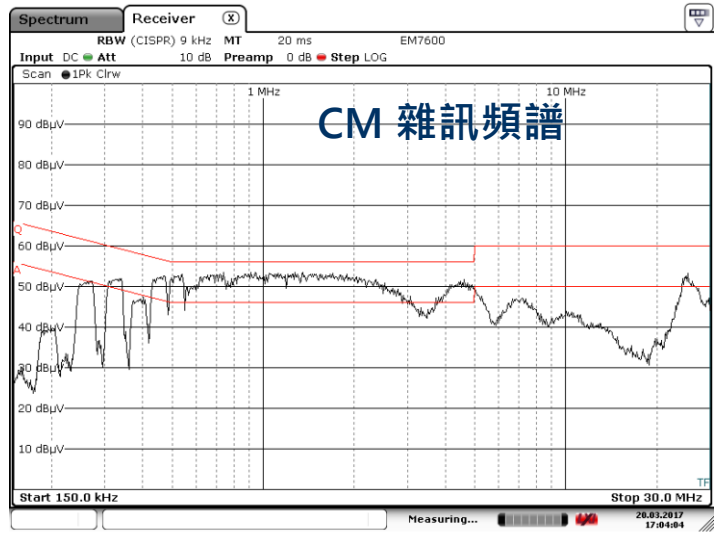




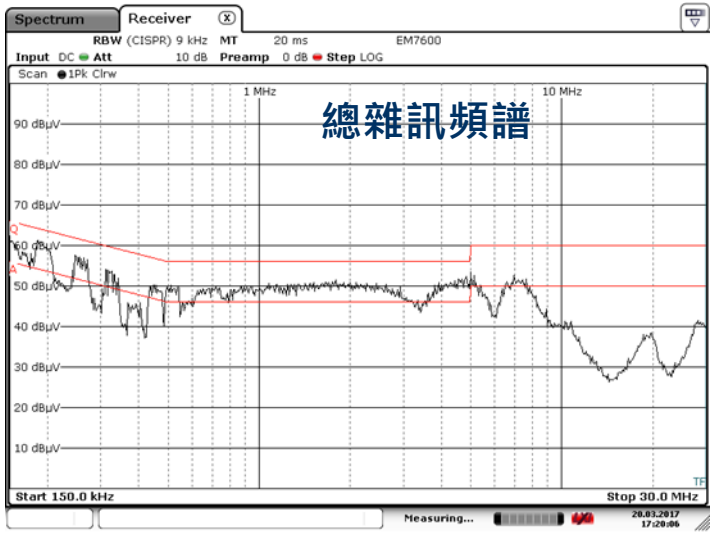


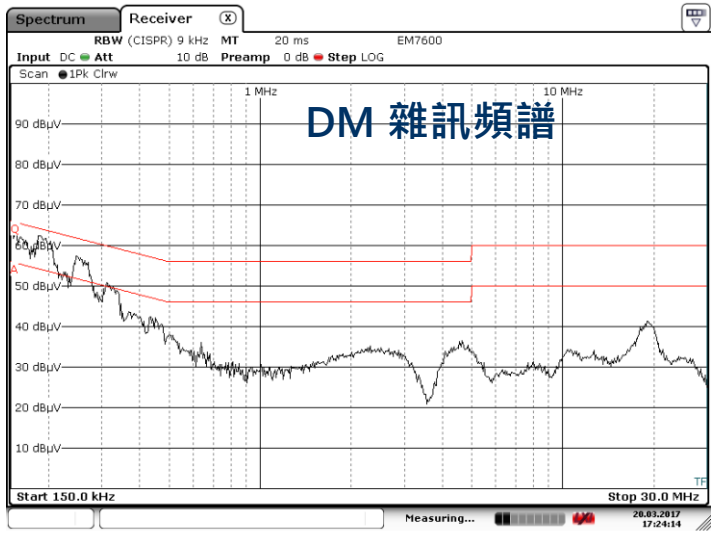
- L1與L2總雜訊頻譜幾無二致
- 低頻(<3MHz) 有-20dB/dec 斜率，與理論一致。(注意低頻段抖頻功能明顯)
- 高頻部份較不規則，DM雜訊約等於總雜訊
- 沒有直接地回路，CM雜訊低於法規線
- 顯然DM雜訊主導整個雜訊干擾

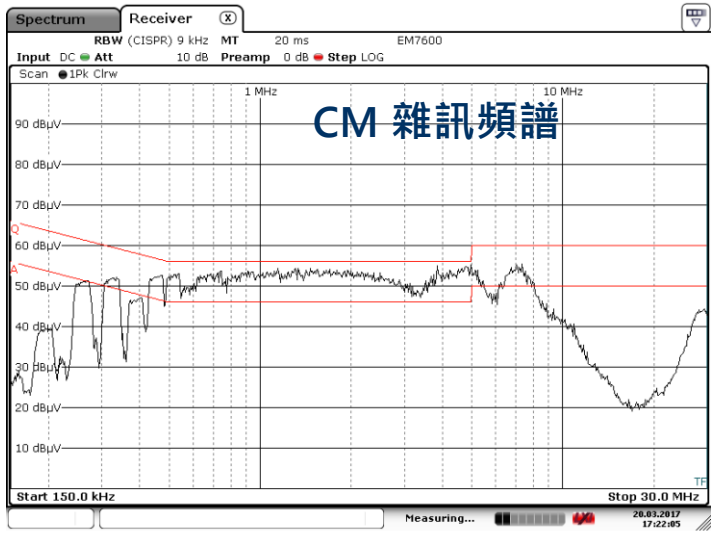




加入差模濾波器對策 (L,N 兩線輸入)

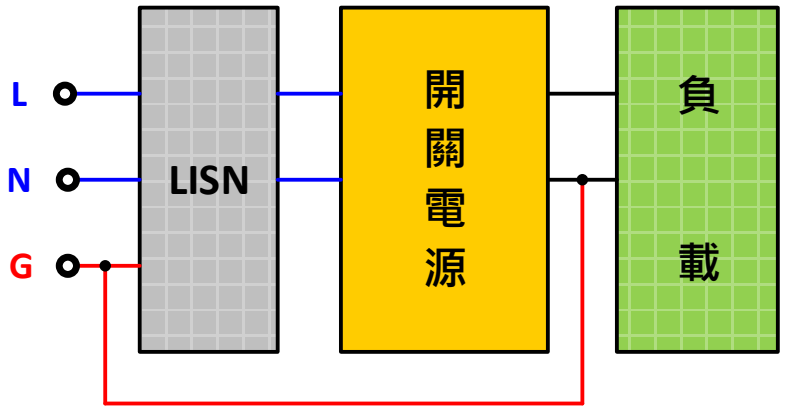


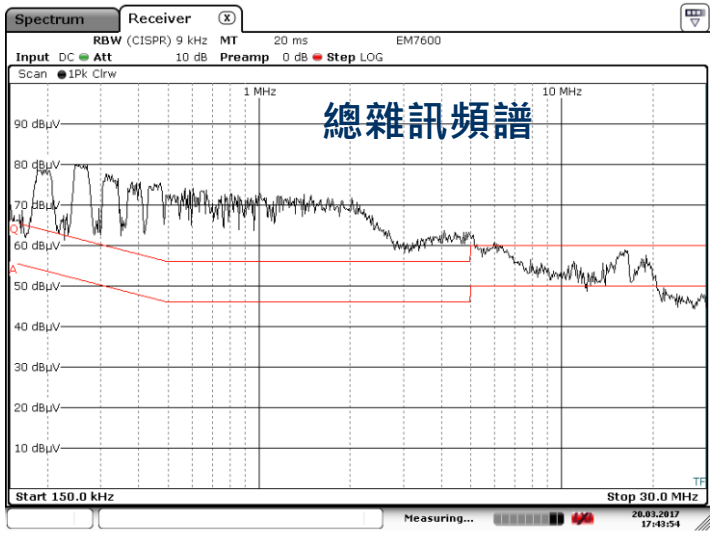




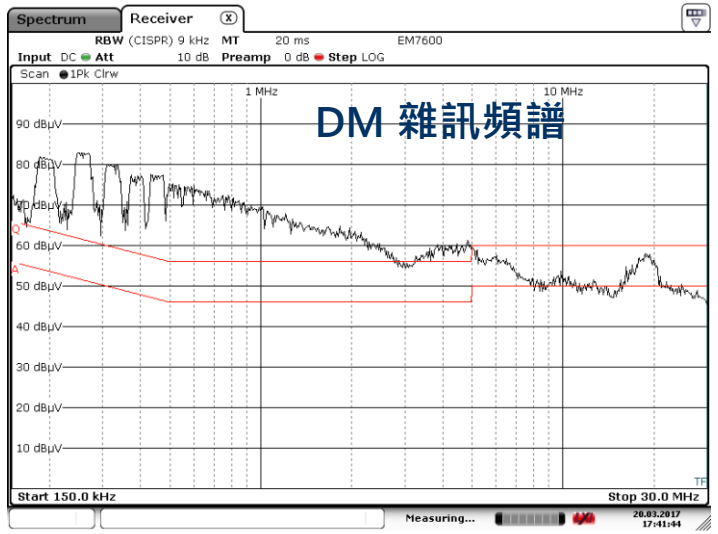
- 加 DM電感和X-CAP
- DM雜訊有效的抑制
- CM雜訊幾乎不變
- 總雜訊視DM或CM孰高孰主導
- 基本上已符合法規要求

L,N 兩線輸入 (撤除慮波器，負載接大地)



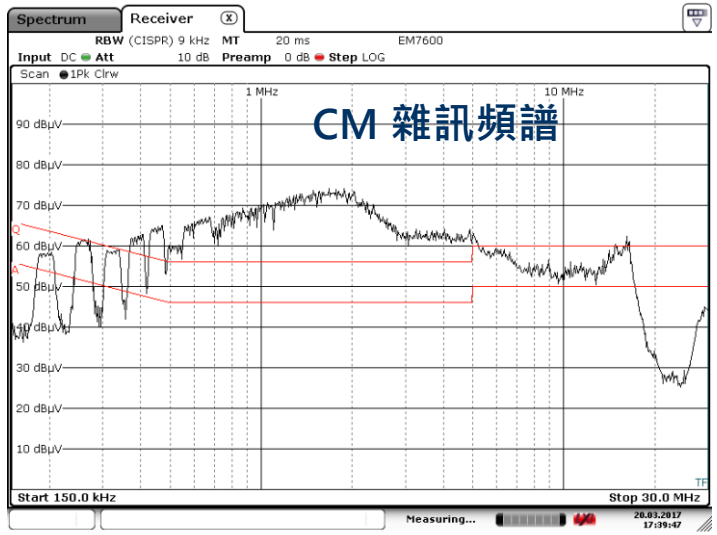


總雜訊頻譜



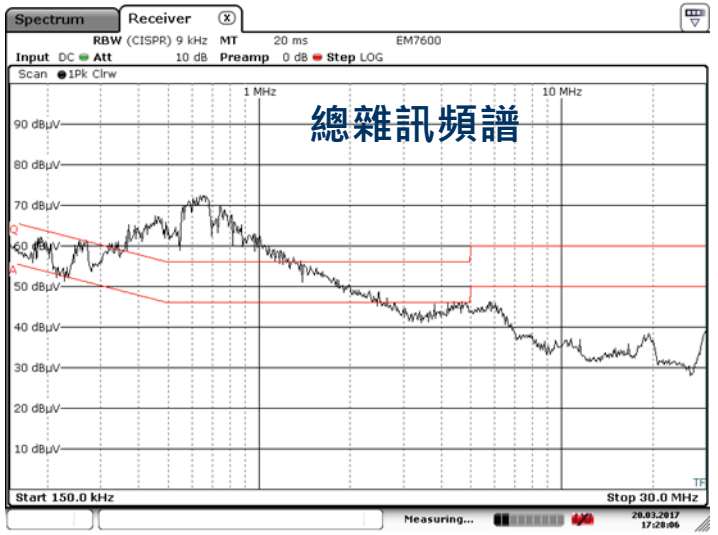
DM 雜訊頻譜

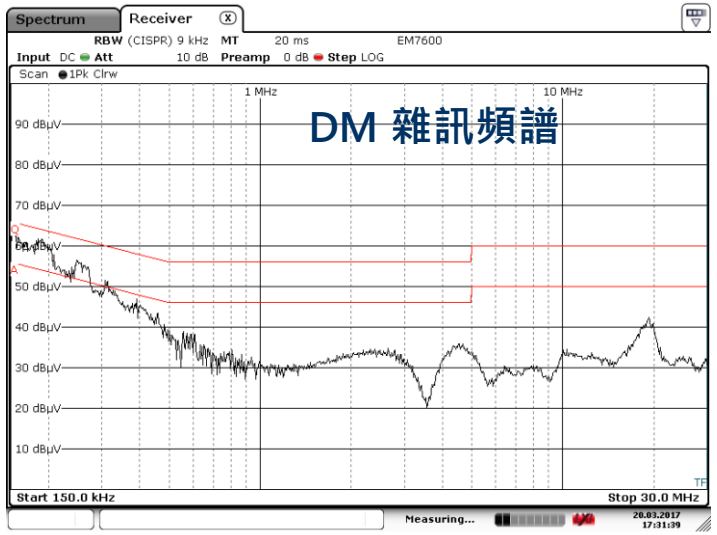
- DM 與原來的一樣。
- 因為有直接耦合通道，CM雜訊浮高。



CM 雜訊頻譜

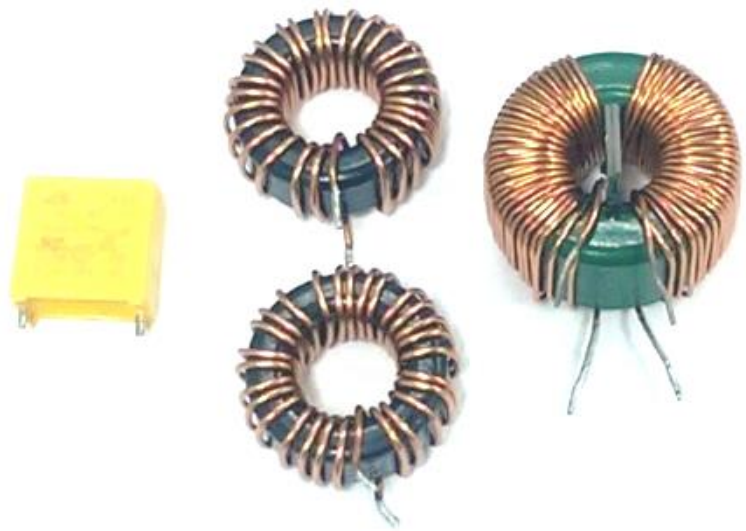
加入差模濾波器對策 (L,N 兩線輸入&負載接地)

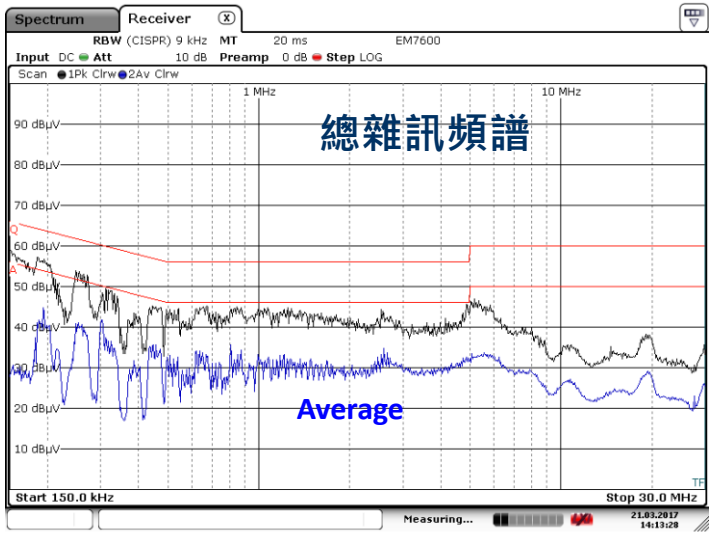




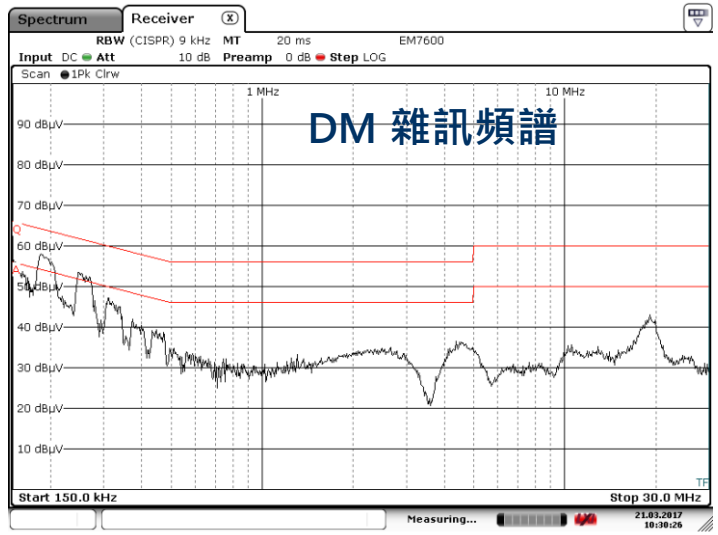
- DM雜訊被差模濾波器有效的濾除
- CM雜訊完全沒有被抑制
- 總雜訊為DM與CM雜訊之向量和(高於法規線)

再加入共模電感對策 (L,N 兩線輸入&負載接地)

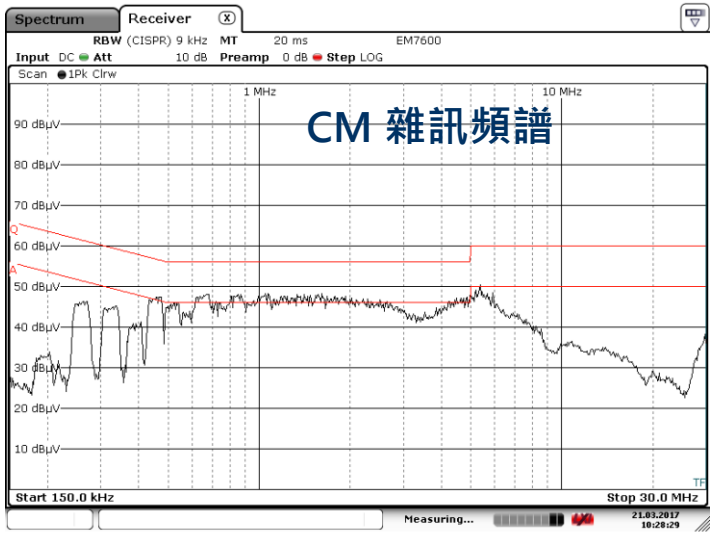




總雜訊頻譜



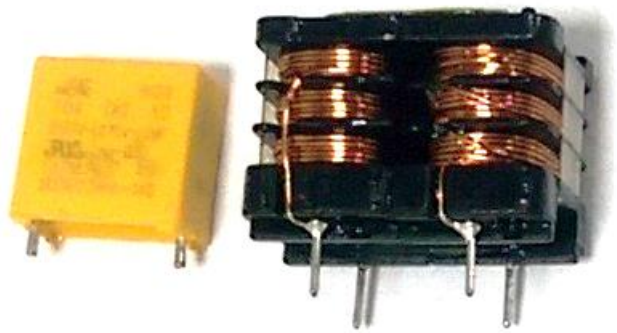
DM 雜訊頻譜

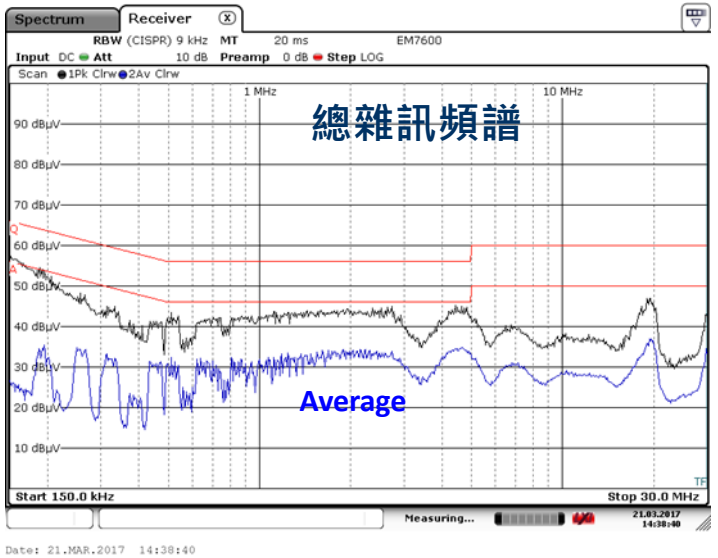


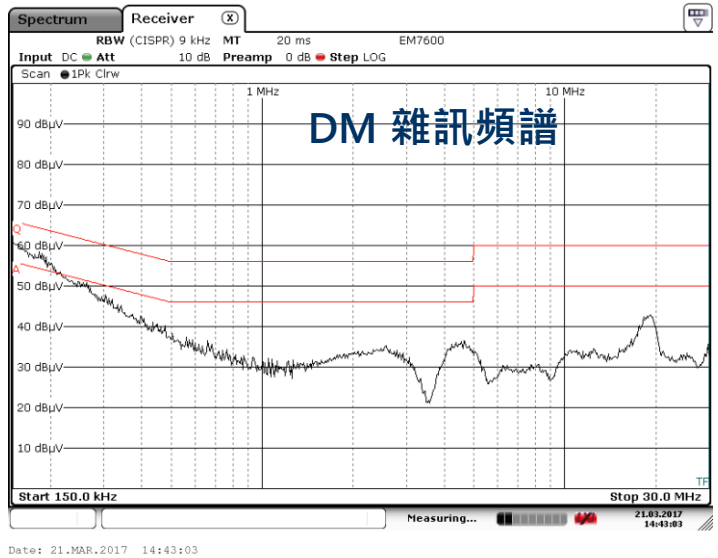
CM 雜訊頻譜

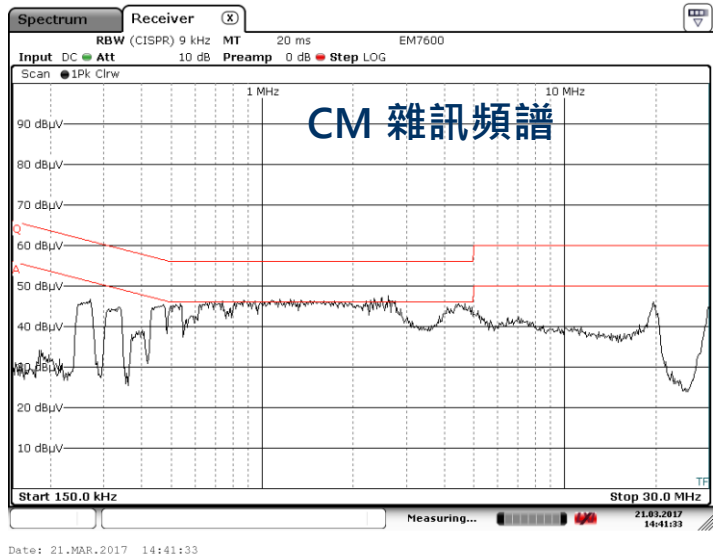
- DM與CM雜訊被濾波器有效的濾除
- 總雜訊符合法規

混成濾波器對策 (L,N 兩線輸入&負載接地)









- 用ASU1203 混成濾波器取代一個CM choke 與兩個 DM choke
- DM/CM雜訊同時被有效的濾除
- 總雜訊符合法規

返馳電源傳導電磁干擾抑制 Part 1

Conducted Emission EMI Reduction of Flyback Power Supplies

王信雄博士

16:50-17:00

EMI is a relatively simple problem to understand but can be a complex problem to solve.

Thanks