結合光耦和分路穩壓器的返馳電源回授設計

Off-line Flyback Feedback Design with Optocoupler and Shunt Regulator

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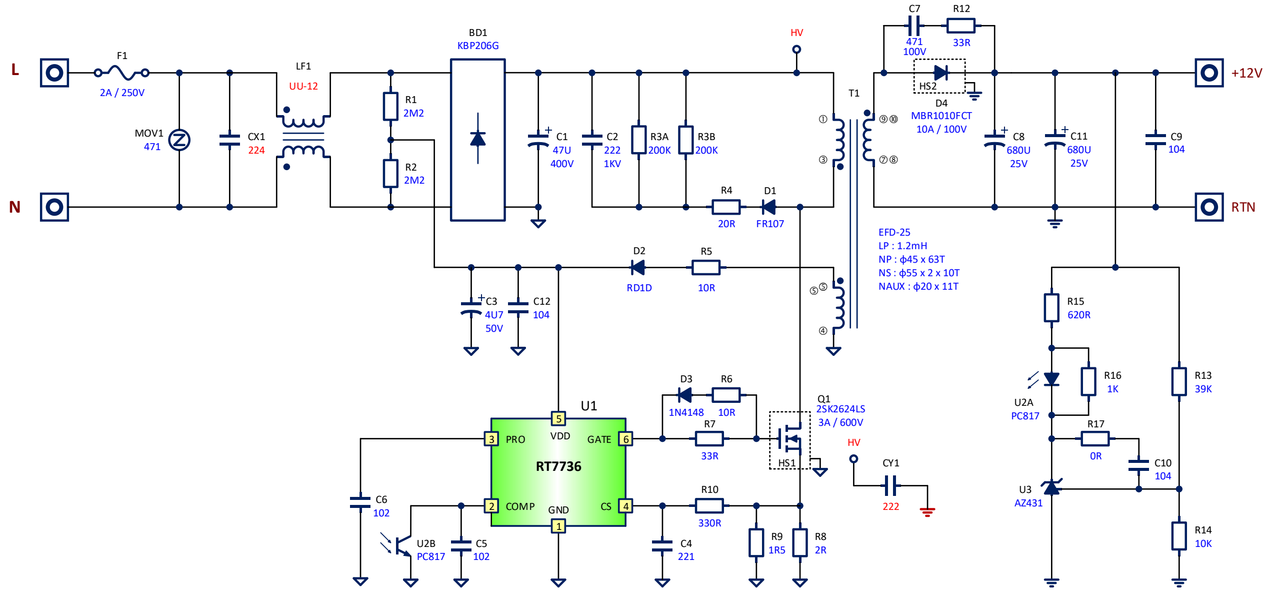


Outline

- DC Steady-State Analysis of a Flyback Converter
- Peak Current Mode Control (PCMC) and Compensation
- Small-Signal Modeling of Flyback Converters
- Type II (2P1Z) Compensator Implemented by Optocoupler and Shunt Regulator
- Stray capacitance of Optocoupler

Prerequisites

- Flyback Power Circuit Design
- Small-Signal Modeling of Switching Regulators
- Peak Current Model Control of Switching Converters

References

1. AN035_TW “離線返馳轉換器設計重點”, 立錡科技
2. AN017_TW “離線返馳轉換器回授設計”, 立錡科技
3. “開關轉換器控制理論與設計實務”, 王信雄 / 立錡科技，城邦出版社

Performance Related Technologies

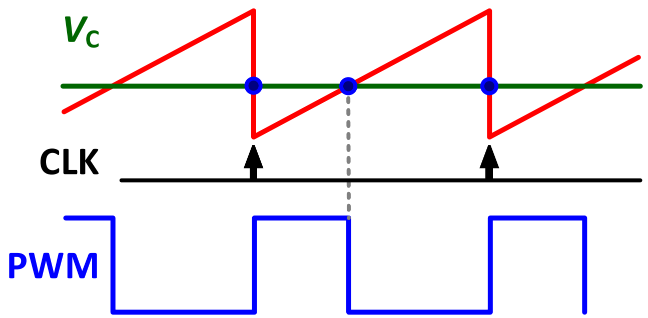
Power Processing Related

- Load Power
- Conversion Efficiency
- Output Voltage Ripple
- Weight and Volume
- Electromagnetic Interference (EMI)

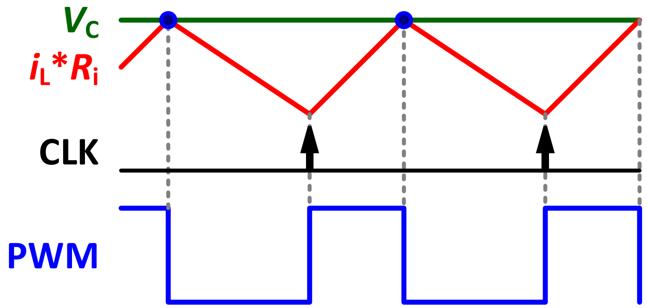
Control Related

- DC Regulation
- Line Rejection (Audio-Susceptibility)
- Load Rejection (Output Impedance)
- Response to a Step Load Change (Dynamic)
- Stability (Phase / Gain Margin)

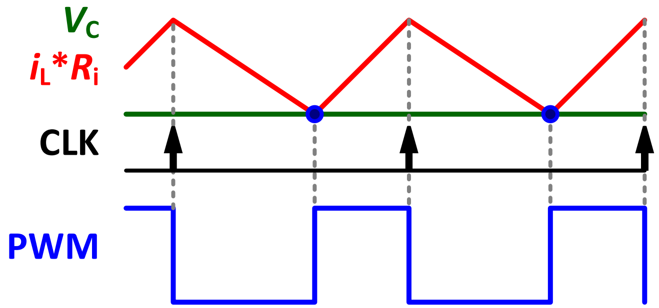
Control Schemes of Switching Converters



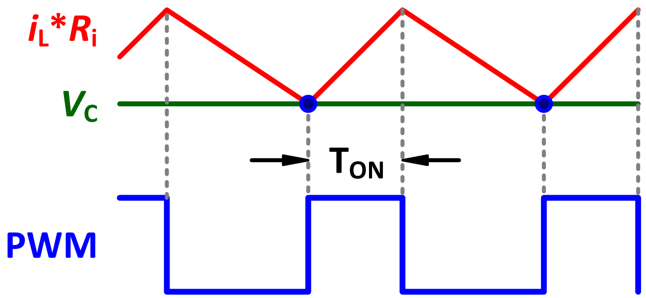
Voltage Mode Control



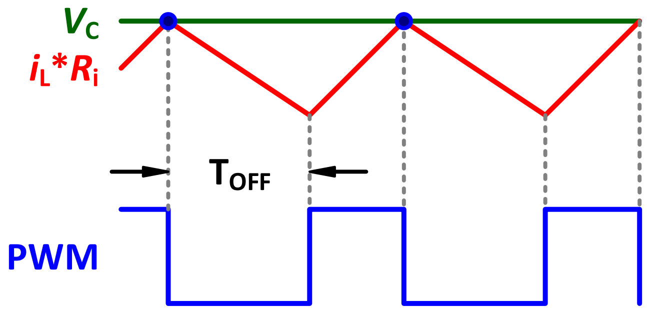
Peak Current Control



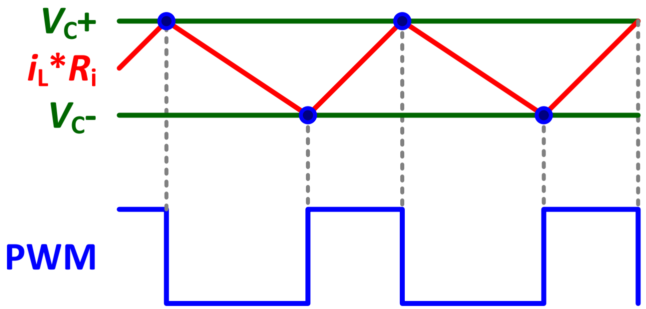
Valley Current Control



Constant ON Time Control

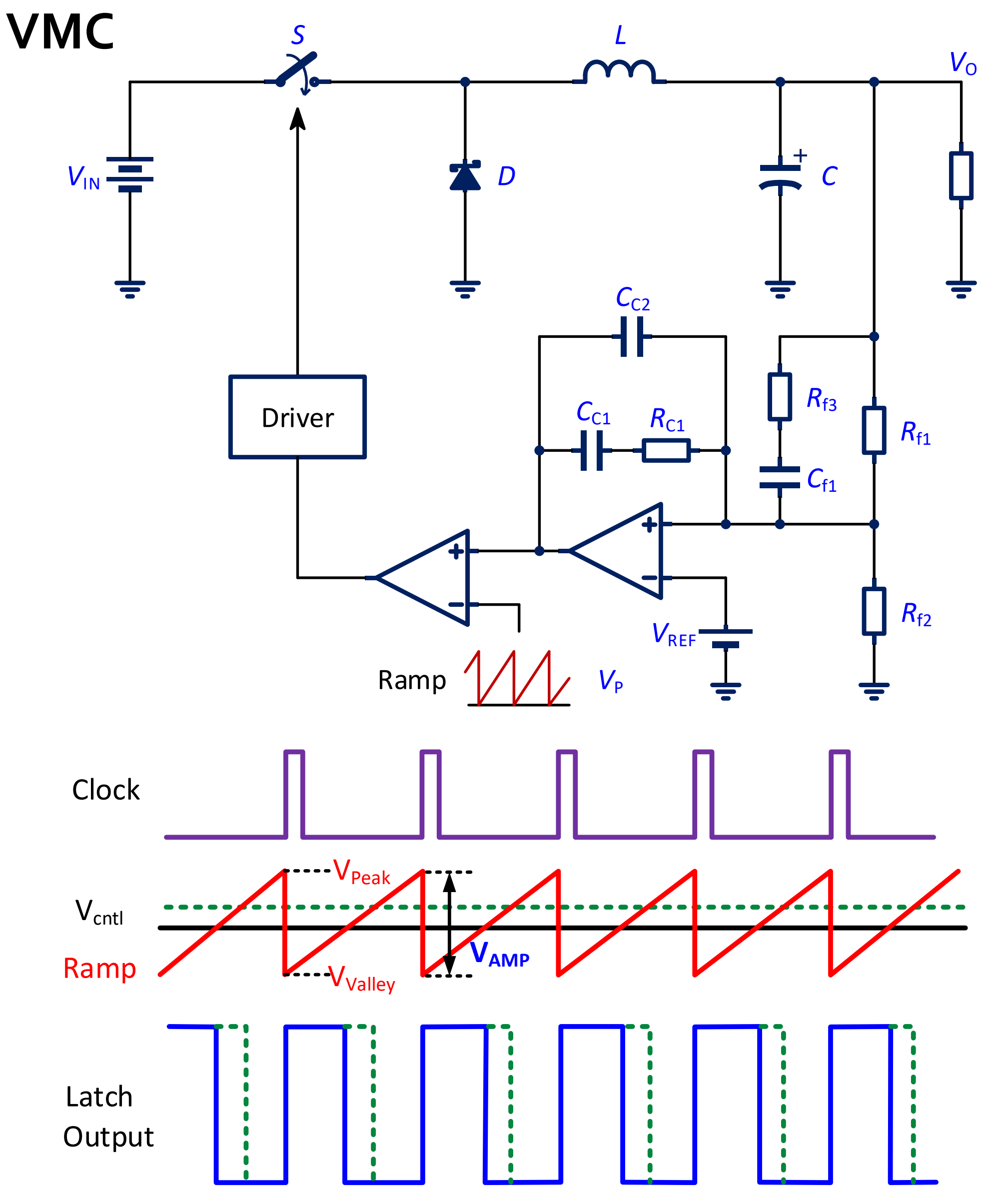


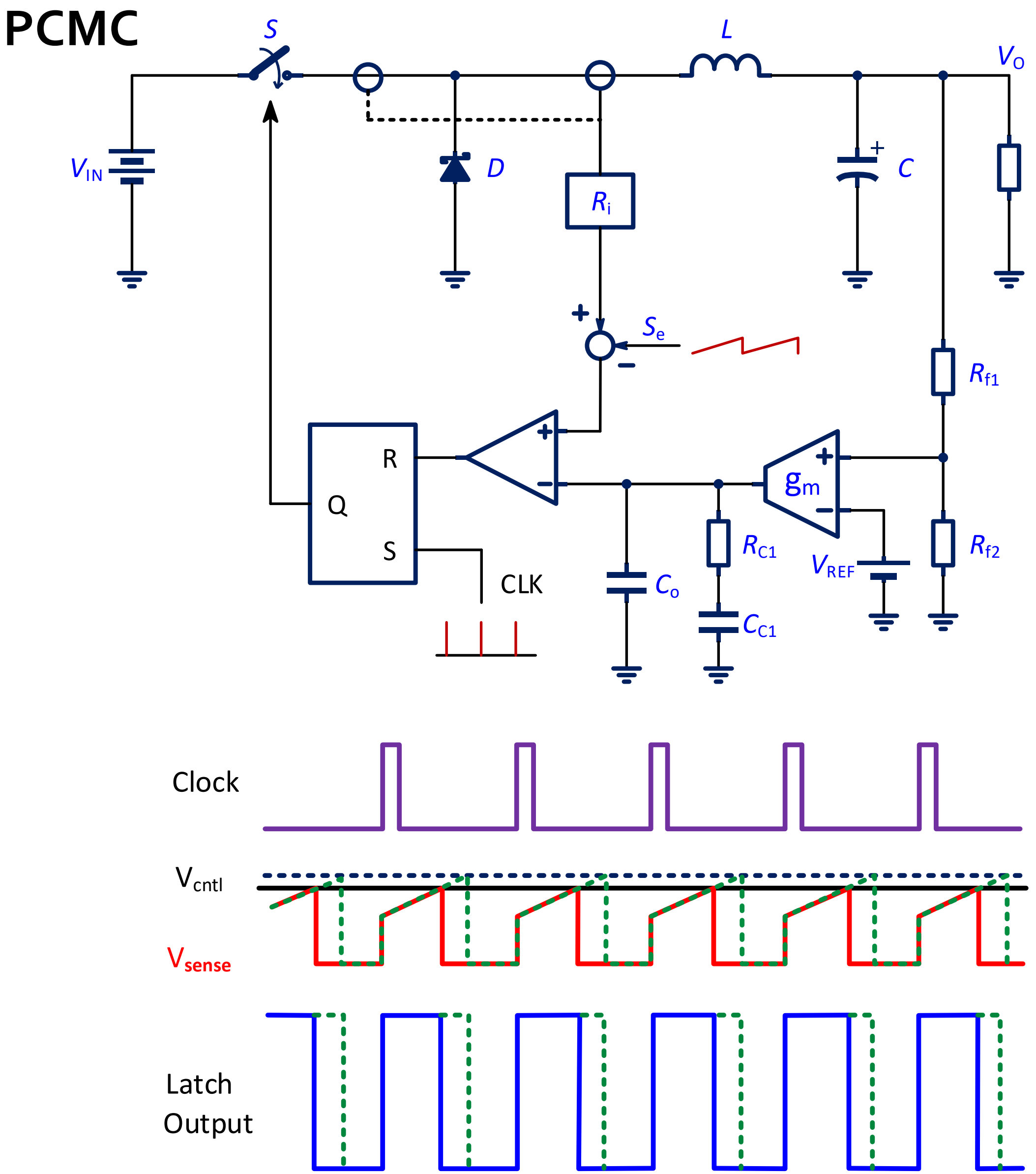
Constant OFF Time Control



Hysteretic Control

Voltage-Mode-Control vs. Peak-Current-Mode Control





Voltage-Mode-Control vs. Peak-Current-Mode Control

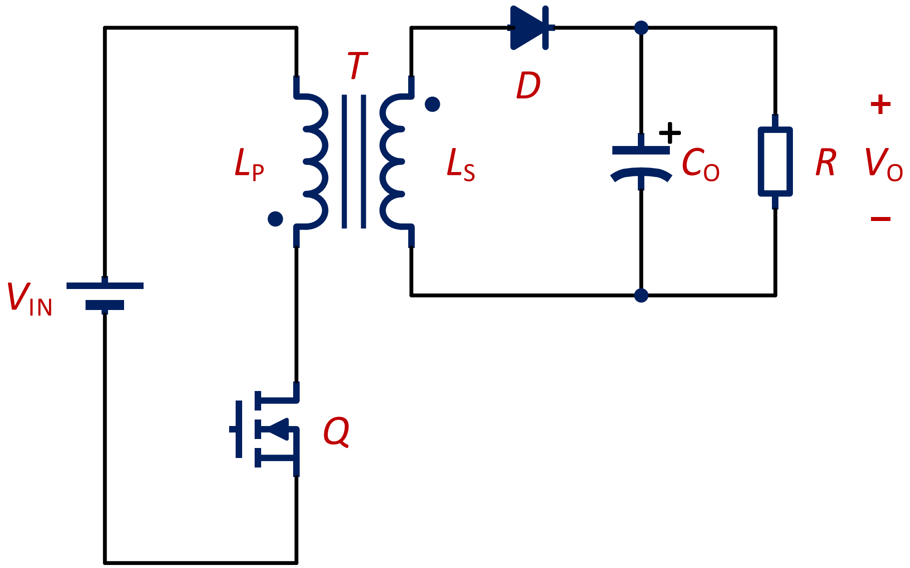
Features of VMC

- Feedback from output voltage to ensure voltage regulation.
- Switching frequency is pre-defined by sawtooth wave.
- Right-Half-Plane Zero limits the crossover bandwidth in boost, buck-boost converters and their derived, such as flyback.
- High noise immunity.

Features of PCMC

- Input voltage feed-forward, good open-loop line regulation
- Optimal large-signal behavior
- No conditional loop stability issues
- Automatic pulse-by-pulse current limiting
- Less complexity / cost
- Subharmonic instability (slope compensation needed)
- Accurate current sensing circuit is needed
- Noise immunity is worse when light load

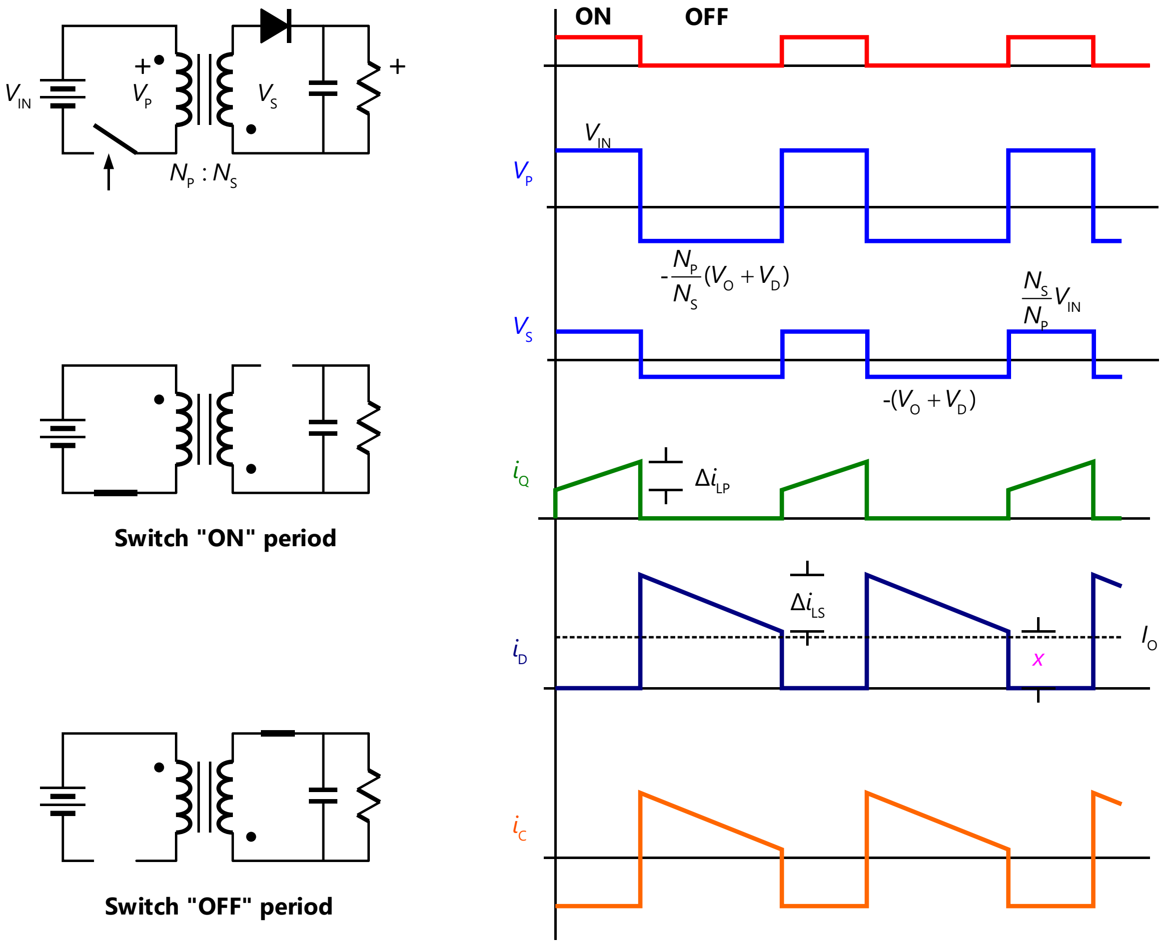
Flyback Converter (I)



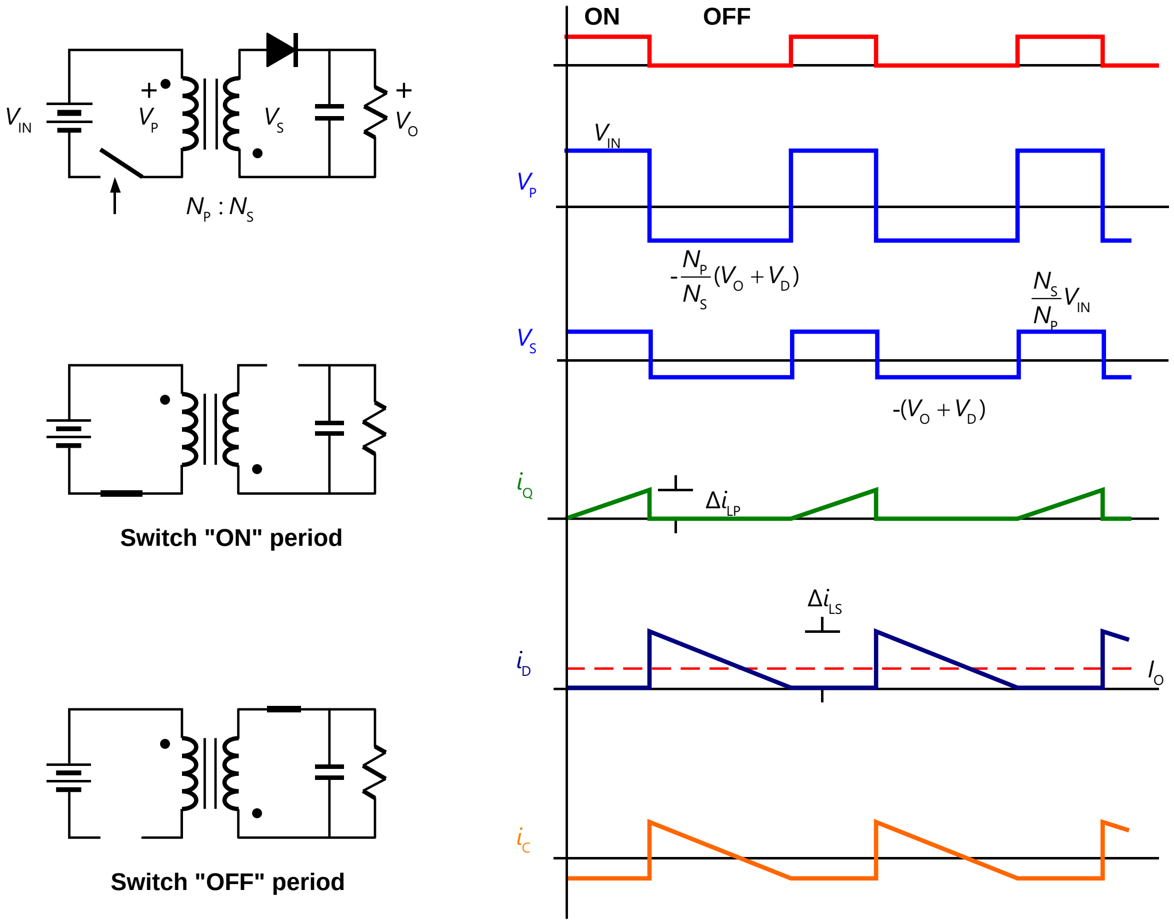
- **Derived from Buck-Boost Converter with Coupled Inductor.**
- **Pulsating Currents in both Input and Output Sides.**
- **Right-Half-Plane-Zero Exists in Control to Output Transfer Function.**
- **Peak-Current-Mode-Control is usually Applied.**
- **Transformer (Coupled-Inductor) Design is similar with Power Inductor.**

Flyback Converter (II)

C.C.M.



D.C.M.



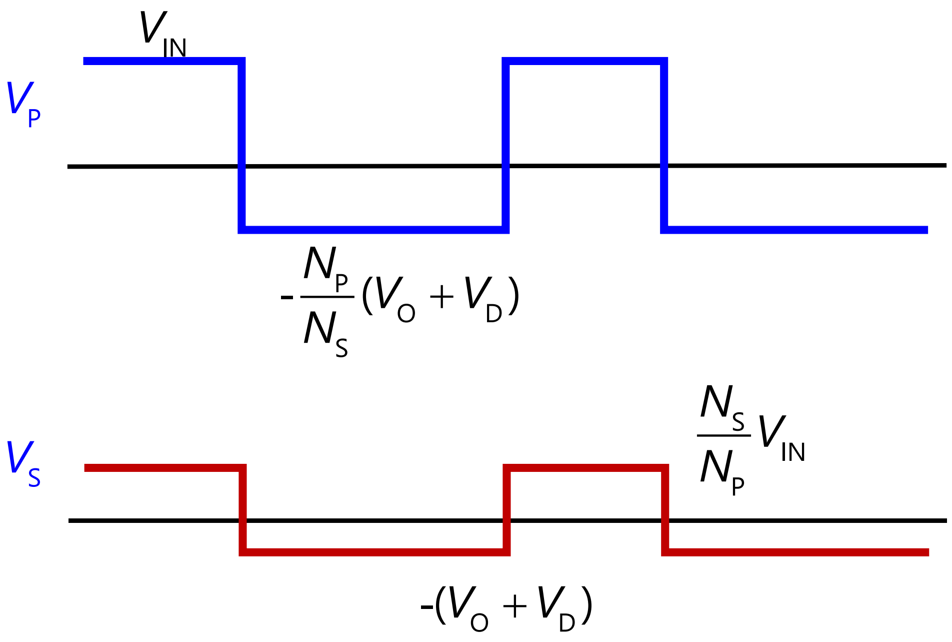
Flyback Converter (III)

Volt-Sec Balance :

$$\frac{N_P}{N_S}\cdot\frac{(V_O+V_D)}{V_{IN}}=\frac{D}{1-D}$$

or

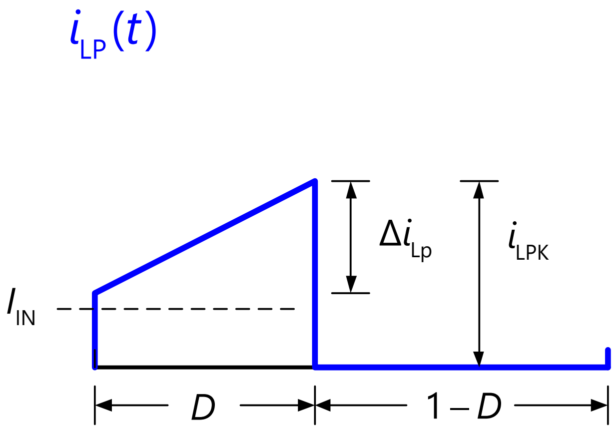
$$D=\frac{\frac{N_P}{N_S}\cdot(V_O+V_D)}{V_{IN}+\frac{N_P}{N_S}\cdot(V_O+V_D)}$$



- **Duty Cycle depends on input and output voltage only.**
- **Duty Cycle can be adjusted by transformer turns ratio.**
- **For minimum input voltage, once turns ratio is fixed, the maximum duty cycle is defined.**

Flyback Converter (IV)

Primary Current



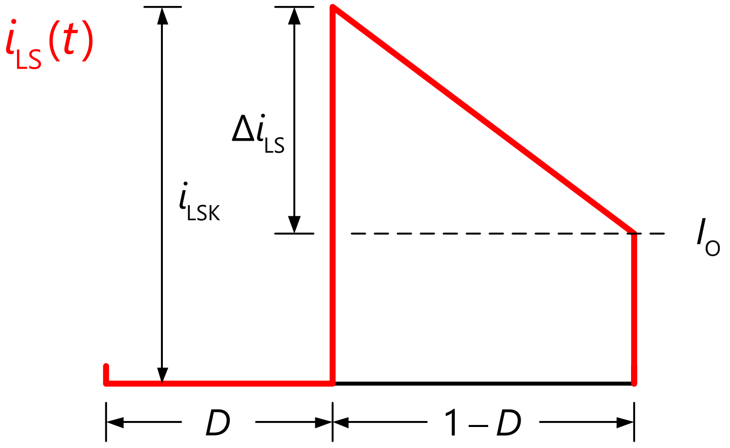
$$\Delta i_{LP} = \frac{V_{IN}}{L_P} \cdot DT_S$$

$$I_Q = I_{IN} = \frac{1}{2} D \cdot (2 i_{LPK} - \Delta i_{LP})$$

$$i_{LPK} = \frac{N_S}{N_P} i_{LSK} \qquad \Delta i_{LP} = \frac{N_S}{N_P} \Delta i_{LS}$$

$$i_{LP,rms} = \sqrt{D \cdot \left[i_{LPK} \cdot \left(i_{LPK} - \Delta i_{LP} \right) + \frac{1}{3} \Delta i_{LP}{}^2 \right]}$$

Secondary Current



$$\Delta i_{LS} = \frac{(V_O + V_D)}{L_S} \cdot (1 - D) T_S$$

$$I_D = I_O = \frac{1}{2} (1 - D) \cdot (2 i_{LSK} - \Delta i_{LS})$$

$$I_{IN} = \left(\frac{D}{1 - D} \right) \cdot \frac{N_S}{N_P} I_O$$

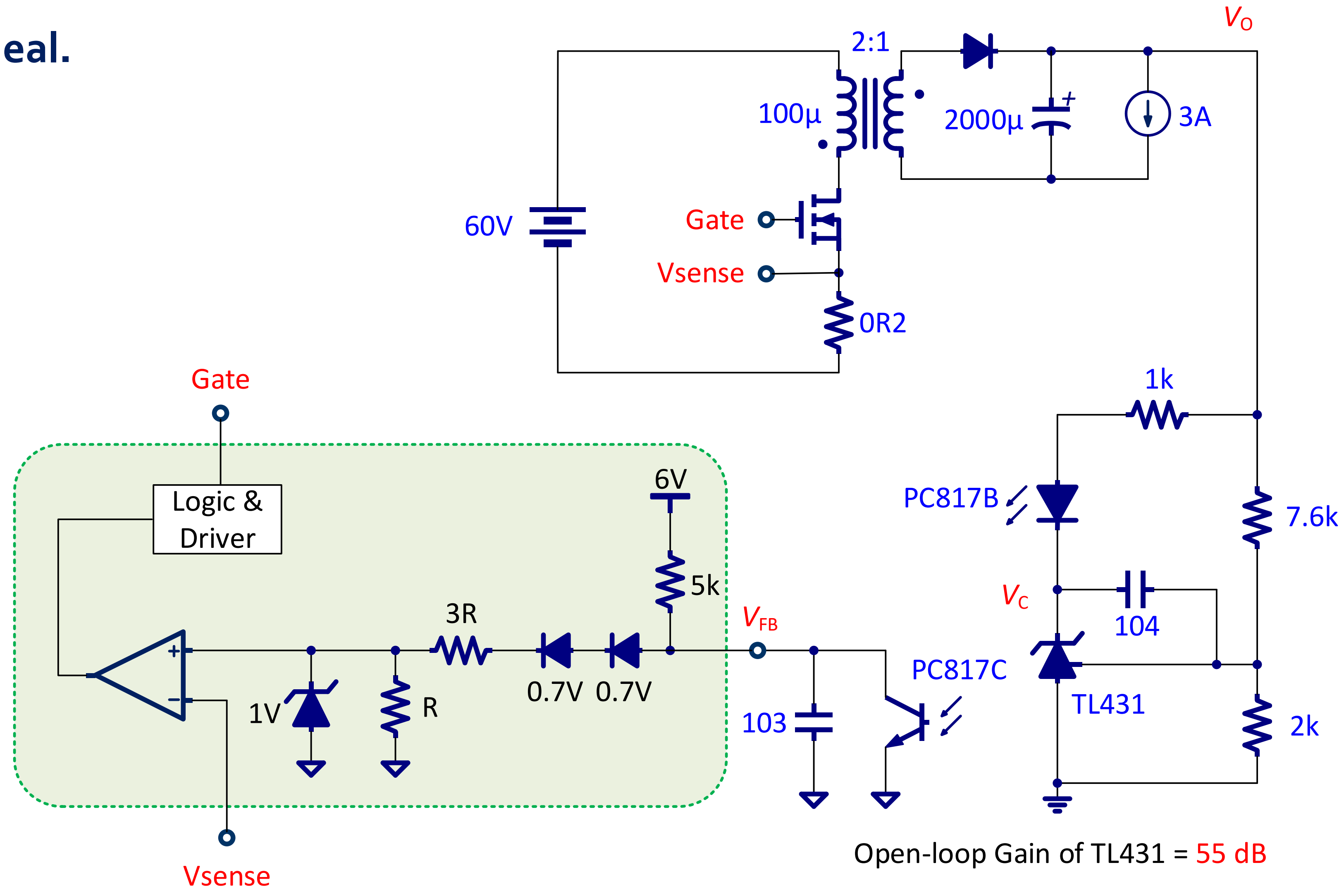
$$i_{LS,rms} = \sqrt{(1 - D) \cdot \left[i_{LSK} \cdot \left(i_{LSK} - \Delta i_{LS} \right) + \frac{1}{3} \Delta i_{LS}{}^2 \right]}$$

DC Analysis (PCMC Flyback)

f_s=100kHz, Q & D are ideal.

CTR of PC817C = 50%

Find V_O, V_C and V_{FB}



Open-loop Gain of TL431 = 55 dB

Operating Point Calculation (I)

$$L_S = \frac{100\mu}{2^2} = 25\mu(\mathrm{H}) \qquad V_O \approx 2.5 \cdot \frac{7.6k + 2k}{2k} = 12(\mathrm{V})$$

Assume C.C.M. operation, calculate duty cycle,

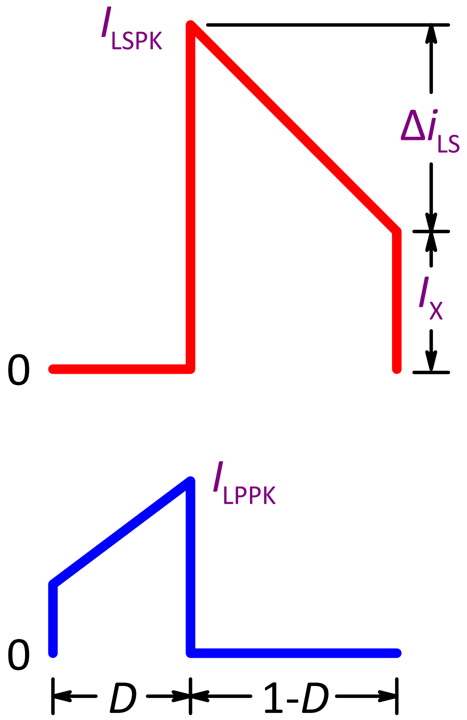
$$D = \frac{nV_O}{(V_{IN} + nV_O)} = \frac{2 \cdot 12}{(60 + 2 \cdot 12)} = 0.286$$

From secondary current,

$$I_O = (2 \cdot I_X + \Delta i_{LS}) \cdot \frac{(1-D)}{2} \quad \text{and} \quad \Delta i_{LS} = \frac{V_O}{L_S} \cdot (1-D) T_S$$

$$\Delta i_{LS} = 3.429(\mathrm{A}) \quad I_X = 2.486(\mathrm{A})$$ (C.C.M. is ensured)

$$\Rightarrow \quad I_{LSPK} = I_X + \Delta_{iLS} = 5.914(\mathrm{A}) \qquad I_{LPPK} = \frac{I_{LSPK}}{n} = 2.957(\mathrm{A})$$



Operating Point Calculation (II)

Sensing voltage : $V_{SENSE} = I_{LPPK} \cdot R_S = 0.591\left(\mathrm{V}\right)$

From PCMC theory, $V_{SENSE} = \left[V_{FB} - \left(2 \cdot 0.7\right)\right] \cdot \dfrac{R}{4R} \Rightarrow V_{FB} = 3.766\left(\mathrm{V}\right)$

Current in opto-transistor, $I_{TR} = \dfrac{6 - V_{FB}}{5k} = 0.447m\left(\mathrm{A}\right)$

Current in opto-diode, $I_{LED} = \dfrac{I_{TR}}{CTR} = 0.894m\left(\mathrm{A}\right)$

Assume voltage drop on opto-diode is 1V, then

$$V_C = 12 - I_{LED} \cdot 1k - 1 = 10.106\left(\mathrm{V}\right)$$

Open-loop gain of TL431 is 560 (55dB), thus voltage on REF pin is

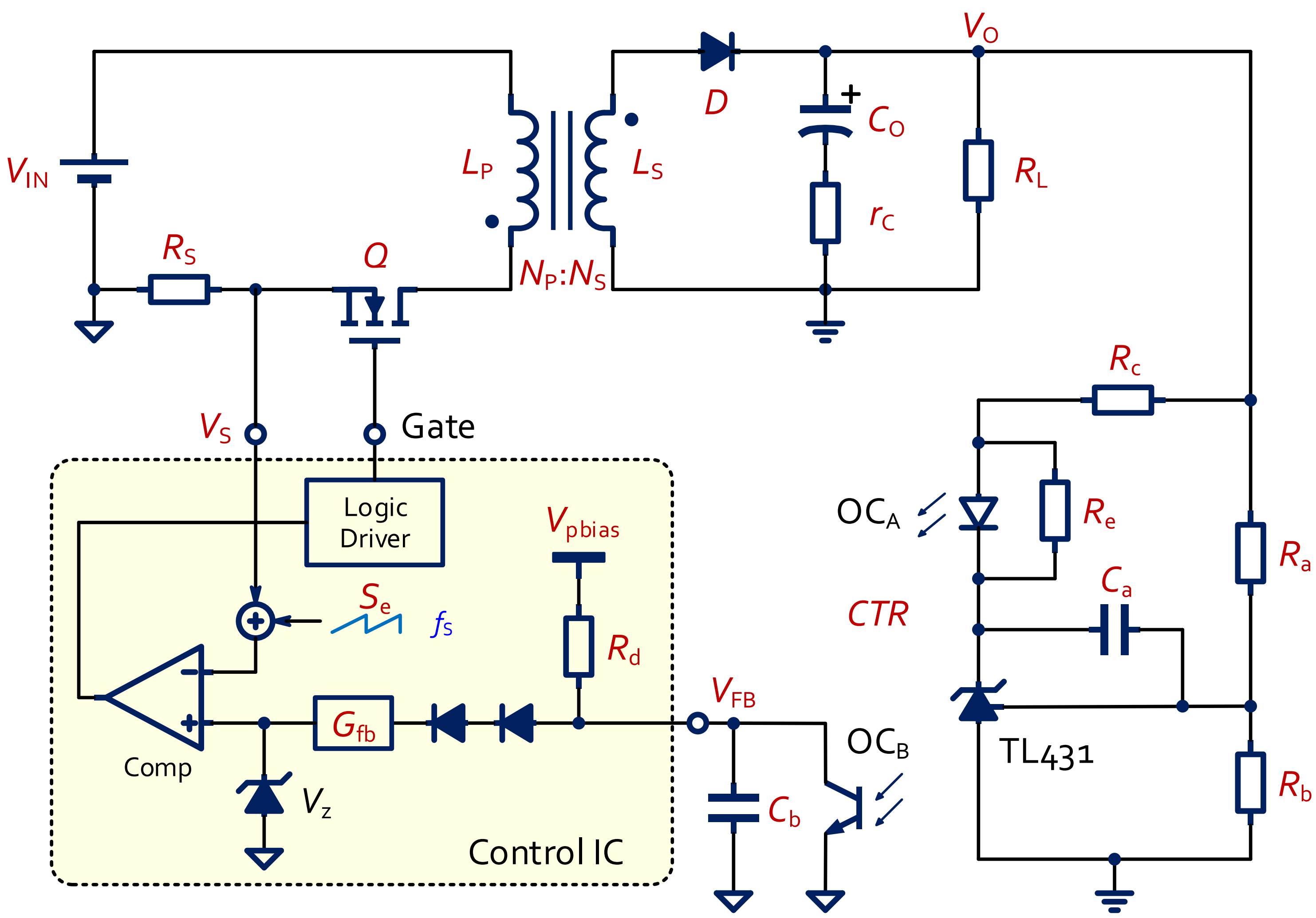
$$V_{REF} = 2.495 - \frac{10.106}{560} = 2.477\left(\mathrm{V}\right)$$

Output voltage, $V_O = 2.477 \cdot \dfrac{7.6k + 2k}{2k} = 11.889\left(\mathrm{V}\right)$

Off-line Flyback Converter

- Right-Half-Plane-Zero → Peak-Current-Mode Control
- Subharmonic Instability for D > 0.5
- Slope Compensation is needed for D > 0.5
- Primary-side Controller, Secondary-side Output
- Opto-coupler is often adopted
- Shunt Regulator (TL431) acts role of Error Amp + V_{REF}
- Type II Compensator Implementation
- Parasitics of Opto-Coupler Issue

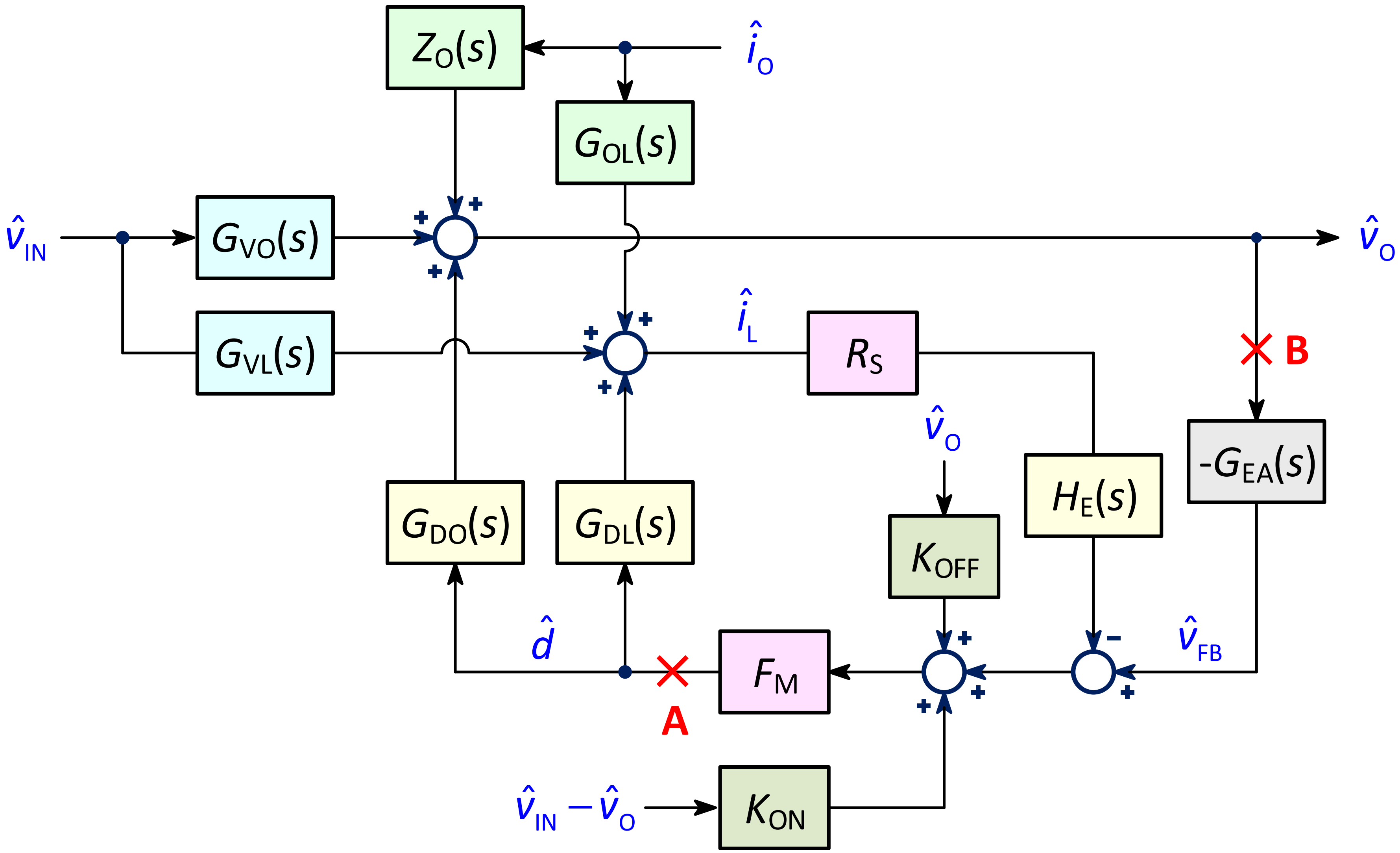
PCMC Flyback Controller



- PWM / PFM
- Slope Compensation
- No Error Amplifier and Reference

Shunt Regulator + Optocoupler

Small-Signal Model for PCMC Converters



Small-Signal Transfer Functions of C.C.M. Flyback Converter

$G_{DO}(s)$	$\frac{\hat{v}_O}{\hat{d}}$	$\frac{N_S}{N_P}\cdot\frac{V_{IN}\cdot(1+s\cdot C_O\cdot r_C)\cdot\left[1-s\cdot\frac{D\cdot L_P}{R_L\cdot(1-D)^2}\cdot\left(\frac{N_S}{N_P}\right)^2\right]}{s^2\cdot\left(\frac{N_S}{N_P}\right)^2\cdot L_P\cdot C_O+s\cdot\left[\frac{L_P}{R_L}\cdot\left(\frac{N_S}{N_P}\right)^2+C_O\cdot r_C\cdot(1-D)^2\right]+(1-D)^2}$
$G_{DL}(s)$	$\frac{\hat{i}_L}{\hat{d}}$	$\left(\frac{N_S}{N_P}\right)^2\cdot\frac{V_{IN}\cdot(1+D)}{R_L\cdot(1-D)}\cdot\frac{1+s\cdot\frac{C_O\cdot R_L}{1+D}}{s^2\cdot\left(\frac{N_S}{N_P}\right)^2\cdot L_P\cdot C_O+s\cdot\left[\frac{L_P}{R_L}\cdot\left(\frac{N_S}{N_P}\right)^2+C_O\cdot r_C\cdot(1-D)^2\right]+(1-D)^2}$
$G_{VO}(s)$	$\frac{\hat{v}_O}{\hat{v}_{IN}}$	$\frac{N_S\cdot D\cdot(1-D)}{N_P}\cdot\frac{1+s\cdot C_O\cdot r_C}{s^2\cdot\left(\frac{N_S}{N_P}\right)^2\cdot L_P\cdot C_O+s\cdot\left[\frac{L_P}{R_L}\cdot\left(\frac{N_S}{N_P}\right)^2+C_O\cdot r_C\cdot(1-D)^2\right]+(1-D)^2}$
$G_{VL}(s)$	$\frac{\hat{i}_L}{\hat{v}_{IN}}$	$\left(\frac{N_S}{N_P}\right)^2\cdot\frac{D}{R_L}\cdot\frac{1+s\cdot C_O\cdot R_L}{s^2\cdot\left(\frac{N_S}{N_P}\right)^2\cdot L_P\cdot C_O+s\cdot\left[\frac{L_P}{R_L}\cdot\left(\frac{N_S}{N_P}\right)^2+C_O\cdot r_C\cdot(1-D)^2\right]+(1-D)^2}$
$Z_O(s)$	$\frac{\hat{v}_O}{\hat{i}_O}$	$\left(\frac{N_S}{N_P}\right)^2\cdot\frac{s\cdot L_P\cdot(1+s\cdot C_O\cdot r_C)}{s^2\cdot\left(\frac{N_S}{N_P}\right)^2\cdot L_P\cdot C_O+s\cdot\left[\frac{L_P}{R_L}\cdot\left(\frac{N_S}{N_P}\right)^2+C_O\cdot r_C\cdot(1-D)^2\right]+(1-D)^2}$
$G_{OL}(s)$	$\frac{\hat{i}_L}{\hat{i}_O}$	$-\frac{N_S\cdot(1-D)}{N_P}\cdot\frac{1+s\cdot C_O\cdot r_C}{s^2\cdot\left(\frac{N_S}{N_P}\right)^2\cdot L_P\cdot C_O+s\cdot\left[\frac{L_P}{R_L}\cdot\left(\frac{N_S}{N_P}\right)^2+C_O\cdot r_C\cdot(1-D)^2\right]+(1-D)^2}$

K_{ON}		$-\frac{D\cdot T_S\cdot R_S}{L_P}\cdot\left(1-\frac{D}{2}\right)$
K_{OFF}		$\frac{(1-D)^2\cdot T_S\cdot R_S}{2\cdot L_P}$
F_M	$\frac{\hat{d}}{\hat{v}_{FB}}$	$\frac{1}{(S_N+S_E)\cdot T_S}$
$H_E(s)$		$\frac{s\cdot T_S}{e^{s\cdot T_S}-1}$
G_{FB}		Constant Gain
$G_{COMP}(s)$	$\frac{\hat{v}_{FB}}{\hat{v}_O}$	To be Designed
$H_E(s)\approx 1-\frac{s}{\omega_n\cdot\frac{2}{\pi}}+\frac{s^2}{\omega_n{}^2}$ $\quad\omega_n=\frac{\pi}{T_S}$		

- **Small-signal model is DC operating point dependent.**

Control to Output Transfer Function of PCMC Flyback

V_{FB} **to Output :**

$$\frac{\hat{v}_O(s)}{\hat{v}_{FB}(s)}=\frac{G_{FB}\cdot F_M\cdot G_{DO}(s)}{1+F_M\cdot\left[R_S\cdot H_E(s)\cdot G_{DL}(s)-K_{OFF}\cdot G_{DO}(s)\right]}$$

Approximated :

$$\frac{\hat{v}_O(s)}{\hat{v}_{FB}(s)}\approx G_{DC}\cdot\frac{\left(1+\frac{s}{\omega_Z}\right)\cdot\left(1-\frac{s}{\omega_{ZRHP}}\right)}{1+\frac{s}{\omega_P}}\cdot\frac{1}{1+\frac{s}{\omega_n\cdot Q_p}+\frac{s^2}{\omega_n^{\ 2}}}$$

Dr. Ray Ridley, “A Small-Signal Model for Current Mode Control”

$$G_{DC}=\frac{R_L}{R_S}\cdot\frac{G_{FB}}{\left(\frac{1+D}{1-D}\right)\cdot\frac{N_S}{N_P}+\frac{R_L\cdot T_S}{L_P}\cdot m_C\cdot(1-D)^2\cdot\left(\frac{N_P}{N_S}\right)}$$

$$\omega_P=\frac{1+D}{C_O\cdot R_L}+\frac{m_C\cdot T_S}{L_P\cdot C_O}\cdot\left(\frac{N_P}{N_S}\right)^2\cdot(1-D)^3$$

$$\omega_Z=\frac{1}{C_O\cdot r_C}$$

$$m_C=1+\frac{S_E}{S_N}$$

$$\omega_{ZRHP}=\frac{R_L\cdot(1-D)^2}{L_P\cdot D}\cdot\left(\frac{N_P}{N_S}\right)^2$$

$$\omega_n=\frac{\pi}{T_S}$$

$$Q_P=\frac{1}{\pi\cdot\left[m_C\cdot(1-D)-0.5\right]}$$

Transfer Functions

Definitions

$D =$ duty cycle

$f_S =$ switching frequency

$M = \dfrac{n \cdot V_O}{V_{IN}} =$ conversion ratio

$n = \dfrac{N_P}{N_S} =$ transformer turns ratio

$\tau_L = \dfrac{2 \cdot L_P \cdot f_S}{n^2 \cdot R_L}$

$S_N = \dfrac{V_{IN}}{L_P} \cdot R_S =$ on-time slope, V/sec

$S_E =$ external ramp slope, V/sec

$G_{FB} = \dfrac{\hat{v}_{RS}}{\hat{v}_{FB}} =$ small-signal gain (eg. $1/3$)

Small-Signal Transfer Function of C.C.M. Flyback

- The flyback converter operated in CCM current-mode is a 3rd-order system. It features a low frequency pole ω_{P1}, followed by a double pole located at half the switching frequency.
- These two poles are affected by a quality coefficient, Q_P, that can create subharmonic oscillations in some cases. To prevent this problem, ramp or slope compensation has to be implemented :
- An artificial ramp of S_E slope is injected on the current-sense signal to oppose the duty cycle action and reduce the current-loop gain.

D.C.M. Flyback Converter

V_{FB} **to Output :**

$$\frac{\hat{v}_O(s)}{\hat{v}_{FB}(s)} \approx G_{DC} \cdot \frac{\left(1+\dfrac{s}{\omega_{Z1}}\right)\cdot\left(1-\dfrac{s}{\omega_{ZRHP}}\right)}{\left(1+\dfrac{s}{\omega_{P1}}\right)\cdot\left(1+\dfrac{s}{\omega_{P2}}\right)}$$

$$G_{DC} = V_{IN} \cdot G_{FB} \cdot \sqrt{\frac{f_S \cdot R_L}{2 \cdot L_P}} \cdot \frac{1}{(S_E + S_N)}$$

$$\omega_{P1} = \frac{2}{C_O \cdot R_L}$$

$$\omega_{P2} = \left(\frac{N_P}{N_S}\right)^2 \cdot \frac{R_L}{L_P \cdot (M+1)^2}$$

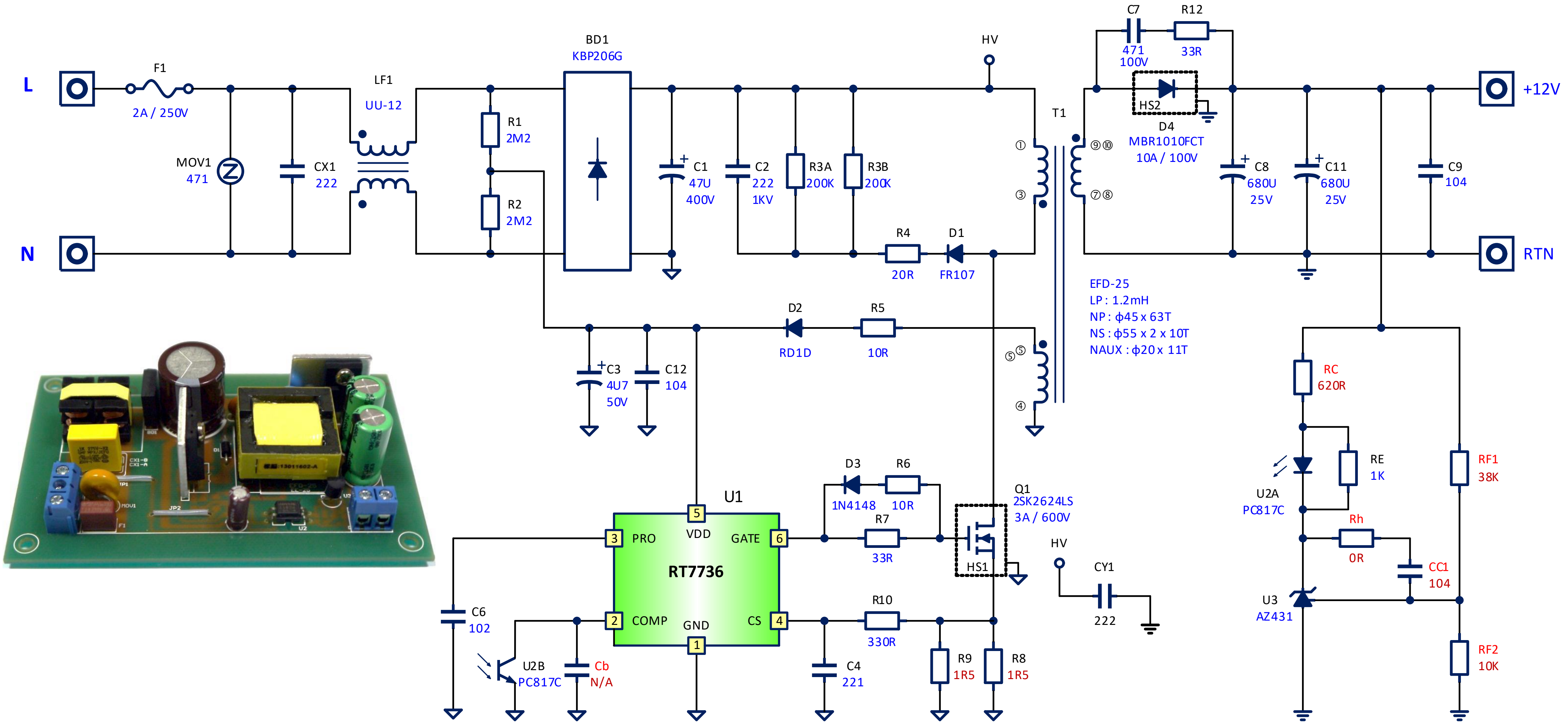
$$\omega_{ZRHP} = \left(\frac{N_P}{N_S}\right)^2 \cdot \frac{R_L}{L_P \cdot M \cdot (M+1)}$$

$$\omega_{Z1} = \frac{1}{C_O \cdot r_C}$$

$$M = \frac{N_P}{N_S} \cdot \frac{V_O}{V_{IN}}$$

- **The flyback converter operated in D.C.M. PCMC features a low frequency pole ω_{P1}, followed by a high-frequency pole ω_{P2}. A RHPZ is also present but its effects are pushed to high frequency portion of the spectrum. Its effects are therefore less sensitive than in C.C.M.. The zero, as in C.C.M., is provided by C_O, and its equivalent series resistor.**

12V/2A Off-Line Flyback Converter



Power Circuit

Engineer's Spec.

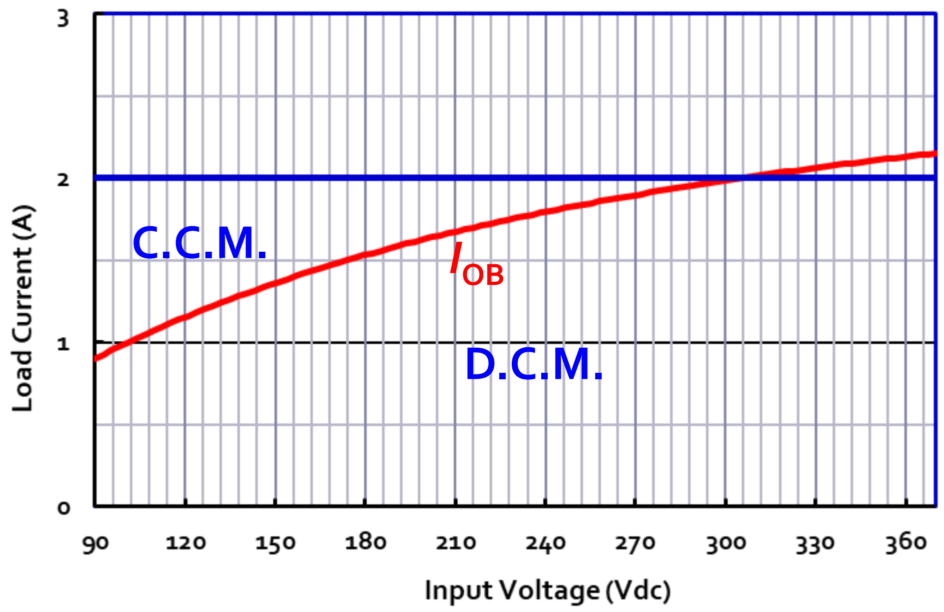
1. Max Duty Cycle @ 90Vdc : $D_{max} = 0.47$
2. I_{OB} @ 90Vdc = 0.9A
3. Peak Flux Density of Flyback Transformer @90Vdc : B_{max} = 0.28 Tesla

Transformer Core : EFD-25 (PC40)

N_P : 63T, N_S : 10T

L_P : 1.2mH, $L_S \approx 30\mu H$

C_O : 680µF x 2 (ESR = 20 mΩ)



Control Circuit

Operating Point V_{IN} = 90Vdc / I_O = 2A

Control IC

Switching Frequency : 65kHz (Frequency Dithering +/- 3k Hz)

External Ramp : 3.33x10^4 V/sec

Sense Resistor : 0.75Ω (OCP concerned)

Power Circuit Transfer Function with Current-Loop Closed

$$G_{DC} = \frac{R_L}{R_S} \cdot \frac{G_{FB}}{\left(\frac{1+D}{1-D}\right) \cdot \frac{N_S}{N_P} + \frac{R_L \cdot T_S}{L_P} \cdot m_C \cdot (1-D)^2 \cdot \left(\frac{N_P}{N_S}\right)} = 4.08 = 12.2\text{dB}$$

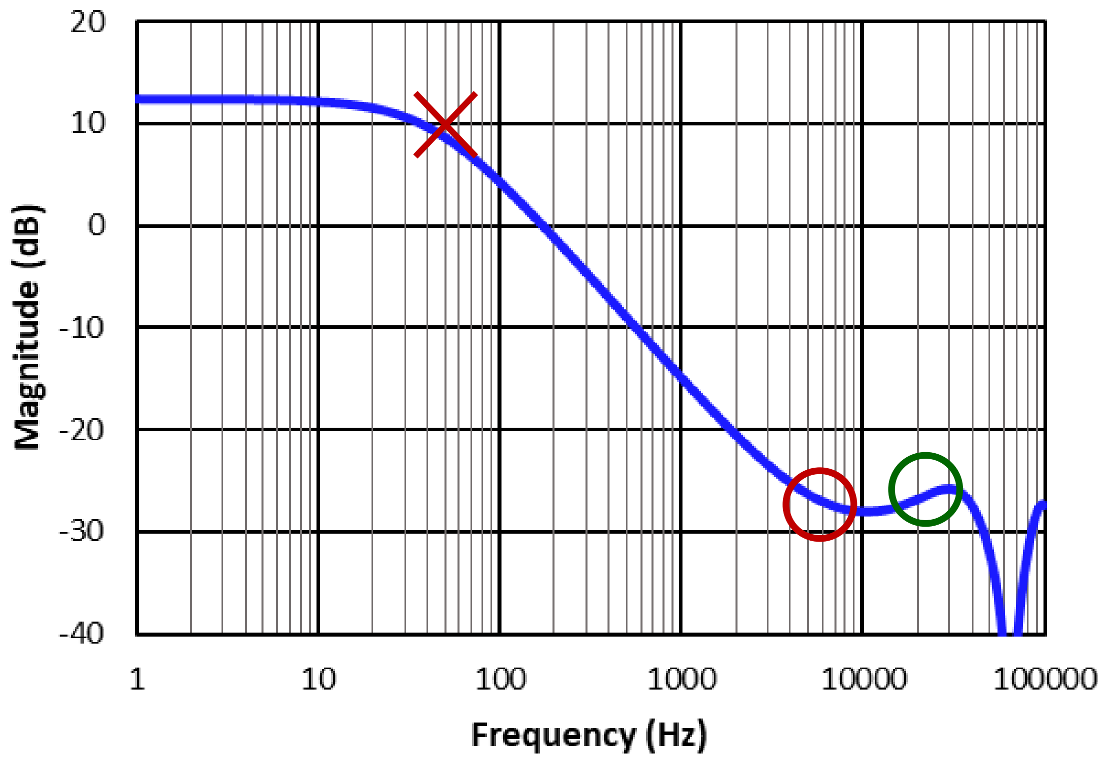
$$\omega_P = \frac{1+D}{C_O \cdot R_L} + \frac{m_C \cdot T_S}{L_P \cdot C_O} \cdot \left(\frac{N_P}{N_S}\right)^2 \cdot (1-D)^3 = 244.1\,(\text{rad}) \qquad f_P = \frac{\omega_P}{2\pi} = 39\,(\text{Hz})$$

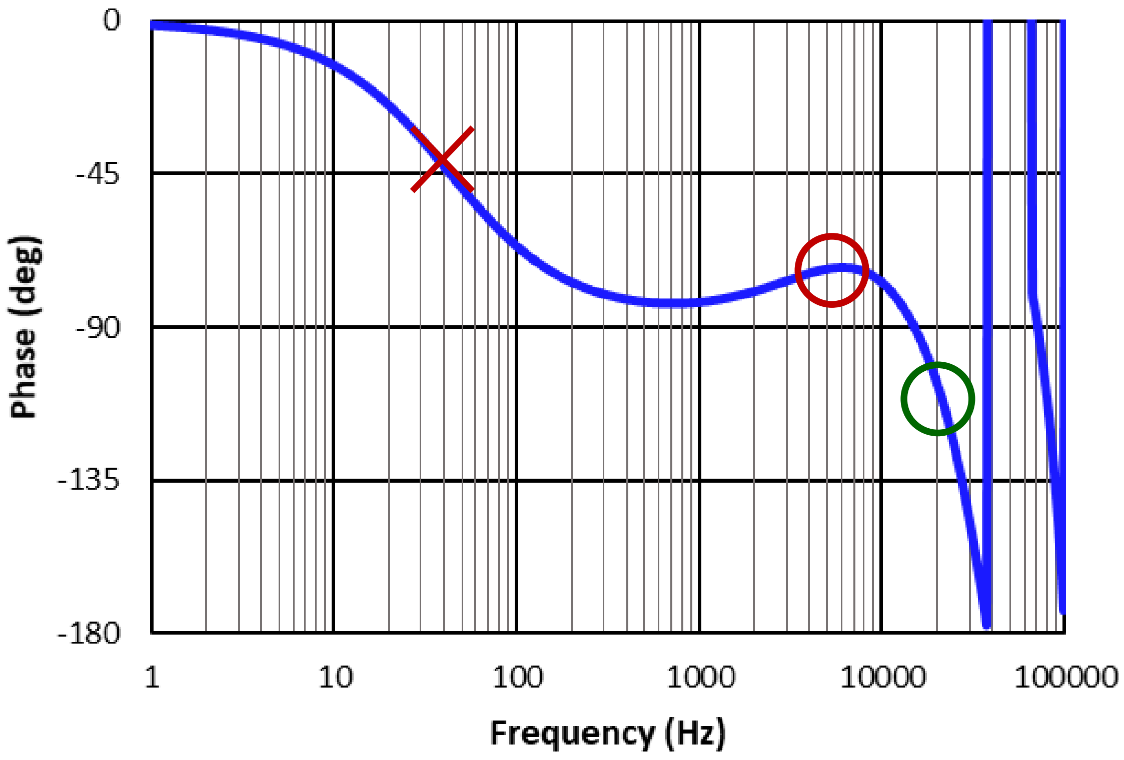
$$\omega_Z = \frac{1}{C_O \cdot r_C} = 3.68k\,(\text{rad}) \qquad f_Z = \frac{\omega_Z}{2\pi} = 5.85k\,(\text{Hz})$$

Control Circuit

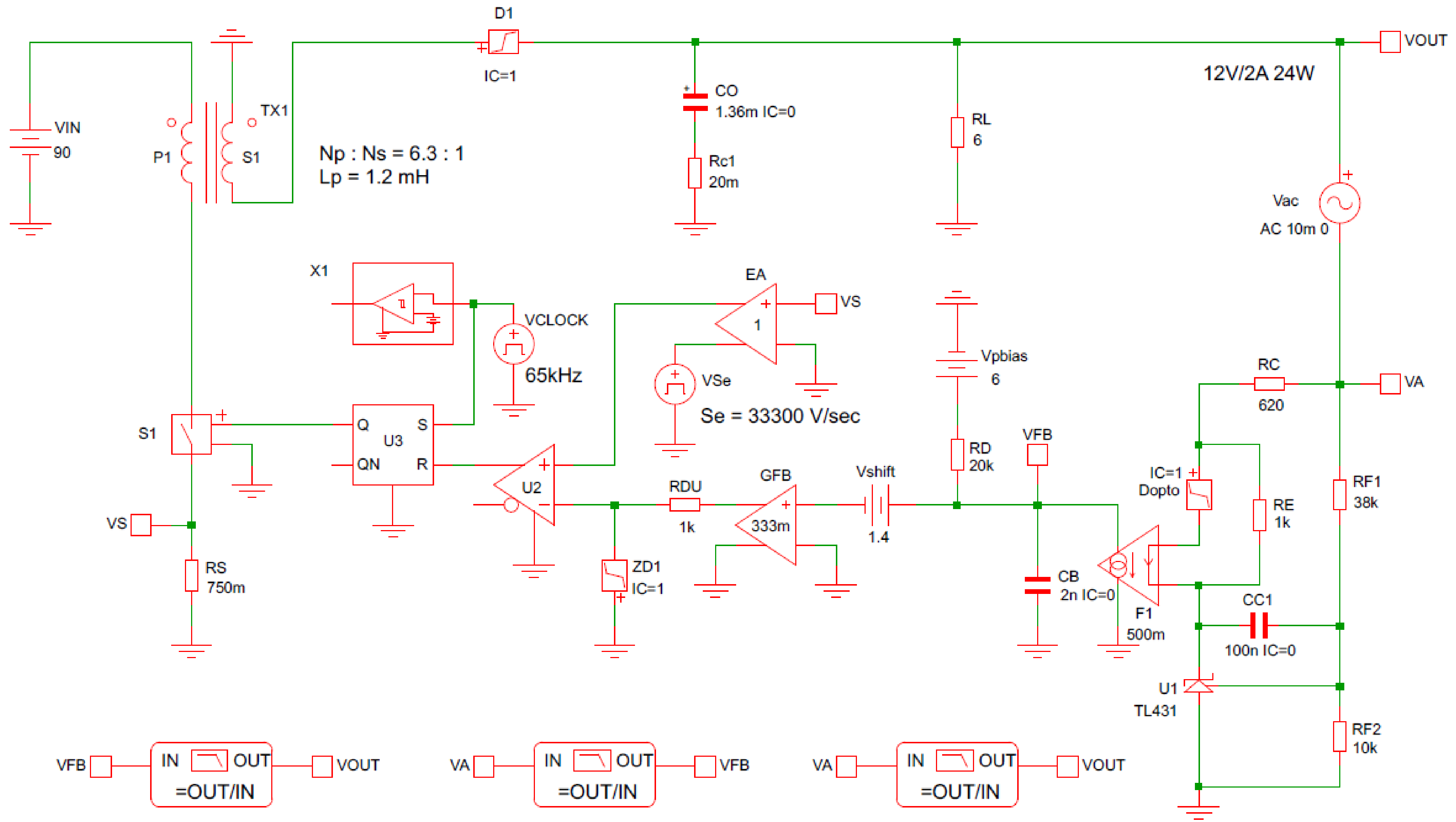
$$\omega_{ZRHP} = \frac{R_L \cdot (1-D)^2}{L_P \cdot D} \cdot \left(\frac{N_P}{N_S}\right)^2 = 128.5k\ (\text{rad}) \qquad f_{RHPZ} = \frac{\omega_{RHPZ}}{2\pi} = 20.4k\ (\text{Hz})$$

$$\omega_n = \frac{\pi}{T_S} = 204.2k\ (\text{rad}) \qquad f_n = \frac{1}{2T_S} = 32.5k\ (\text{Hz}) \qquad Q_P = \frac{1}{\pi \cdot \left[m_C \cdot (1-D) - 0.5\right]} = 0.872$$

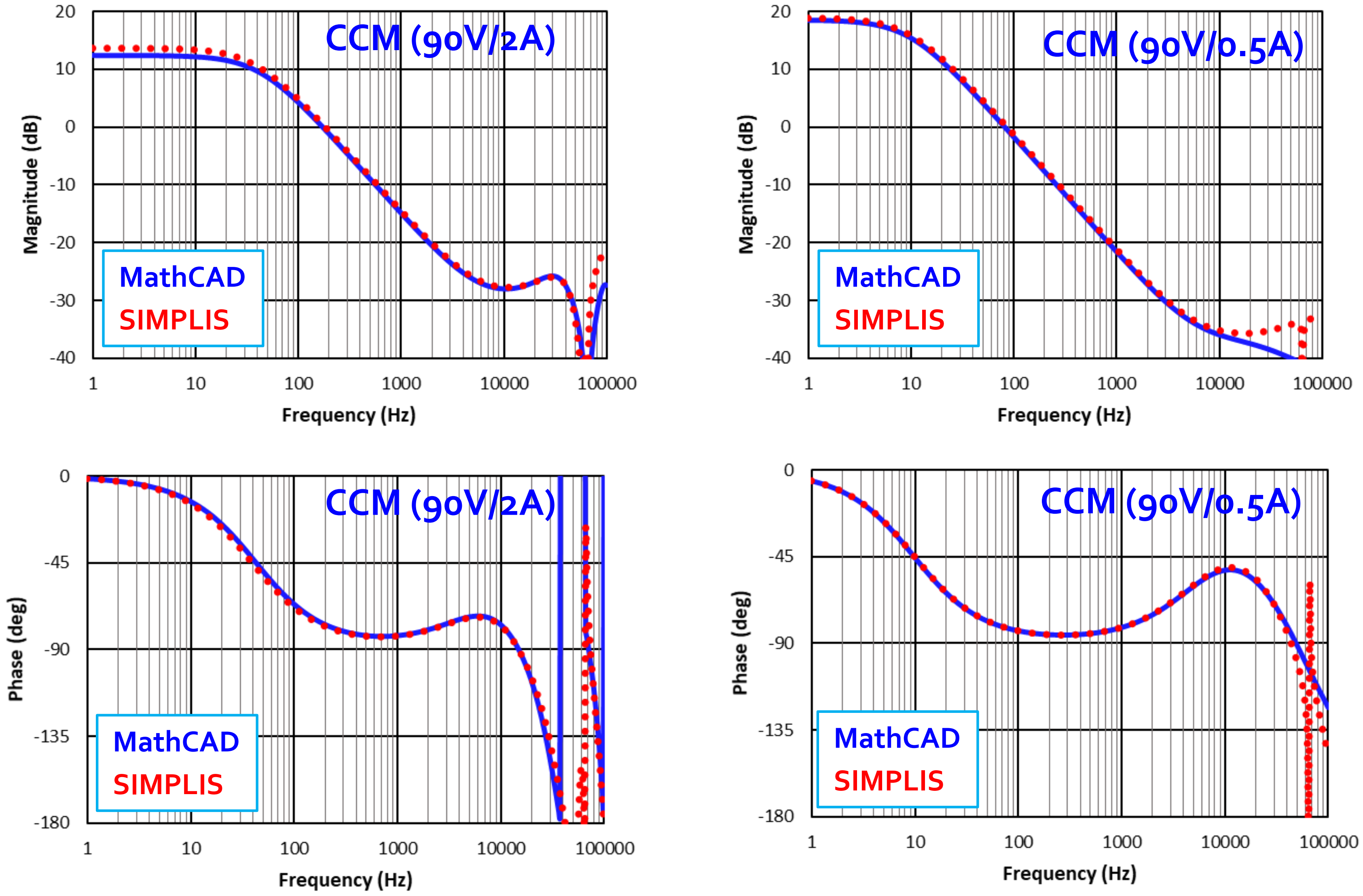




SIMPLIS Simulation Example (12V/2A)



V_{FB} to V_O Transfer Function (with Current-Loop Closed)



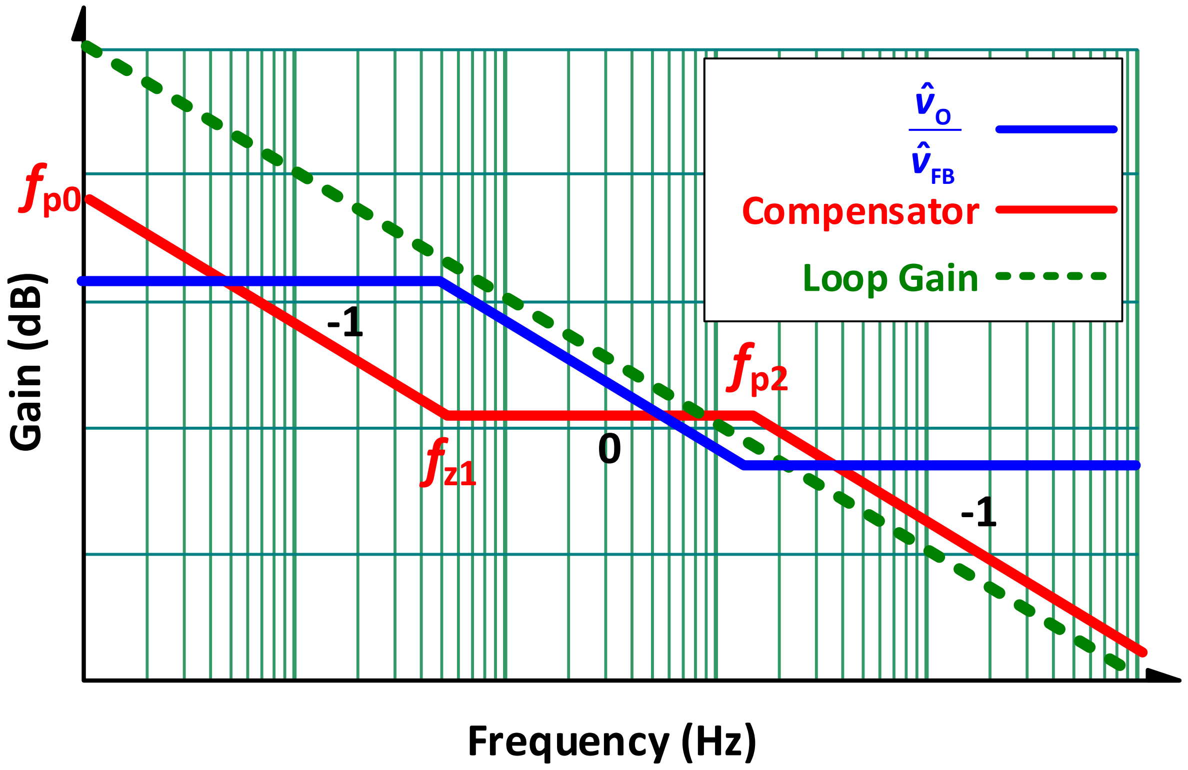
- Operating Point dependent.
- 1P1Z (up to ½ f_S) for both CCM and DCM.

Will Be Back
At 16:10

Time	Topic
16:00-16:10	Break Time
16:10-16:50	返結合光耦和分路穩壓器的返馳電源回授設計– 2 Off-line Flyback Feedback Design with Optocoupler and Shunt Regulator
16:50-17:00	QA
17:00	Lucky Draw

王信雄博士

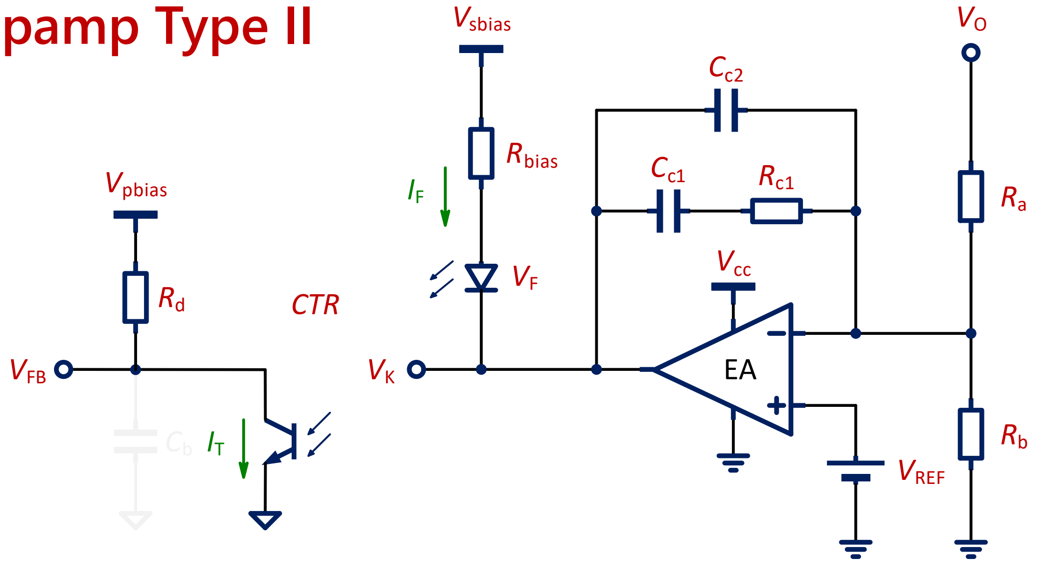
Compensation



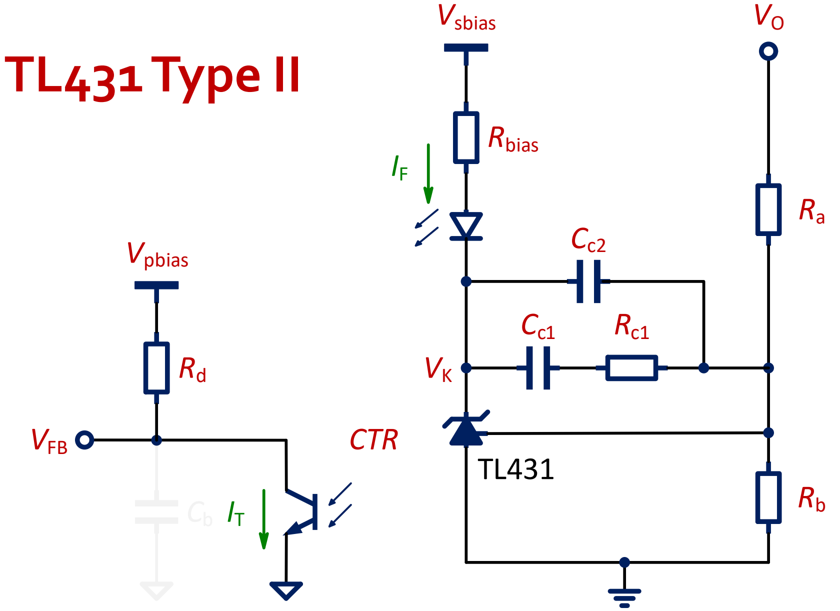
- Generally, a Type II (2P1Z) compensator is adequate for both C.C.M. and D.C.M. flyback.
- Based on an operating point to design the compensator. Pole-Zero placement of K-factor approaches are commonly used.

Isolated Compensating Network

Opamp Type II



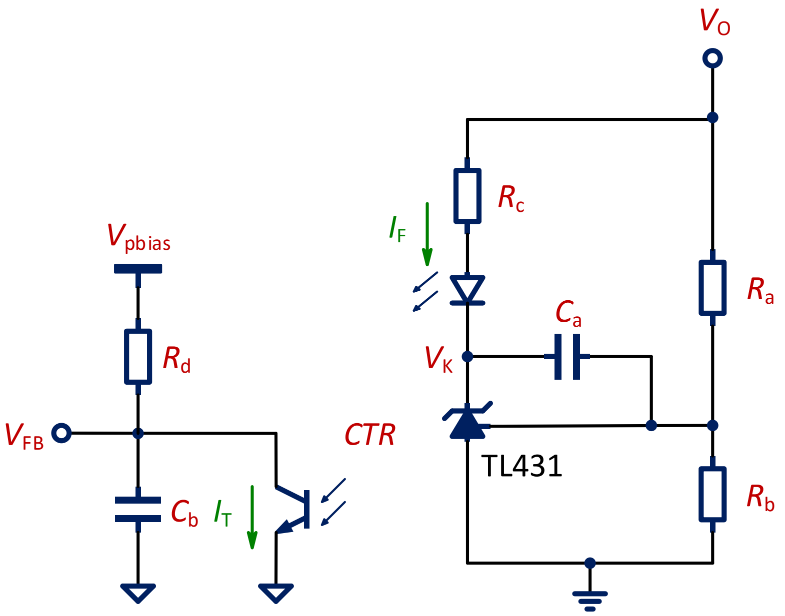
TL431 Type II

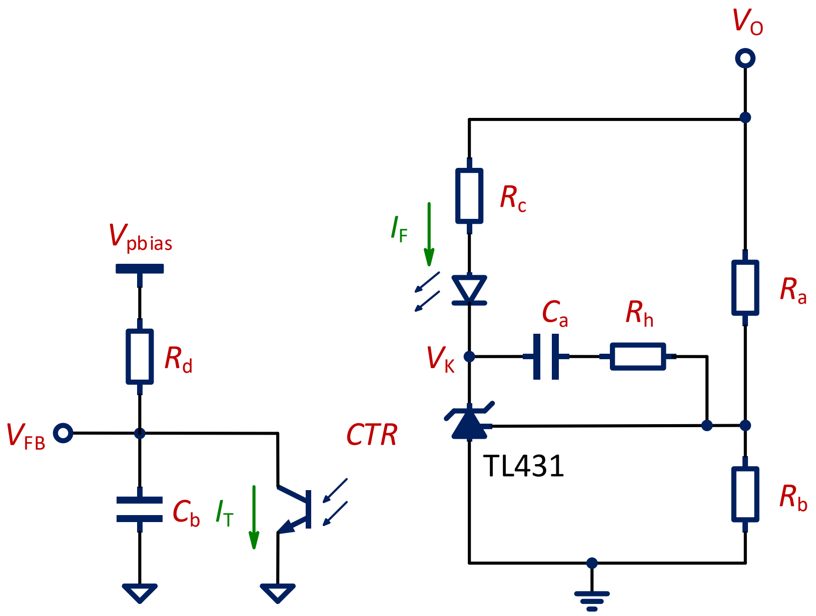


$$G_{comp}(s) = CTR \cdot \frac{R_d}{R_{bias} \cdot R_a (C_{c1} + C_{c2})} \cdot \frac{1 + sR_{c1}C_{c1}}{s \cdot \left(1 + sR_{c1} \cdot \frac{C_{c1}C_{c2}}{C_{c1} + C_{c2}}\right)}$$

- Opamp network with V_{REF} and optocoupler can conceptually fit the requirement.
- A shunt regulator (TL431) with optocoupler is the most commonly adopted for its simplicity and low cost.

Practical Compensator Structure



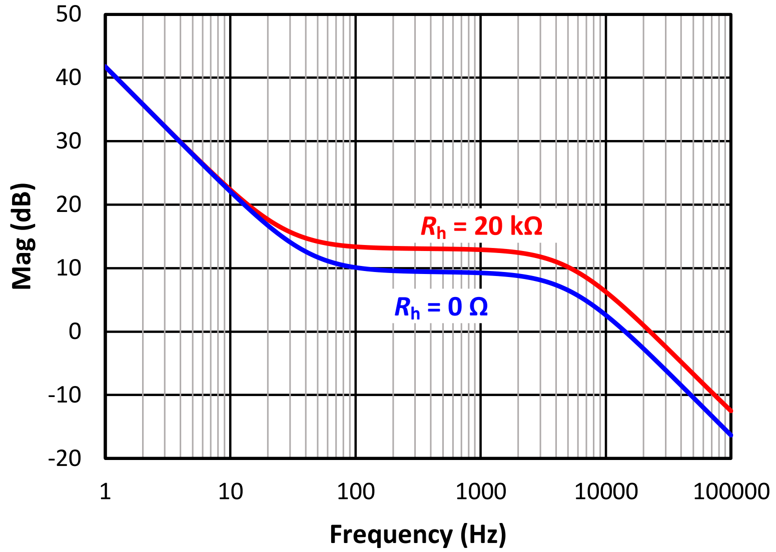


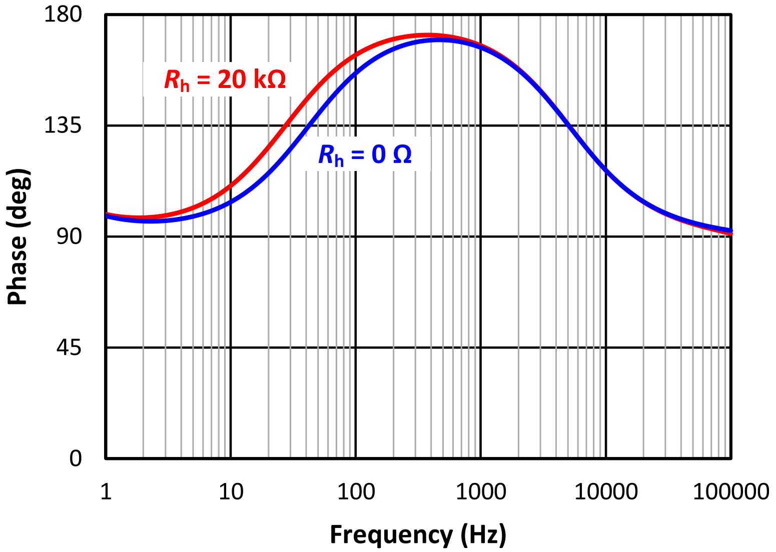
$$G_{COMP}(s) = CTR \cdot \frac{R_d}{R_c} \cdot \frac{1 + sR_aC_a}{sR_aC_a\left(1 + sR_dC_b\right)}$$

$$G_{COMP}(s) = CTR \cdot \frac{R_d}{R_c} \cdot \frac{1 + s\left(R_a + R_h\right)C_a}{sR_aC_a\left(1 + sR_dC_b\right)}$$

- TL431 is powered by output voltage.
- Both two compensating networks have Type II structure.
- The right one has more design degree of freedom.

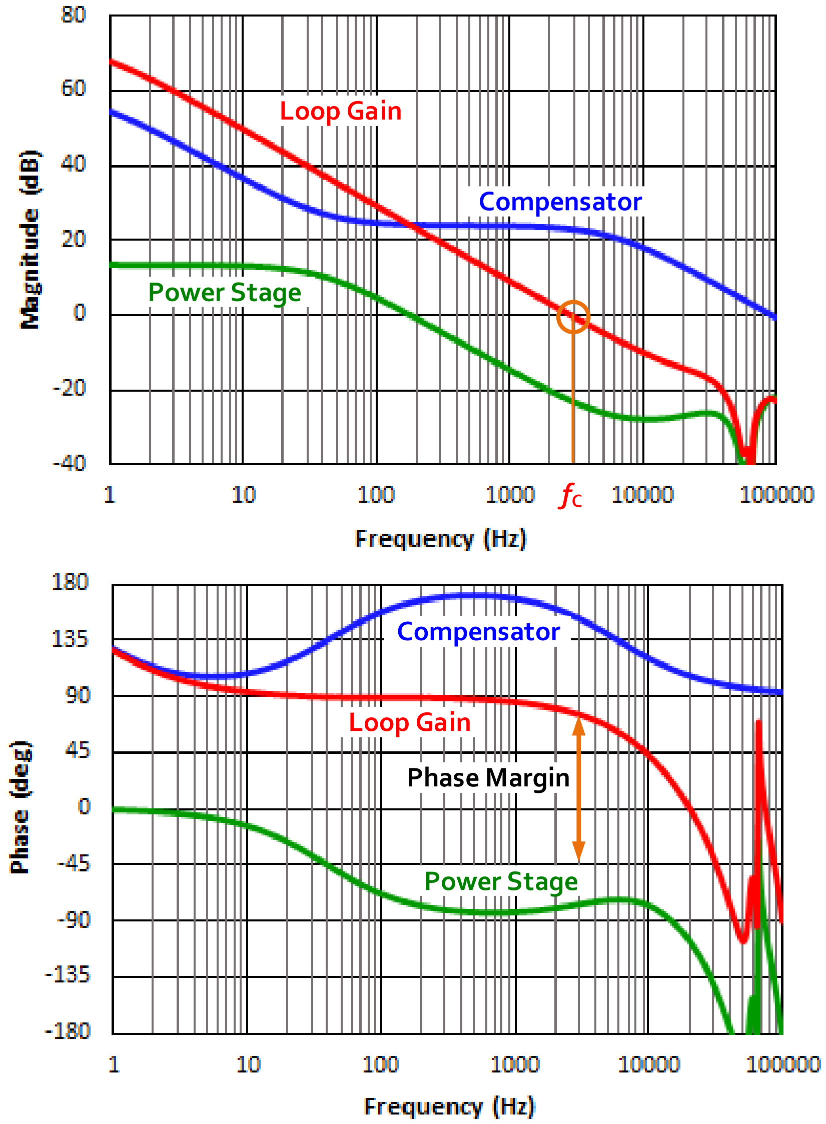
Compensation Network of Flyback Converter





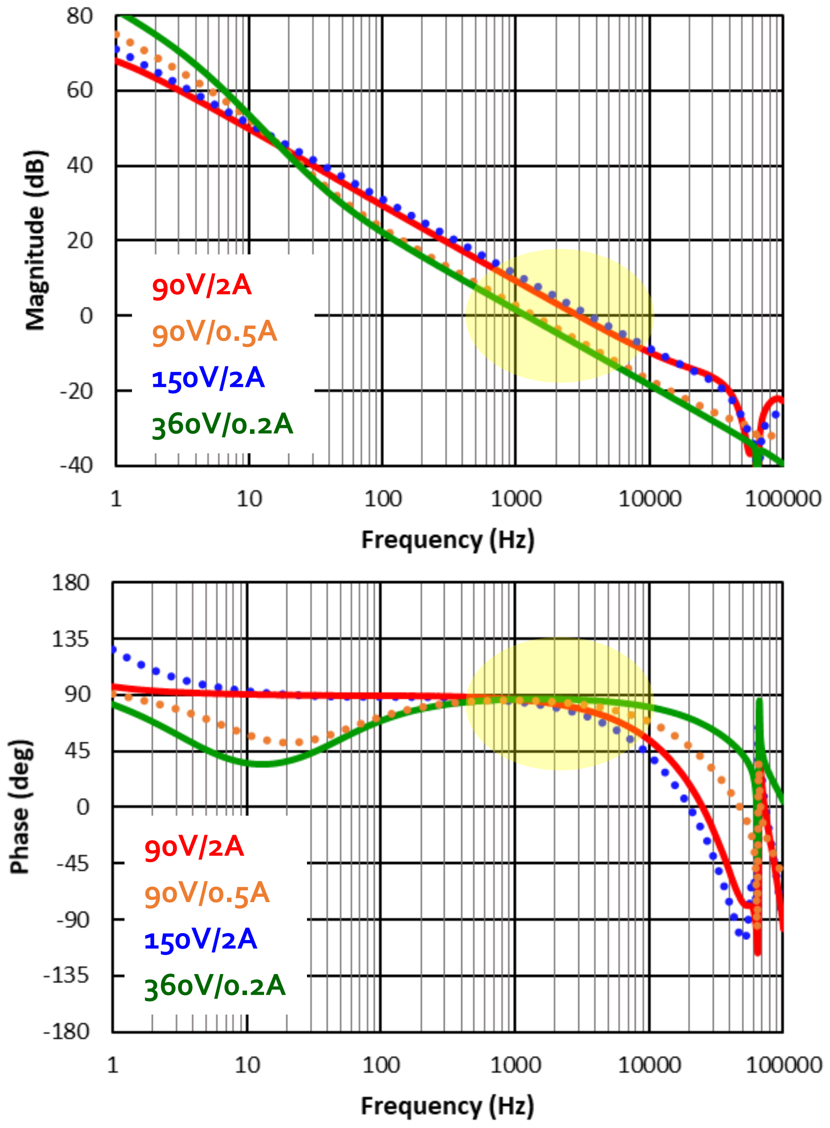
- **The existence of R_h can increase the gain in the middle frequency range.**
- **At the same time, more split the location of pole-zero pair, which changes the phase arising of compensator.**

Flyback Feedback



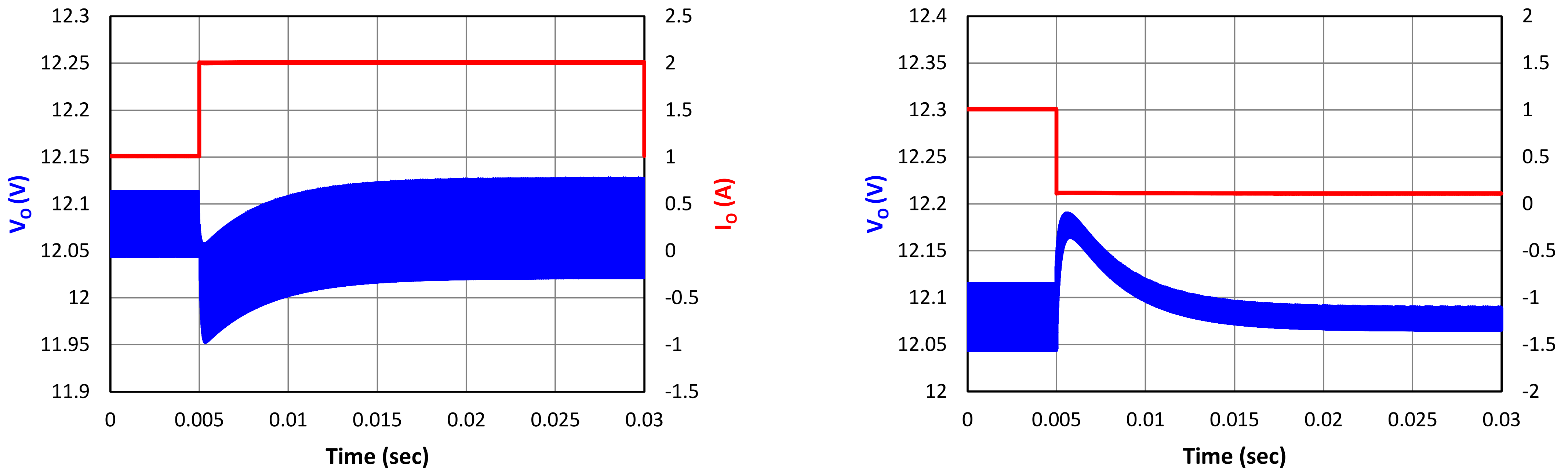
- With proper design of compensator, one can easily achieve very good loop gain with quite high cross-over frequency and phase margin.
- Pole-zero placement (pole-zero cancellation) approach is recommended to obtain -1 slope of loop gain.
- For PCMC, there is no LC peaking in loop gain.
- RHPZ and two-pole at half of switching frequency results in phase drop in high frequency range.
- Due to feedforward characteristics, the input variation only affect little in loop gain.

D.C.M. of Flyback Converter



- Once the converter operates in D.C.M., the crossover frequency will be decreased if same compensator applied.
- Pay more attention to the compensator design based on which operating point. Check every corner to ensure stability.
- In the modern flyback controller, the switching frequency will be decreased in light load condition, which will result in worse frequency response. Adaptive gain design in control IC can mitigate the symptom.

Dynamic Load Change Transient Response



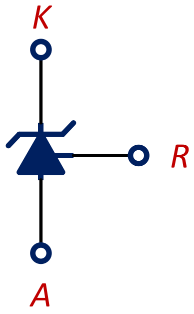
I_O : 1A → 2A

I_O : 1A → 0.1A

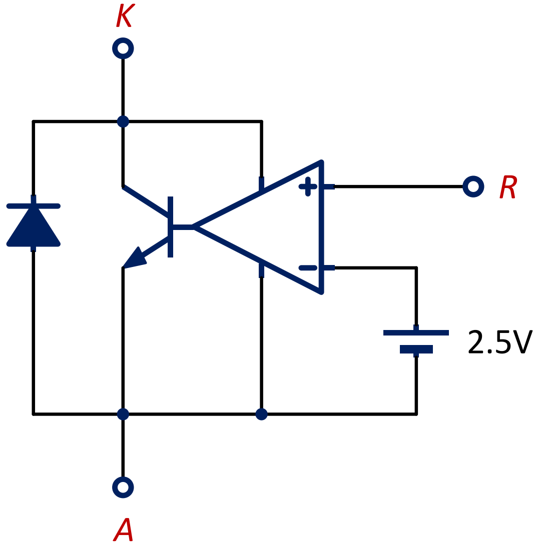
- **Dynamic load change response indicates the discrepancy of target operating points.**
- **Higher over-shoot and slow settling time in D.C.M.**

Shunt Regulator TL431

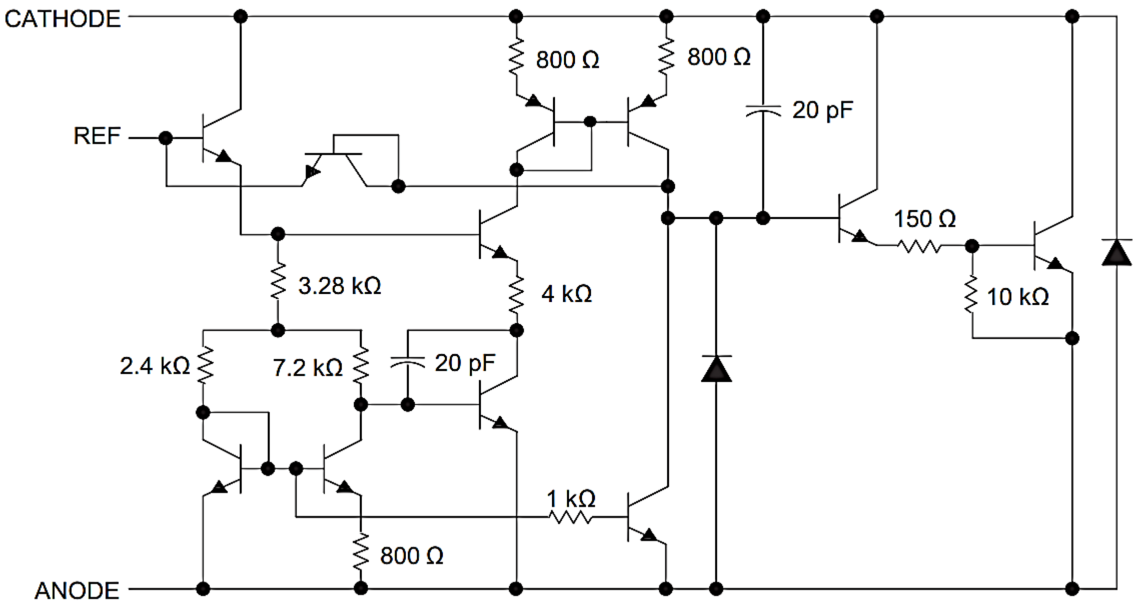
Symbol



Functional Block Diagram



Equivalent Schematics



Reference Voltage

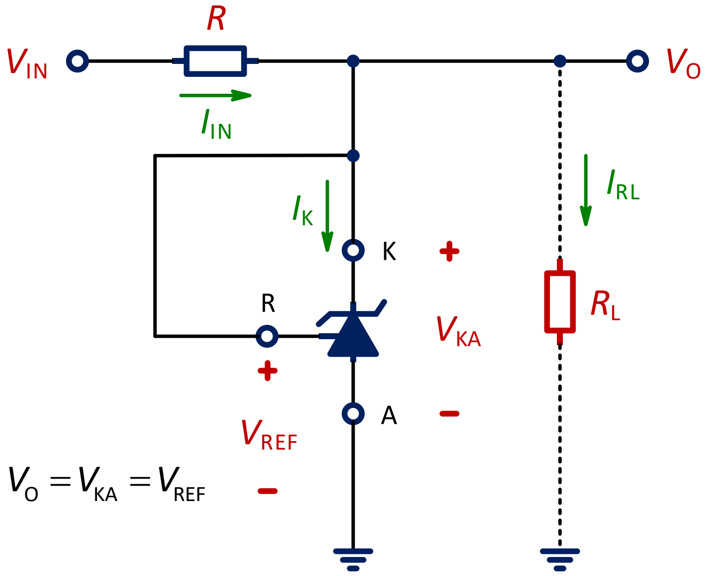
ELECTRICAL CHARACTERISTICS

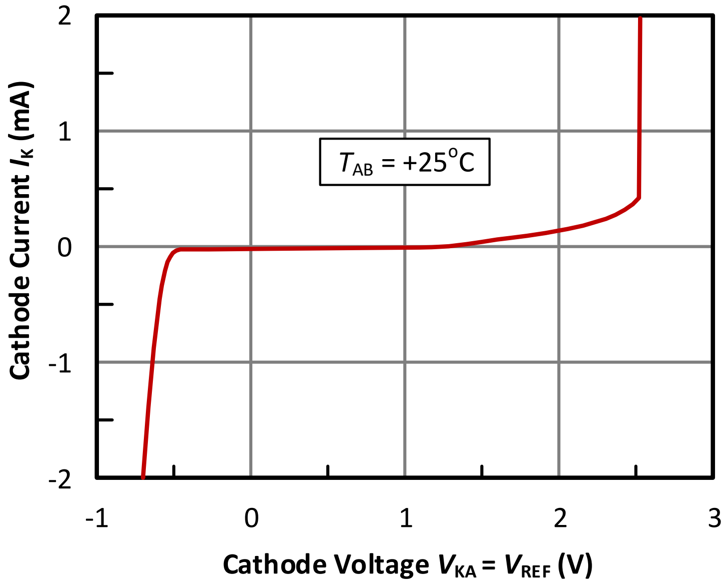
T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	TL431C			TL431AC			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{ref}	Reference Input Voltage $V_{KA} = V_{ref}$, Ik = 10 mA T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$	2.44 2.423	2.495	2.55 2.567	2.47 2.453	2.495	2.52 2.537	V
ΔV_{ref}	Reference Input Voltage Deviation Over-Temperature Range - note 1 V_{KA} = Vref, Ik = 10 mA, $T_{min} \le T_{amb} \le T_{max}$		3	17		3	15	mV

Shunt Regulator TL431

Regulation vs. Cathode Current

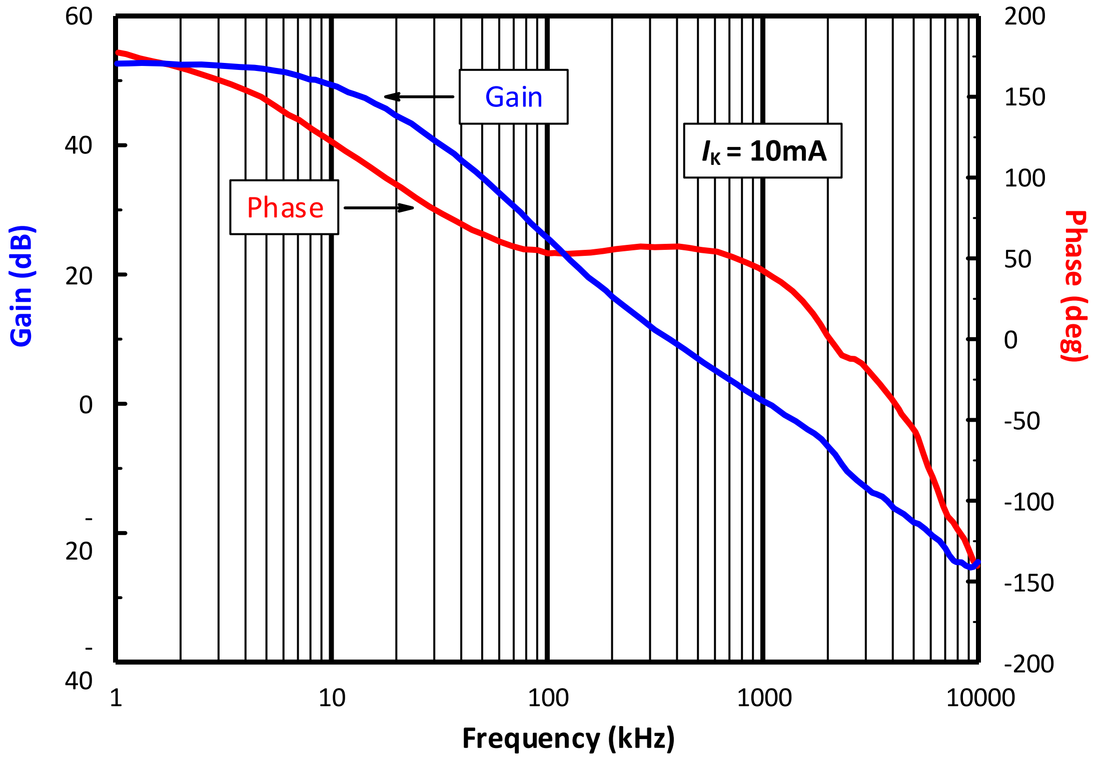


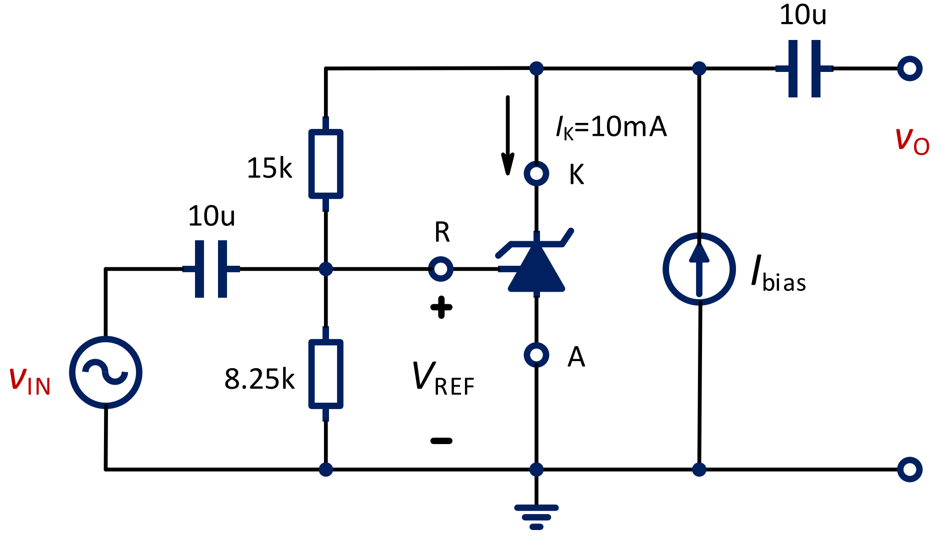


- The cathode current should be higher than **500μA** (depending on spec.) to guarantee the regulation.
- The current flowing into reference pin of TL431 is around 2μA, such that the current on lower voltage divider is chosen as more than 100 times to ensure the accuracy.
- In other words, the lower resistance should be lower than 12.5kΩ.

Frequency-Domain Characteristics of TL431

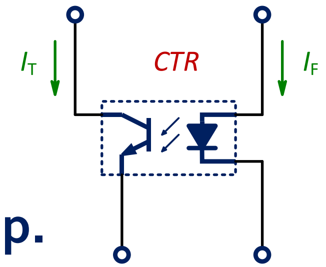
Gain and Phase



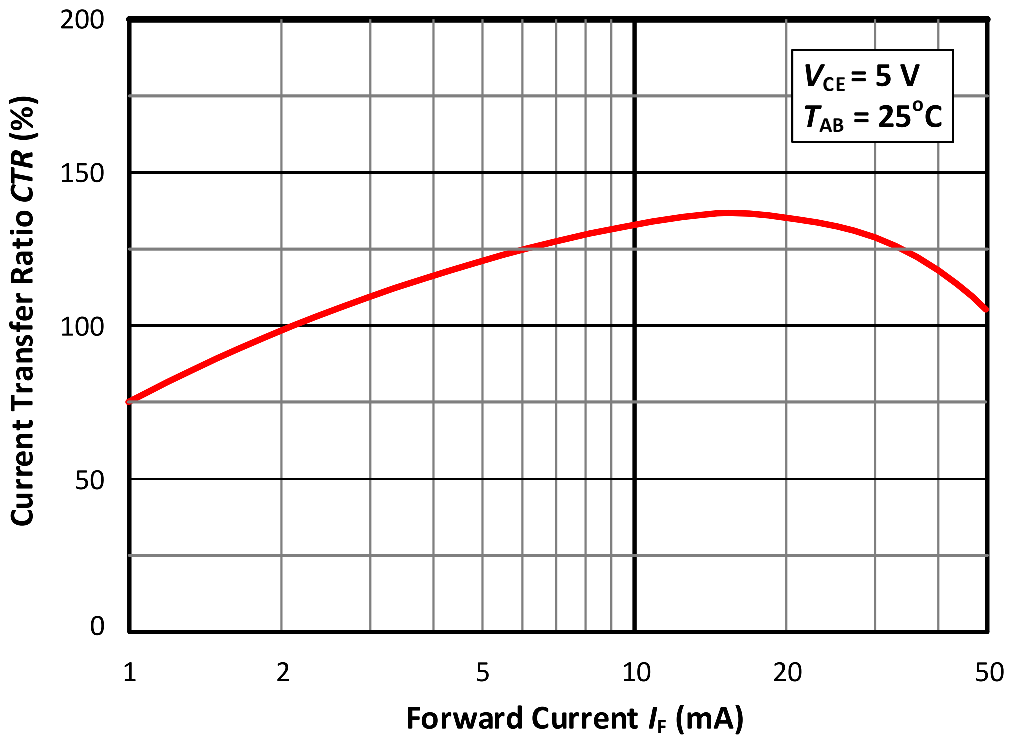


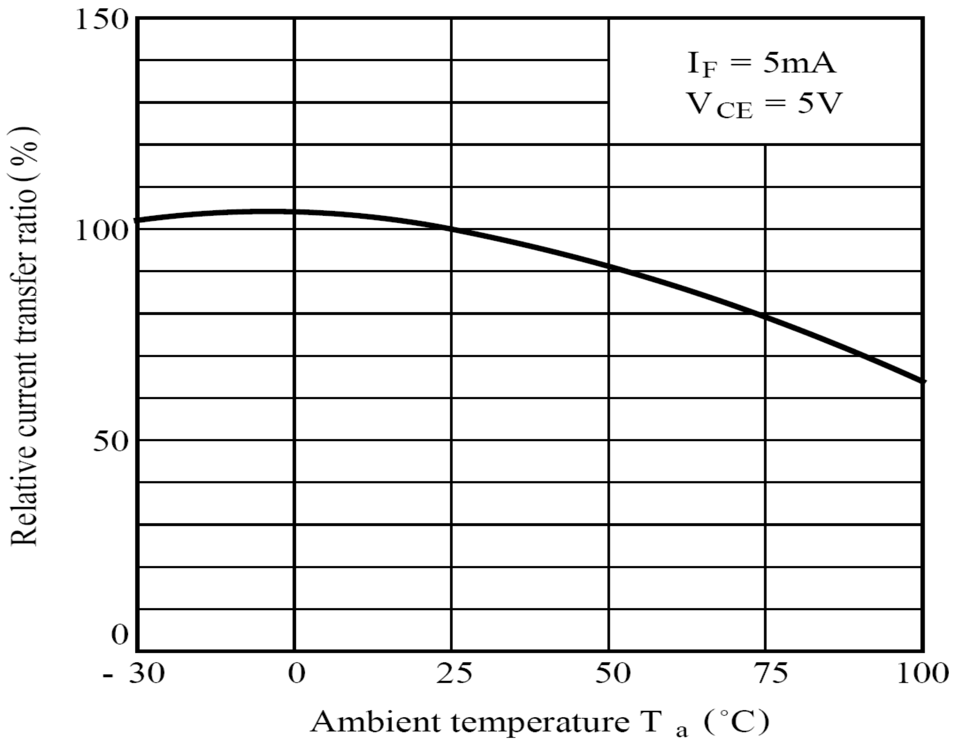
- DC Gain = 53 dB, Pole = 10kHz

Opto-Coupler PC817C



Forward Current vs. CTR vs. Ambient Temp.

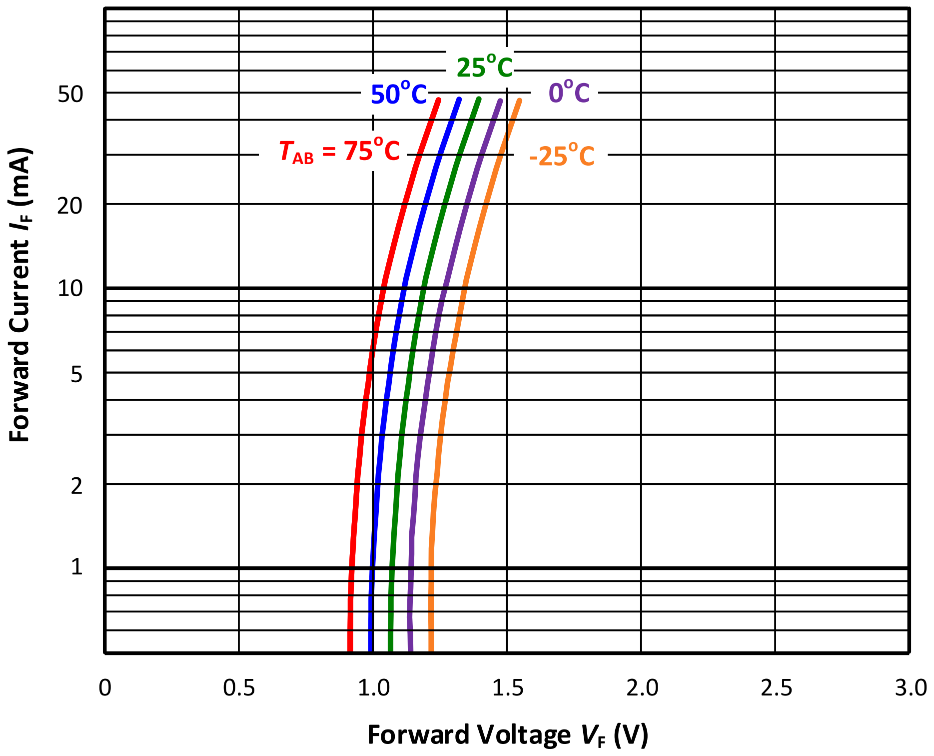




- CTR is quite nonlinear with forward current and temperature.

Opto-Coupler PC817C

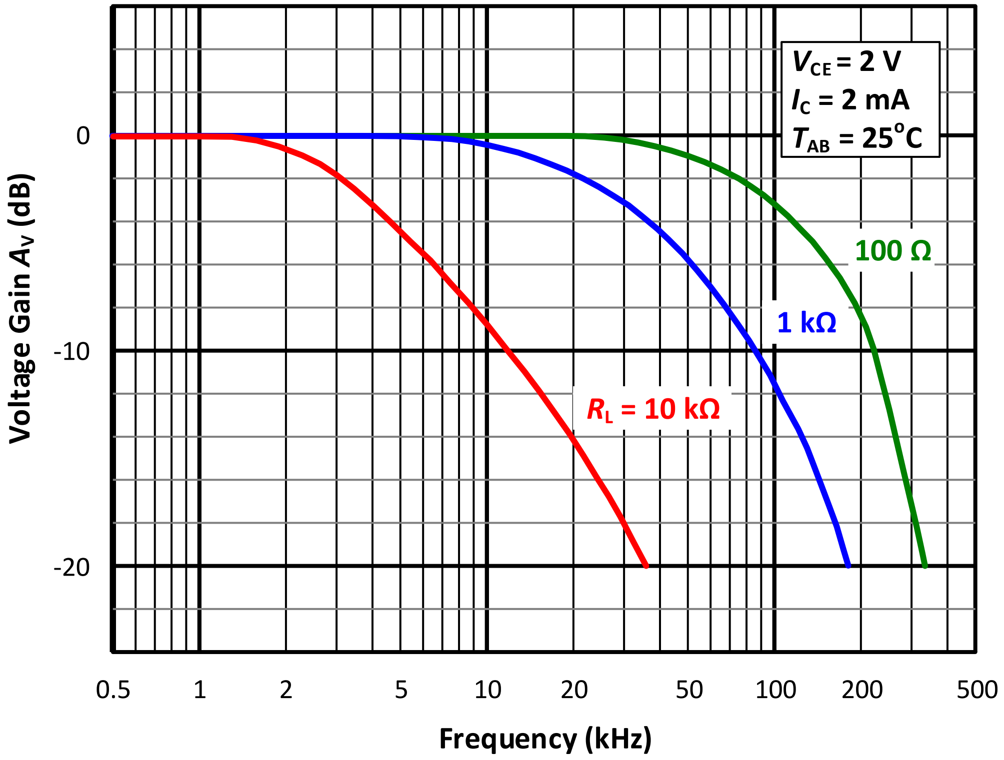
Forward Current vs. Forward Voltage

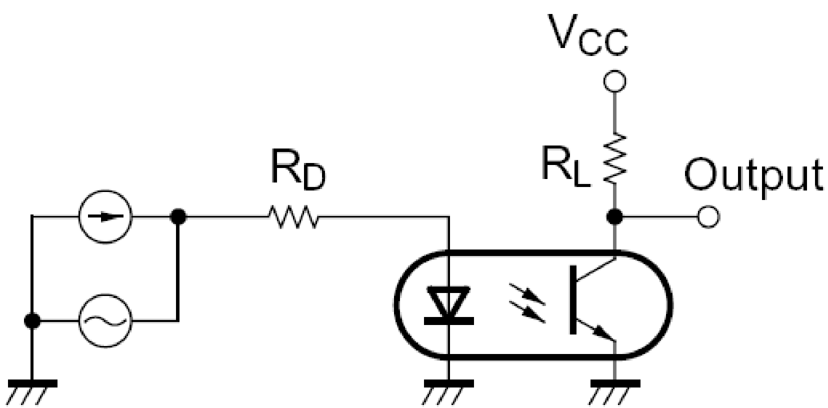


- Forward voltage on opto-diode has only small variation in low forward current range. Assumed to be constant for simplicity.
- Forward voltage is getting lower when higher ambient temperature.

Opto-Coupler PC817C

Frequency Response of PC817C

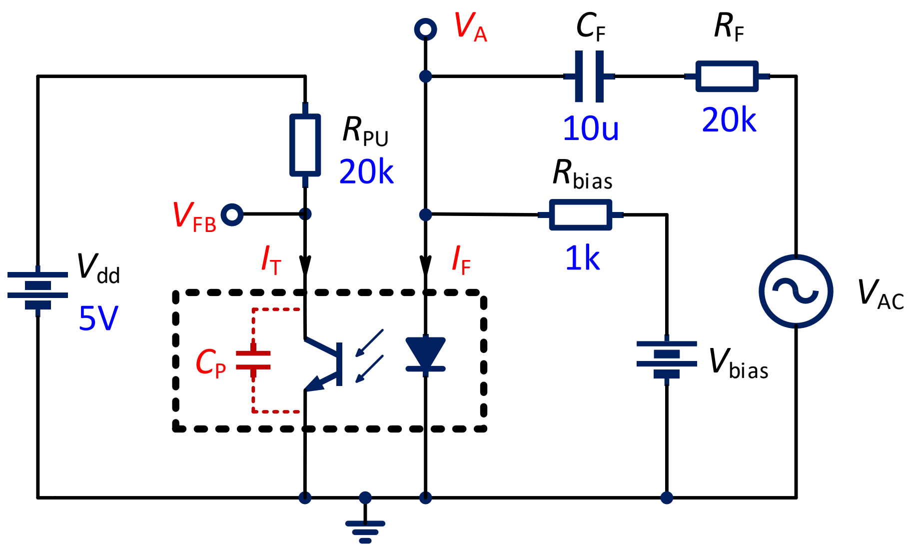


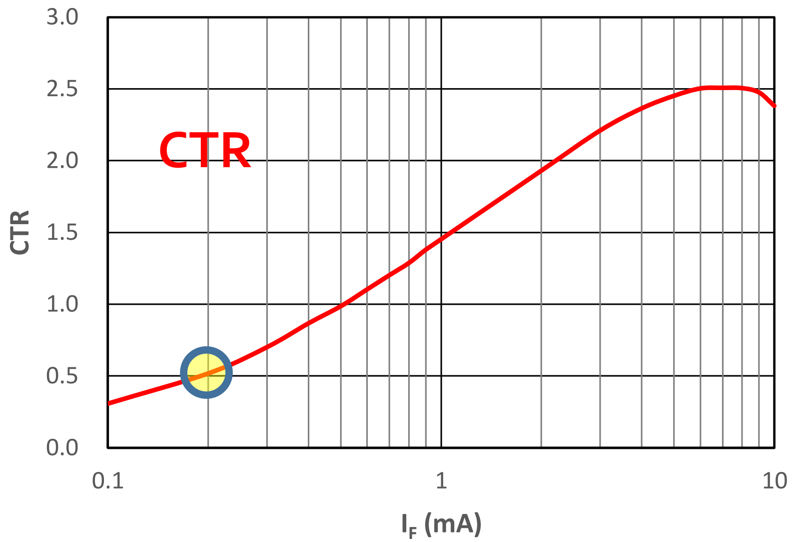


$$G_{opto}(s) = \frac{\Delta V_c(s)}{\Delta V_1(s)} = CTR \cdot \frac{R_L}{R_D \cdot \left(1 + \frac{s}{2\pi f_{po}}\right)}$$

f_{po} : pole on optocoupler 1 ~ 50 kHz

Characterization of PC817C



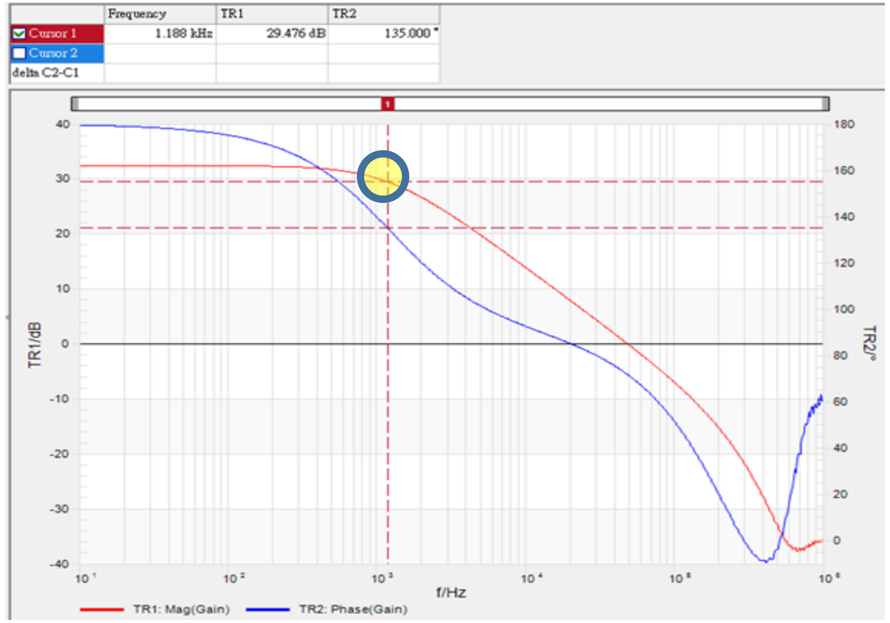


Frequency of -3dB point

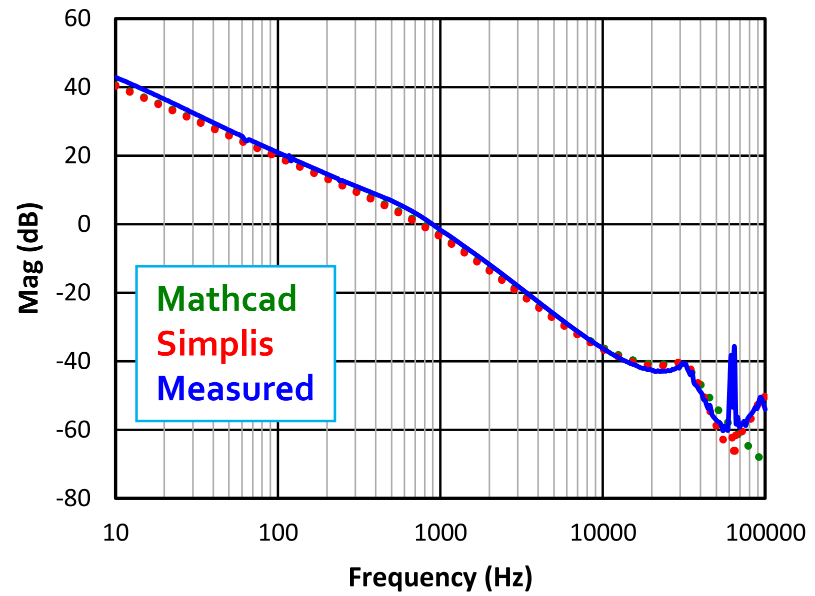
$$f_{po} \approx 1.188\,\text{kHz}$$

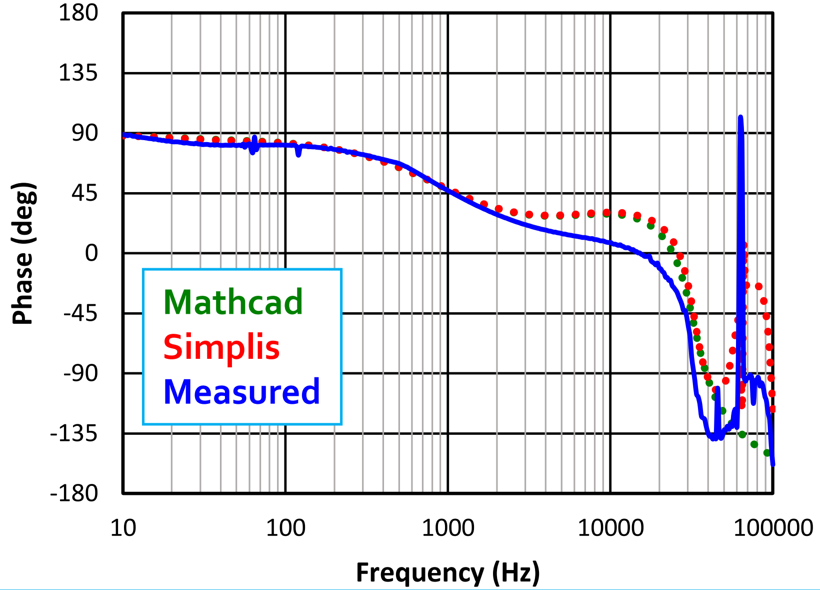
Parasitic Capacitance：

$$C_b = \frac{1}{2\pi \cdot R_{pu} \cdot f_{po}} = 6.7\,\text{nF}$$



Parasitic Cap. of Opto-Transistor

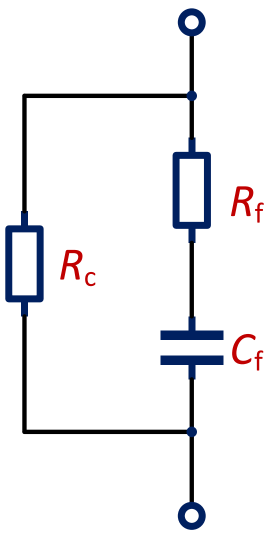




- Operating point : V_{IN} = 150V, I_O = 2A; C.C.M. operation, Duty cycle ≈ 0.335.
- Corssover frequency, f_c = 2kHz;
- Voltage divider : R_a = 38 kΩ, R_b = 10 kΩ;
- Feedback capacitance, C_a = 100 nF;
- Gain Resistance, R_c = 620 Ω;
- ESR zero of output capacitor is around 5.85 kHz;
- Pull-up resistance inside controller is 20 kΩ. Together with parasitic capacitance (8nF) of opto-transistor, the pole is located around 1 kHz. The pole is inherently much lower than ESR zero, such that lower crossover frequency and lower phase margin are expected.

Countermeasure Proposed (Phase Booster)

- **The countermeasure could be adding a "phase booster".**
- A series R_f and C_f is paralleled to cathode resistor R_c. It can equivalently form a phase booster.
- The pole (R_d, C_b) is aimed to cancel ESR zero of output capacitor. However, if the location of pole is much lower than ESR zero, the gain will be decreased before ESR zero. The crossover frequency will be lower, and the phase margin will be lower accordingly.



$$Z(s) = R_c \parallel \left(R_f + \frac{1}{sC_f} \right) = R_c \parallel \left(\frac{1 + sR_fC_f}{sC_f} \right)$$

$$= \frac{R_c\left(1 + sR_fC_f\right)}{1 + s\left(R_c + R_f\right)C_f} \cong \frac{R_c\left(1 + \dfrac{s}{\omega_z}\right)}{\left(1 + \dfrac{s}{\omega_p}\right)}$$

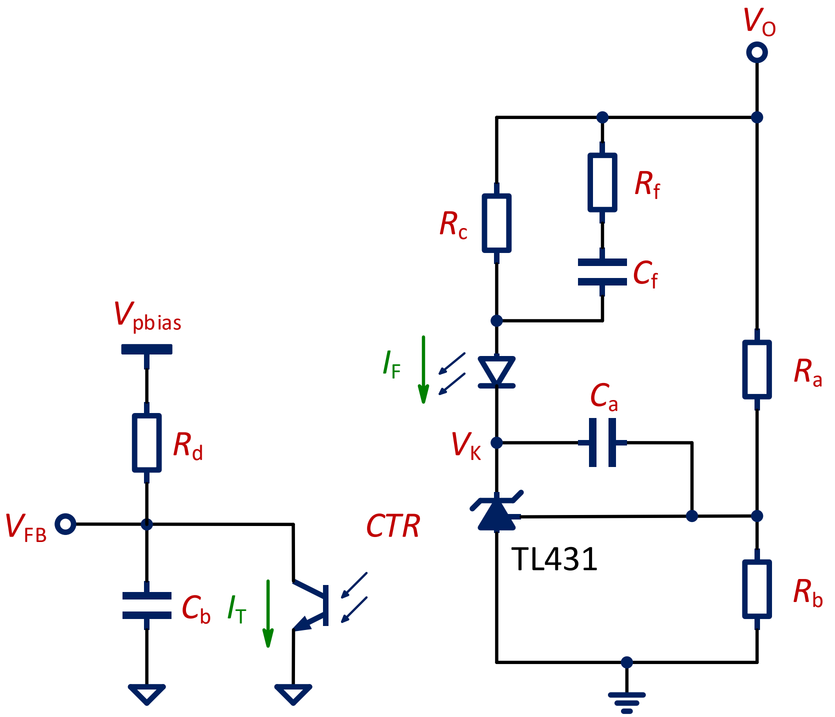
$$\omega_p = \frac{1}{R_fC_f} \quad , \quad \omega_z = \frac{1}{\left(R_c + R_f\right)C_f}$$

$$\begin{cases} R_fC_f = r_CC_O \\ (R_c + R_f)C_f = R_dC_b \end{cases}$$

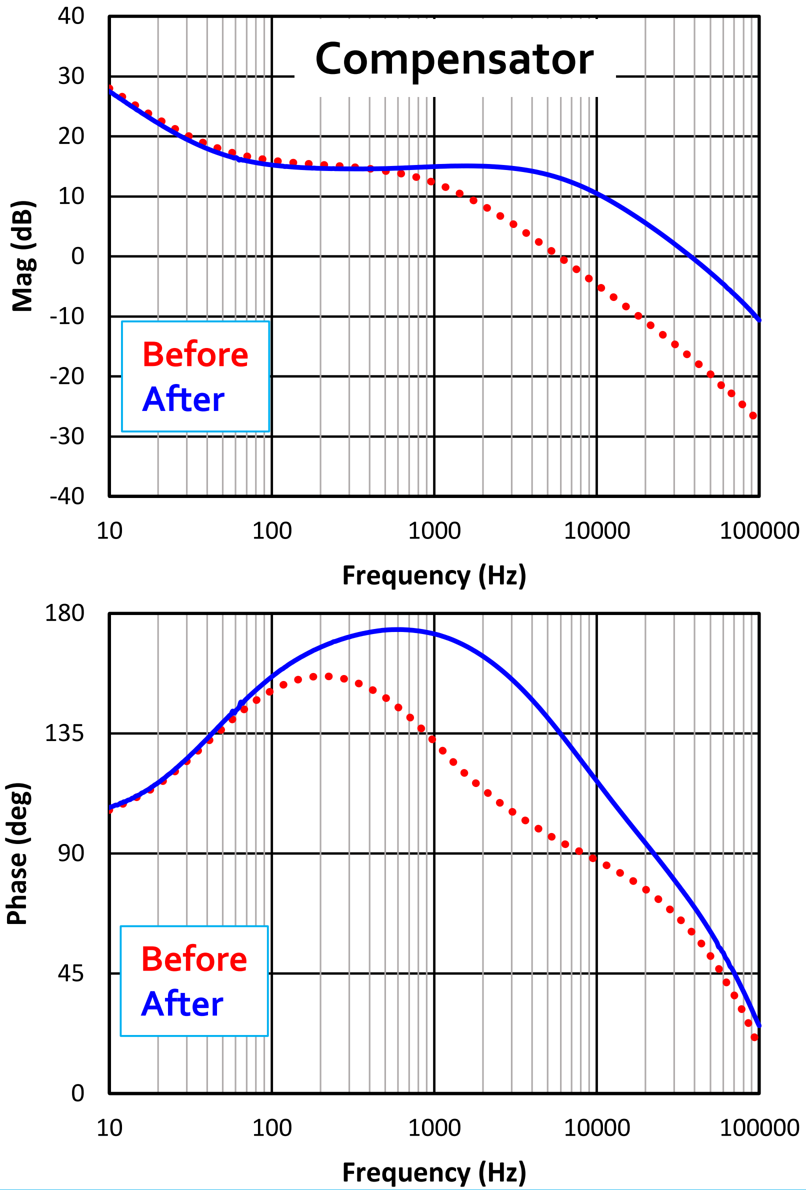
$$R_f = \frac{R_c}{\dfrac{R_dC_b}{r_CC_O} - 1} \quad , \quad C_f = \frac{r_CC_O}{R_f}$$

- ESR Zero is getting higher for new output capacitors.

Phase Booster of Compensator



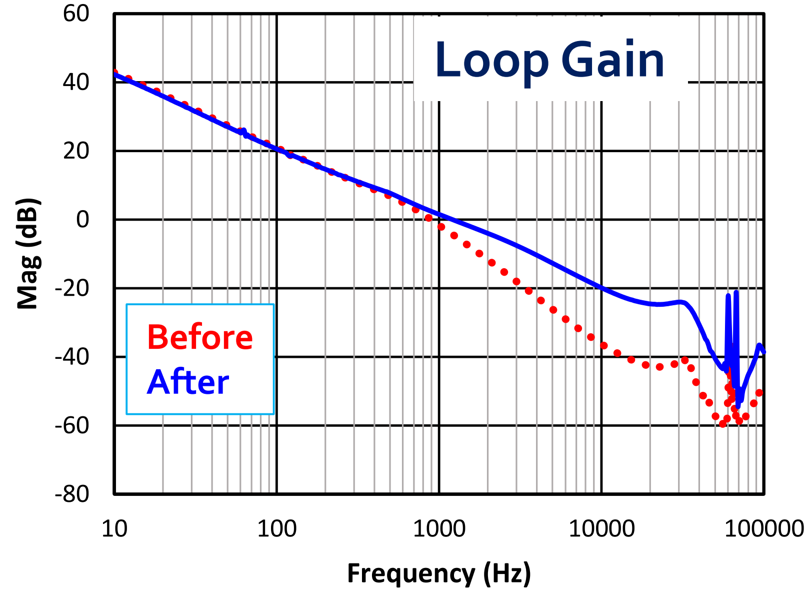
$R_C = 620\Omega$
$R_f = 120\Omega$
$C_f = 0.22\mu F$

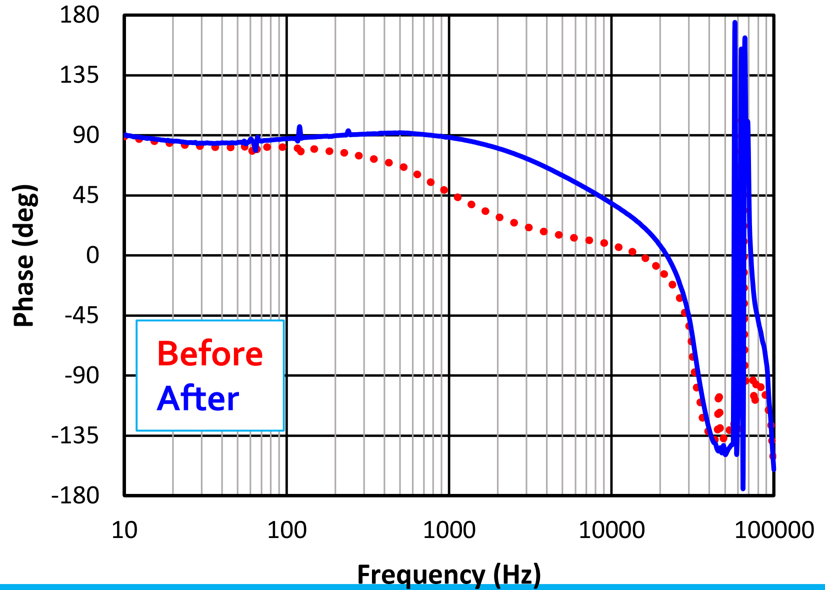


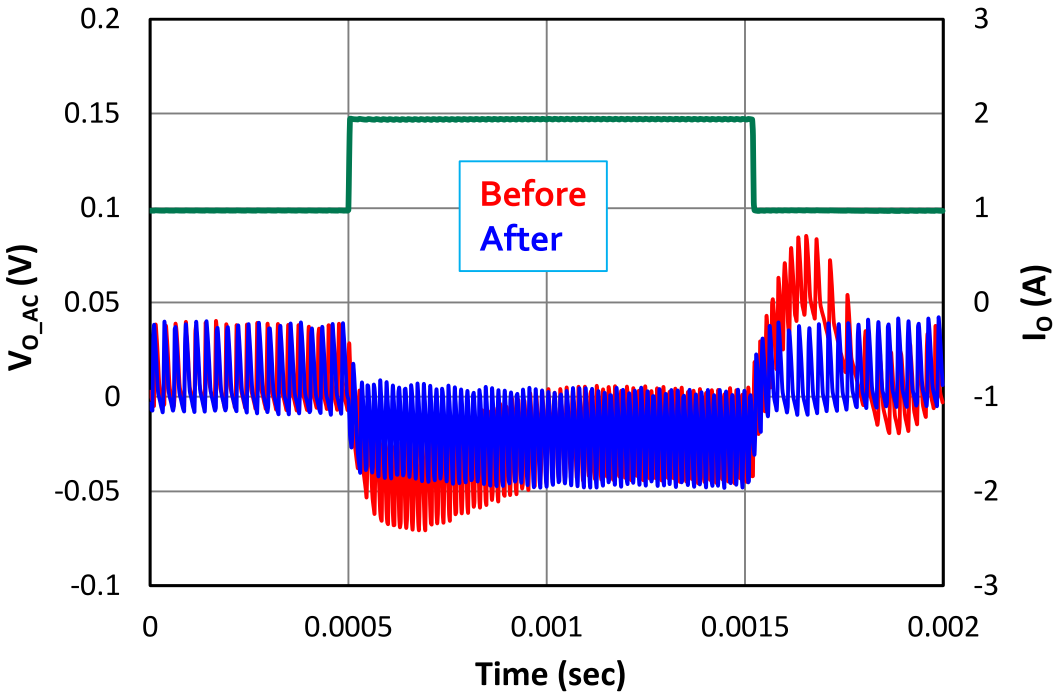
$$G_{COMP}(s) = CTR \cdot \frac{R_d}{R_c} \cdot \frac{(1 + s \cdot R_a C_a) \cdot [1 + s(R_c + R_f) C_f]}{sR_a C_a \cdot (1 + sR_d C_b) \cdot (1 + sR_f C_f)}$$

- Additional R_f/C_f acts as phase booster. One lower zero compensates R_d/C_b pole. Another new high-frequency pole to cancel the ESR zero.

Loop Gain and Dynamic Load Measurement





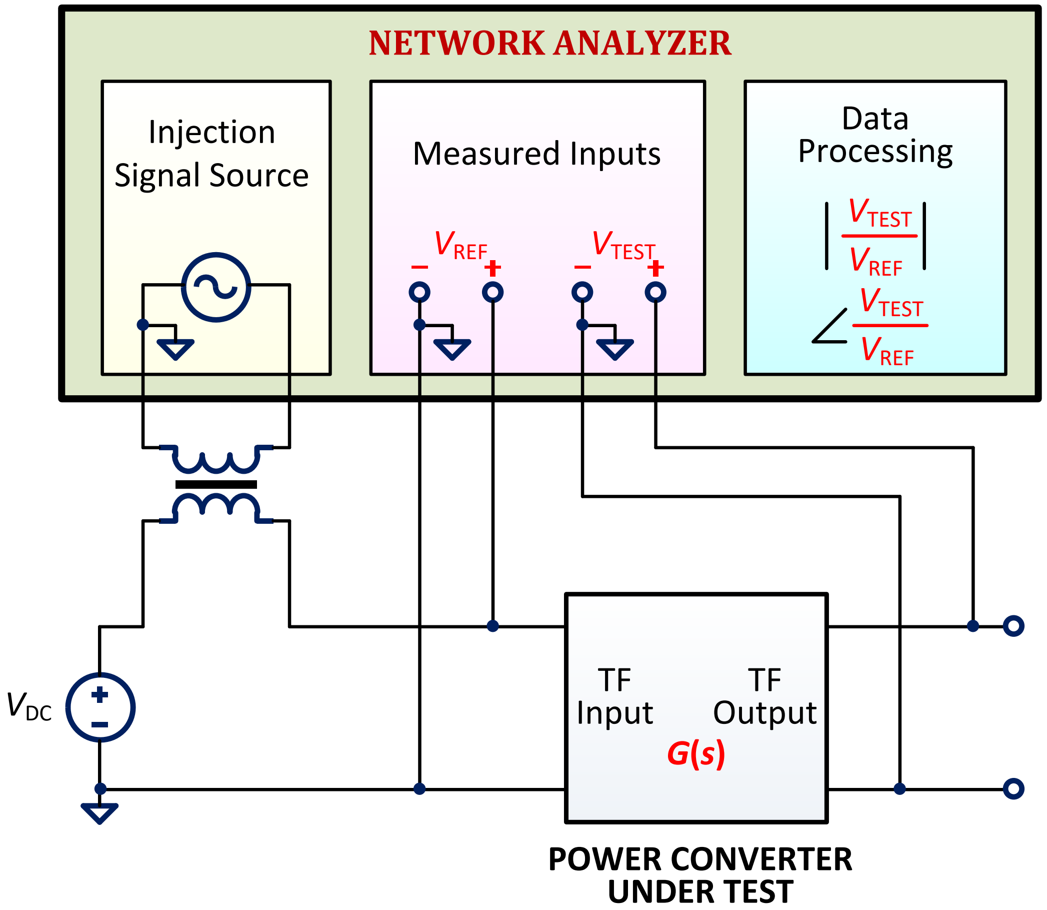


- Loop gain as well as phase margin is improved significantly.
- Dynamic load change response is improved. (Steady-state error results from output terminal measured)

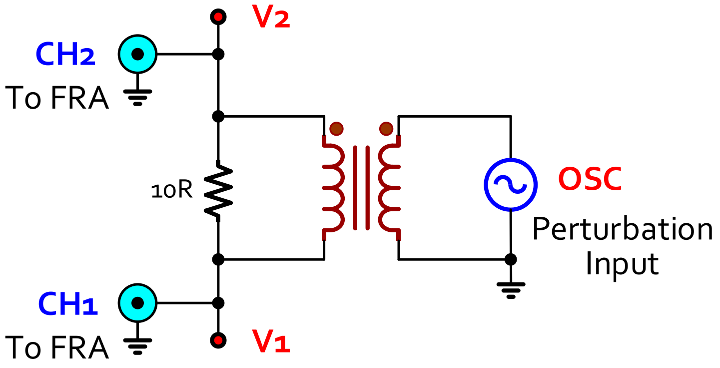
Conclusions

1. 1P1Z plant for both C.C.M. and D.C.M. PCMC Flyback.
2. A Type II (2P1Z) compensator is the most adequate for PCMC Flyback.
3. Opto-coupler + Shunt regulator is the most cost effective way to implement Type II compensator for isolated power converters.
4. Parasitic capacitance of Opto-coupler could degrade the loop performance (bandwidth , phase margin) and dynamic load change response, especially for higher ESR zero capacitors.
5. A simple phase booster is proposed to eliminate the effect from opto-coupler's parasitic capacitance.

Transfer Function Measurement

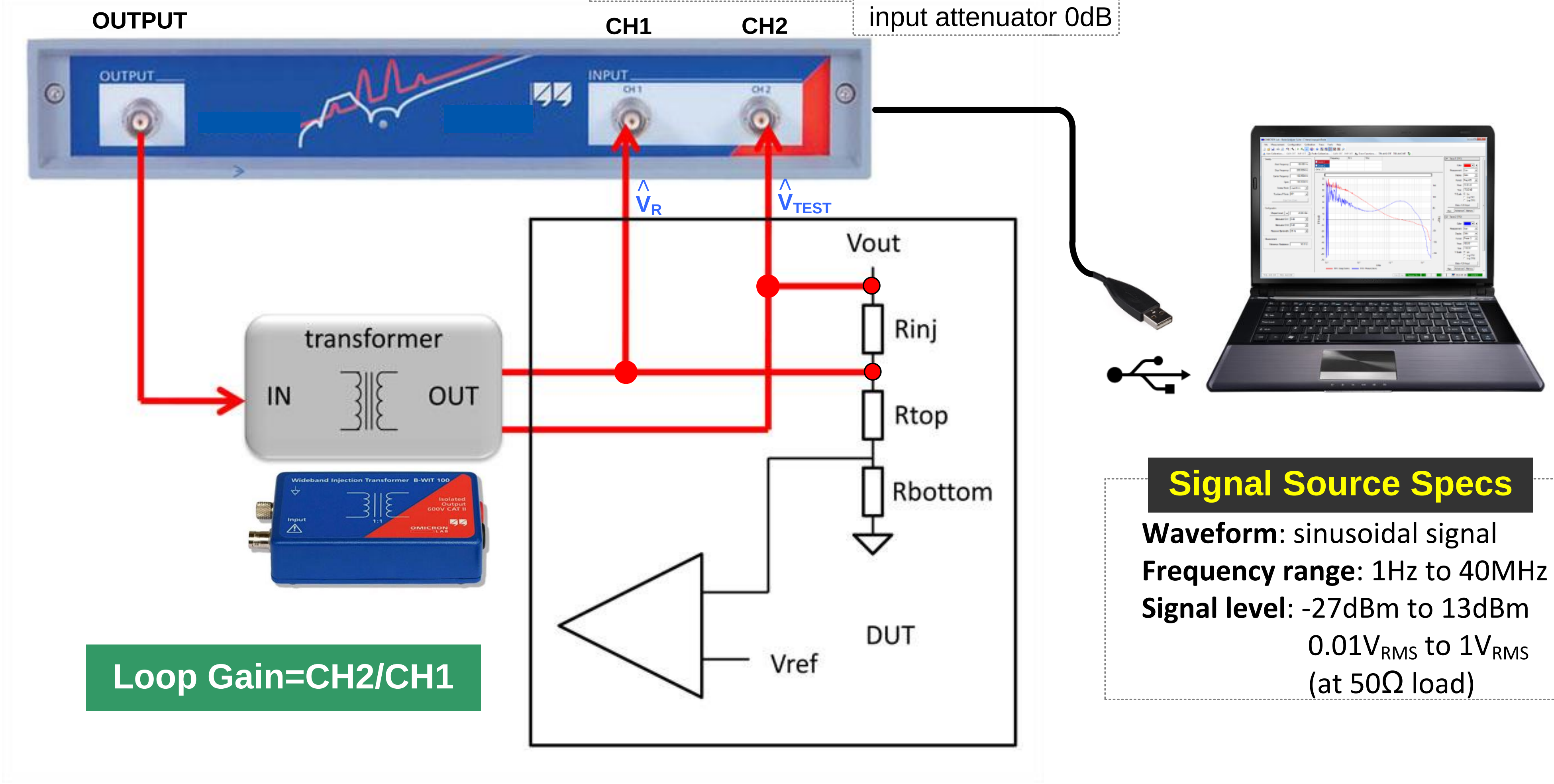


- Impedance of Passive Components
- Gain-Phase of a Transformer
- Loop Gain / Compensator / Power Stage Transfer Functions / Output Impedance of Switching Converters



- Network Analyzer automatically generates Bode Plots of V_{TEST}/V_{REF} , including magnitude and phase.

Loop Gain Measurement with OSC Options



CH1/CH2 sensitivity: 100mV full scale for input attenuator 0dB

Signal Source Specs

Waveform: sinusoidal signal
Frequency range: 1Hz to 40MHz
Signal level: -27dBm to 13dBm
$0.01V_{RMS}$ to $1V_{RMS}$
(at 50Ω load)

Demo : Loop Gain Measurement (RTA4004-K36, R&S)

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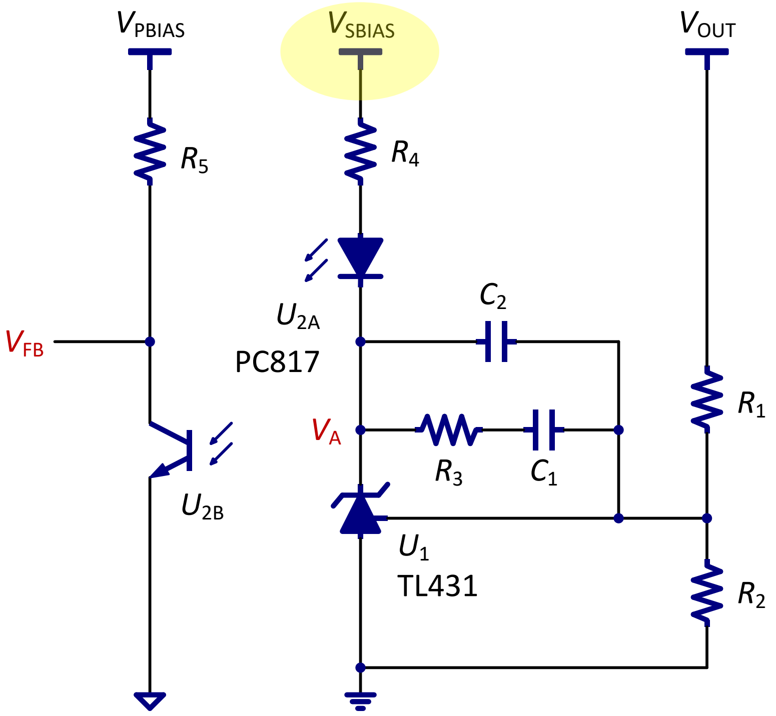
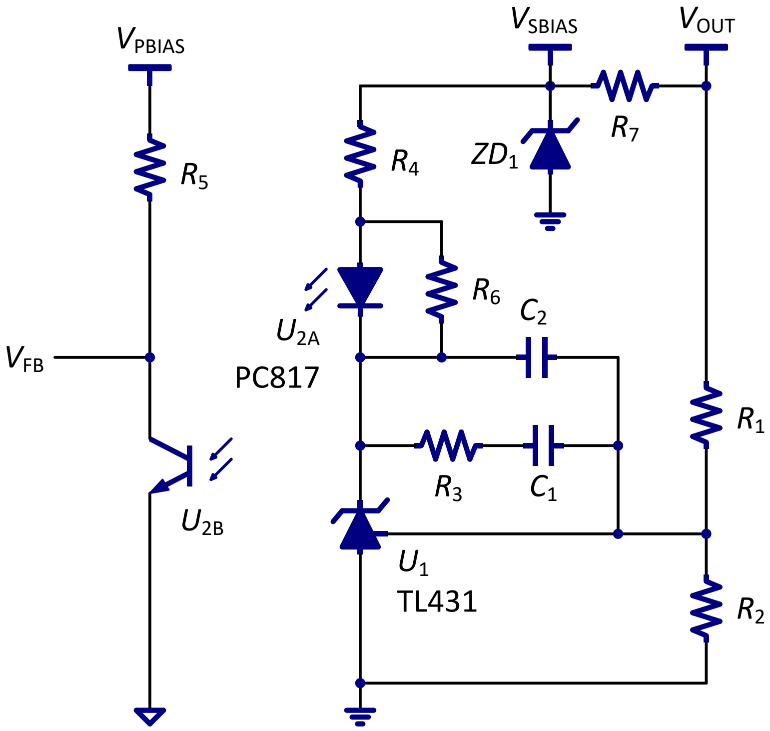
Thanks

Transfer Functions Derivation for Various Type II Compensator Based on Opto-Coupler and Shunt Regulator

Configuration I





Assumptions

1. Open-Loop Gain of TL431 is *K*.
2. Only constant gain (CTR) is in Opto-coupler.
3. V_{LED} is constant.
4. Loading of V_{FB} is zero.

Implementation of V_{SBIAS}

DC Analysis

$$V_A = K \cdot \left[\left(V_{OUT} \times \frac{R_2}{R_1 + R_2} \right) - V_{REF} \right] \quad (1)$$

$$V_A = V_{SBIAS} - I_{LED} \times R_4 - V_{LED} \quad (2)$$

$$I_{TR} = CTR \times I_{LED} \quad (3)$$

$$V_{PBIAS} = I_{R5} \times R_5 + V_{FB} = I_{TR} \times R_5 + V_{FB} \quad (4)$$

$$\begin{aligned} V_{FB} &= V_{PBIAS} - I_{TR} \times R_5 \\ &= V_{PBIAS} - CTR \times I_{LED} \times R_5 \\ &= V_{PBIAS} - CTR \times \frac{(V_{SBIAS} - V_A - V_{LED})}{R_4} \times R_5 \\ &= V_{PBIAS} - CTR \times \frac{R_5}{R_4} \times \left\{ K \cdot \left[V_{REF} - \left(V_{OUT} \times \frac{R_2}{R_1 + R_2} \right) \right] + V_{SBIAS} - V_{LED} \right\} \quad (5) \end{aligned}$$

AC Analysis

The feedback network, including C_1, C_2 and R_3 is represented as Z_{FB}.

$$Z_{FB}(s) = \frac{1 + sC_1R_3}{s(C_1 + C_2)(1 + s\frac{C_1C_2}{C_1 + C_2}R_3)} \quad (6)$$

$$\frac{\hat{v}_A(s)}{\hat{v}_{OUT}(s)} = \frac{Z_{FB}(s)}{R_1} \quad (7)$$

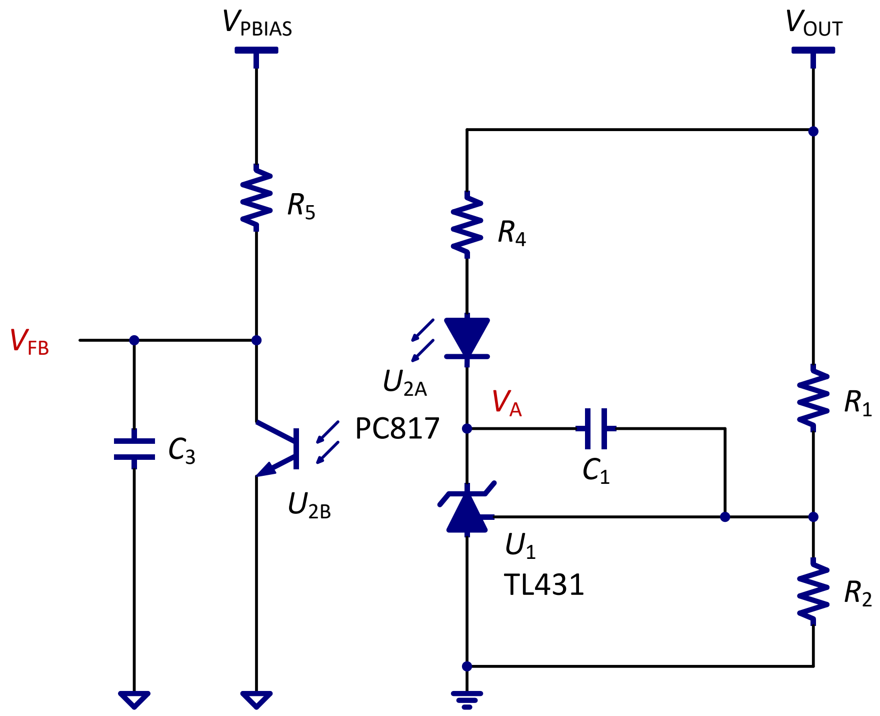
$$\hat{v}_A(s) = -\hat{i}_{LED}(s) \times R_4 \quad (8)$$

$$\hat{v}_{FB}(s) = -CTR \times R_5 \times \hat{i}_{LED}(s) \quad (9)$$

$$\frac{\hat{v}_{FB}(s)}{\hat{v}_{OUT}(s)} = CTR \times \frac{R_5}{R_4} \times \frac{Z_{FB}(s)}{R_1} = CTR \times \frac{R_5}{R_4} \times \frac{1 + sC_1R_3}{sR_1(C_1 + C_2)(1 + s\frac{C_1C_2}{C_1 + C_2}R_3)} \quad (10)$$

$\boxed{\text{2-pole 1-zero (Type II)}}$

Configuration II (the most commonly adopted)



- TL431 is powered by output voltage.
- Perturbation on V_{OUT} can go through both voltage divider (error amplifier) and opto-diode directly.

DC Analysis

$$V_A = K \cdot \left[\left(V_{OUT} \times \frac{R_1}{R_1 + R_2} \right) - V_{REF} \right] \quad (11)$$

$$V_A = V_{OUT} - I_{LED} \times R_4 - V_{LED} \quad (12)$$

$$I_{TR} = CTR \times I_{LED} \quad (13)$$

$$V_{PBIAS} = I_{R5} \times R_5 + V_{FB} = I_{TR} \times R_5 + V_{FB} \quad (14)$$

Similar with (1) ~ (4), except V_{SBIAS} in (2) is changed to V_{OUT}.

AC Analysis

$$\frac{\hat{v}_A(s)}{\hat{v}_{OUT}(s)} = \frac{Z_{FB}(s)}{R_1} \quad (15)$$

$$\hat{v}_A(s) = \hat{v}_{OUT}(s) - \hat{i}_{LED}(s) \times R_4 \quad (16)$$

$$\hat{v}_{FB}(s) = -CTR \times \frac{R_5}{1 + sR_5C_3} \times \hat{i}_{LED}(s) \quad (17)$$

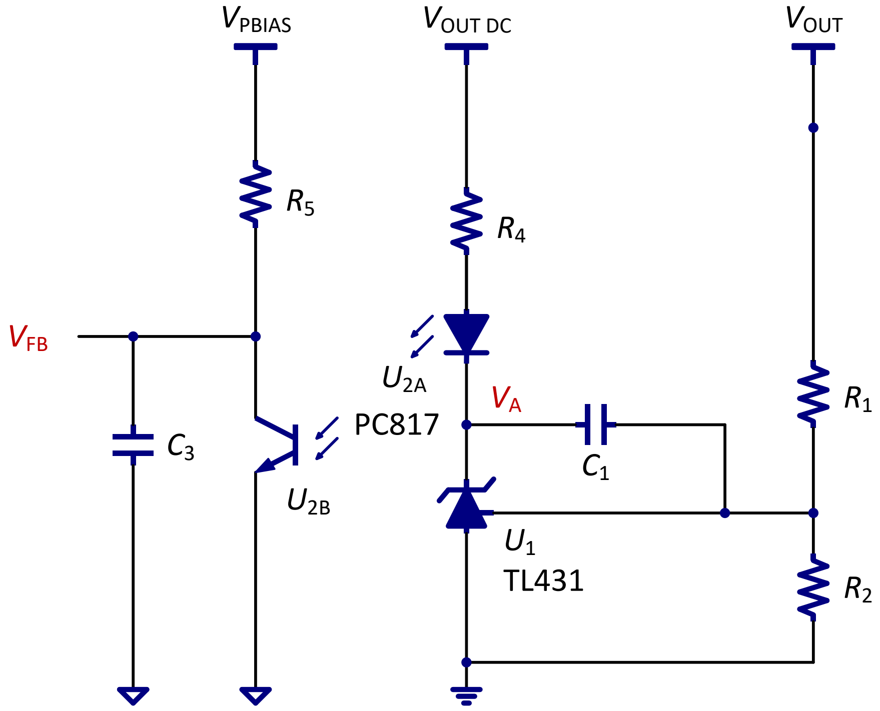
$$\frac{\hat{v}_{FB}(s)}{\hat{v}_{OUT}(s)} = CTR \times \frac{R_5}{R_4} \times \frac{1 + \frac{Z_{FB}(s)}{R_1}}{1 + sR_5C_3} \quad (18)$$

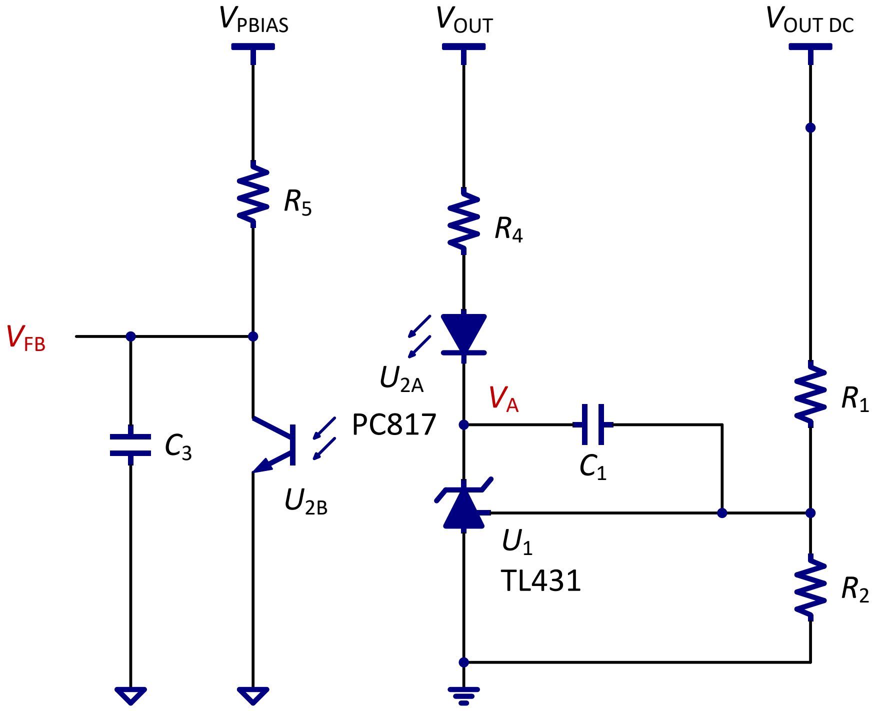
$$Z_{FB}(s) = \frac{1}{sC_1} \quad (19)$$

2-pole 1-zero (Type II)

$$\frac{\hat{v}_{FB}(s)}{\hat{v}_{OUT}(s)} = CTR \times \frac{R_5}{R_4} \times \frac{1 + sR_1C_1}{sR_1C_1(1 + sR_5C_3)} \quad (20)$$

Superposition





$$\frac{\hat{v}_{FB}(s)}{\hat{v}_{OUT}(s)} = CTR \times \frac{R_5}{R_4} \times \frac{1}{sR_1C_1(1+sR_5C_3)}$$

(Slow Lane)

$$+$$

$$\frac{\hat{v}_{FB}(s)}{\hat{v}_{OUT}(s)} = CTR \times \frac{R_5}{R_4} \times \frac{1}{1+sR_5C_3}$$

(Fast Lane)

- Superposition can be applied to get slow-lane and fast-lane transfer function with respectively.

Bode plot of a Type II (2P1Z) Compensator