Signal Integrity of Samtec highspeed connector with flyover cables for PCIe5 signaling

INNOVATIVE TECHNOLOGIES • SUDDEN SERVICE • GLOBAL REACH

Outlines

Samtec -HIGH-SPEED connector - PCIe5 / Gen Z / HIGH-DENSITY 56Gb/112Gb/s series

Samtec -TWINAX cable - PCIe5 / Gen Z extend cable / 56Gb/112Gb Filyover series

- **Correlations on PCIe 5 connector**
  - Fixture designs and boards
  - Examples of SPEC from simulated and measured S para.
- **ARC6 Channel Simulation for PCIe5 signaling**
  - Parts/ configs.
  - Channel response.
  - Results.
- **EBTX**
  - EBTX for backplane
  - EBTX + Si-fly internal
  - EBTX + ARC6 internal

- **Samtec Test Fixture & RF solution**

HIGH-SPEED/HIGH-DENSITY | Board to Board connector

BOARD-TO-BOARD & BACKPLANES

SEARAY™

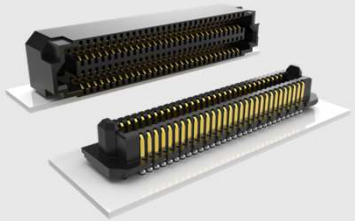
PAM4 56 Gbps

High-Speed Open-Pin-Field Arrays
1.27mm/0.85mm / Up to 500 pin

ACCELERATE® HD

PAM4 56 Gbps

Ultra Dense, 4 Row Strips /0.635mm
up to 400 pin



ACCELERATE® HP

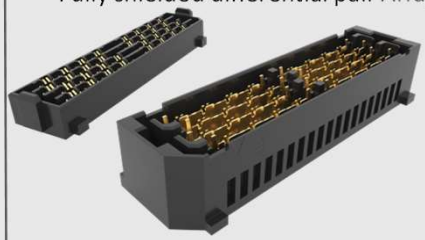
PAM4 112 Gbps

High-Performance Multi-Row Strips
0.635mm / up to 800 pin

NOVARAY®

PAM4 112 Gbps

Extreme Performance/ 0.8mm / 32 pair
Fully shielded differential pair Arrays



ExaMAX®

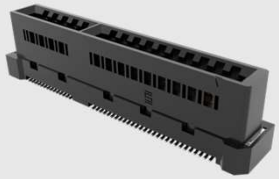
PAM4 56 Gbps

BACKPLANE - 2.0mm
Up to 24 - 72 pair

GEN Z

PAM4 56 Gbps

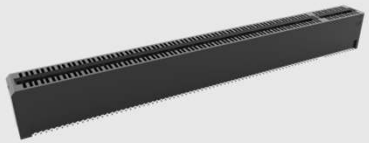
Compliant to SFF-TA-1002 Edge Card
x4 (IC), x8 (2C), x16 (4C and 4C+)



PCI EXPRESS®

PAM4 56 Gbps

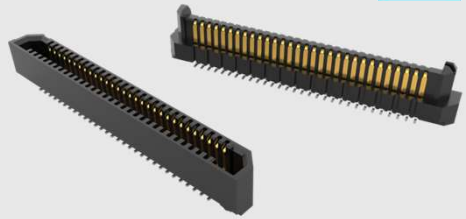
PCIe-Gen 5/ Gen4 x4/x8/x16
Edge Card Technology



EDGE RATE® CONTACT

PAM4 56 Gbps

Rugged latching,
0.50 /0.635 / 0.80 mm
10 !200 pin



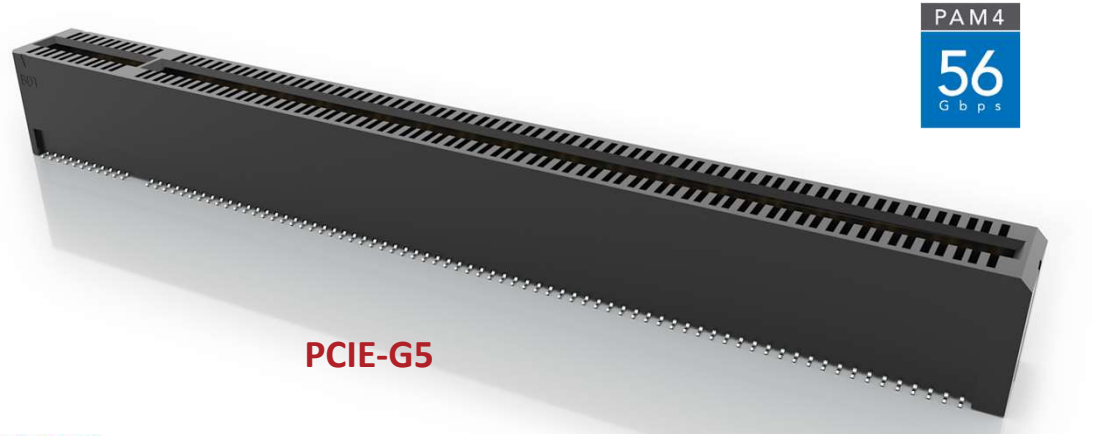
PCI EXPRESS® G5/ G4 SOCKETS

Differential pair system

1.00 mm pitch

Mates with standard PCIe® expansion cards

1, 4, 8 and 16 PCI Express® 5.0 link options



PCIE-G5

PCIe® 4.0/5.0 mating cable assembly in development

KEY SPECIFICATIONS

SERIES	TOTAL PINS (LANES)	INSULATOR MATERIAL	CONTACT MATERIAL	OPERATING TEMP RANGE	CURRENT RATING	VOLTAGE RATING	PCIE® COMPATIBILITY
PCIE	36 (x1), 64 (x4), 98 (x8), 164 (x16)	-TH = Black Nylon -EMS2 & -TH = LCP	Phosphor Bronze	-55 °C to +125 °C	2.4 A (2 pins)	215 VAC	3.0
PCIE-LP	36 (x1), 64 (x4), 98 (x8), 164 (x16)	LCP	Phosphor Bronze	-55 °C to +125 °C	2.1 A (2 pins)	215 VAC	4.0
PCIE-G4	36 (x1), 64 (x4), 98 (x8), 164 (x16)	LCP	Copper Alloy	-55 °C to +125 °C	2.2 A (2 pins)	300 VAC	4.0
PCIE-G5	36 (x1), 64 (x4), 98 (x8), 164 (x16)	LCP	Copper Alloy	-55 °C to +125 °C	3.2 A (2 pins)	235 VAC	5.0

Gen Z – SOCKETS

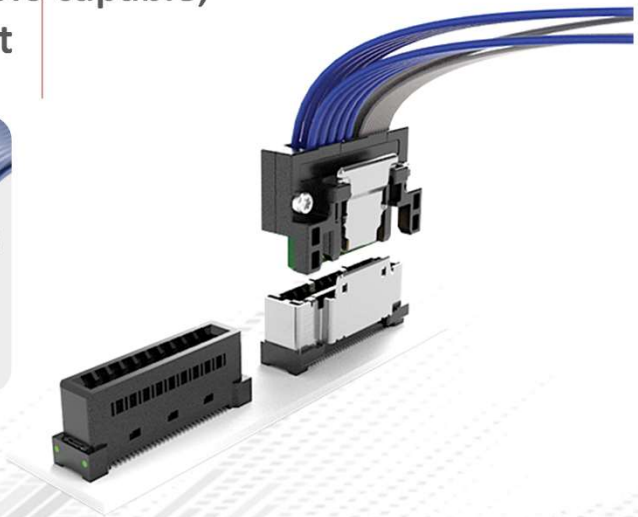
Differential pair Edge Rate® contacts

Compliant to SFF-TA-1002:

x4 (IC), x8 (2C), x16 (4C and 4C+)

Mates with .062" (1.60 mm) thick cards

PCI Express® 4.0 and 5.0 capable;
and Gen-Z™ compliant



GENERATE

PAM4 56 Gbps

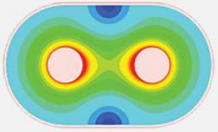
HSEC6-DV

ULTRA LOW SKEW TWINAX cable

MICRO CELLULAR DIELECTRIC EXTRUSION

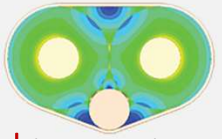
- Critical dimensions measured at every dielectric spool
- Inline laser and CAPAC devices for capacitance monitoring and diameter control
- In-process stats summary sheet for Cpk acceptance

SAMTEC CABLE



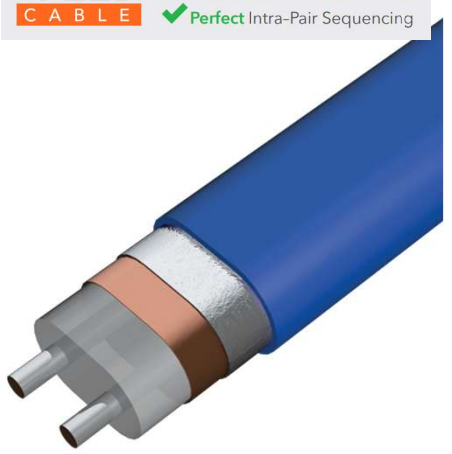
✔ Good design coupling with Samtec's co-extruded ultra low skew twinax

INDUSTRY CABLE

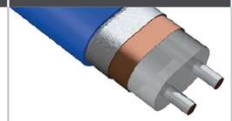
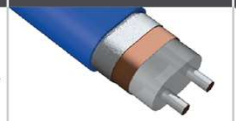
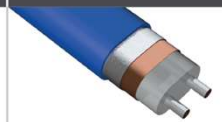
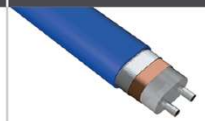
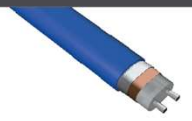


✘ Bad design coupling with individually extruded conductors & drain wire

EYE SPEED CABLE



NOMINAL PERFORMANCE

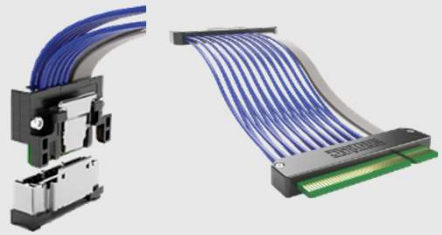
			28 AWG	30 AWG	32 AWG	34 AWG	36 AWG
Eye Speed® Ultra Low Skew Twinax Cable							
14 GHz (28G NRZ/ 56G PAM4)	0.25 m	IL (dB)	-1.0	-1.2	-1.5	-1.8	-2.2
	1.00 m		-4.1	-4.7	-5.9	-7.5	-8.9
28 GHz (56G NRZ/ 112G PAM4)	0.25 m		-1.5	-1.8	-2.2	-2.7	-3.2
	1.00 m		-6.1	-7.1	-8.7	-10.9	-12.7
Density/Flexibility			Good	Good	Better	Best	Best

HIGH-SPEED CABLE

Board-TO-Cable Solutions

GEN Z PCI EXPRESS 5.0 SOLUTION

PAM4 56 Gbps

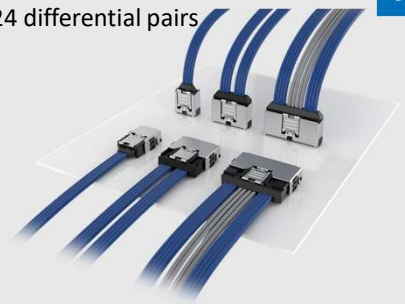


ACCELERATE®

Slim Body Direct Attach Cables

8~24 differential pairs

PAM4 56 Gbps



ACCELERATE®HP

32 to 72 differential pairs

92 Ω differential

PAM4 112 Gbps

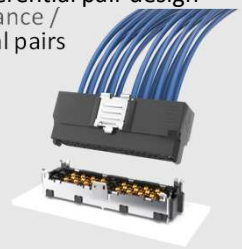
NOVARAY®

fully shielded differential pair design

Extreme Performance /

8 to 32 differential pairs

PAM4 224 Gbps



SI-FLY™

extremely low 3.8 mm low profile

8-16 differential pairs, 92 Ω / 100 Ω

PAM4 112 Gbps

FLYOVER®

8 Channels (16 pairs) , 92 Ω

Up to 800 Gbps aggregate (

QSFP-DD800

MSA Compliant

PAM4 112 Gbps

ExaMAX®

Backplane Cable System

24 - 72 pair designs

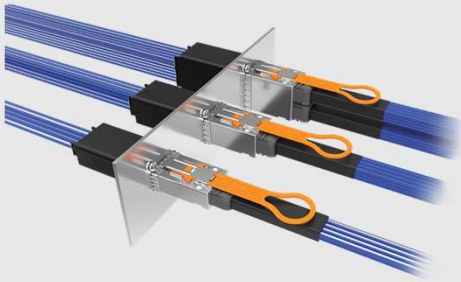
PAM4 112 Gbps

NOVARAY® I/O

Extreme Density Bulkhead

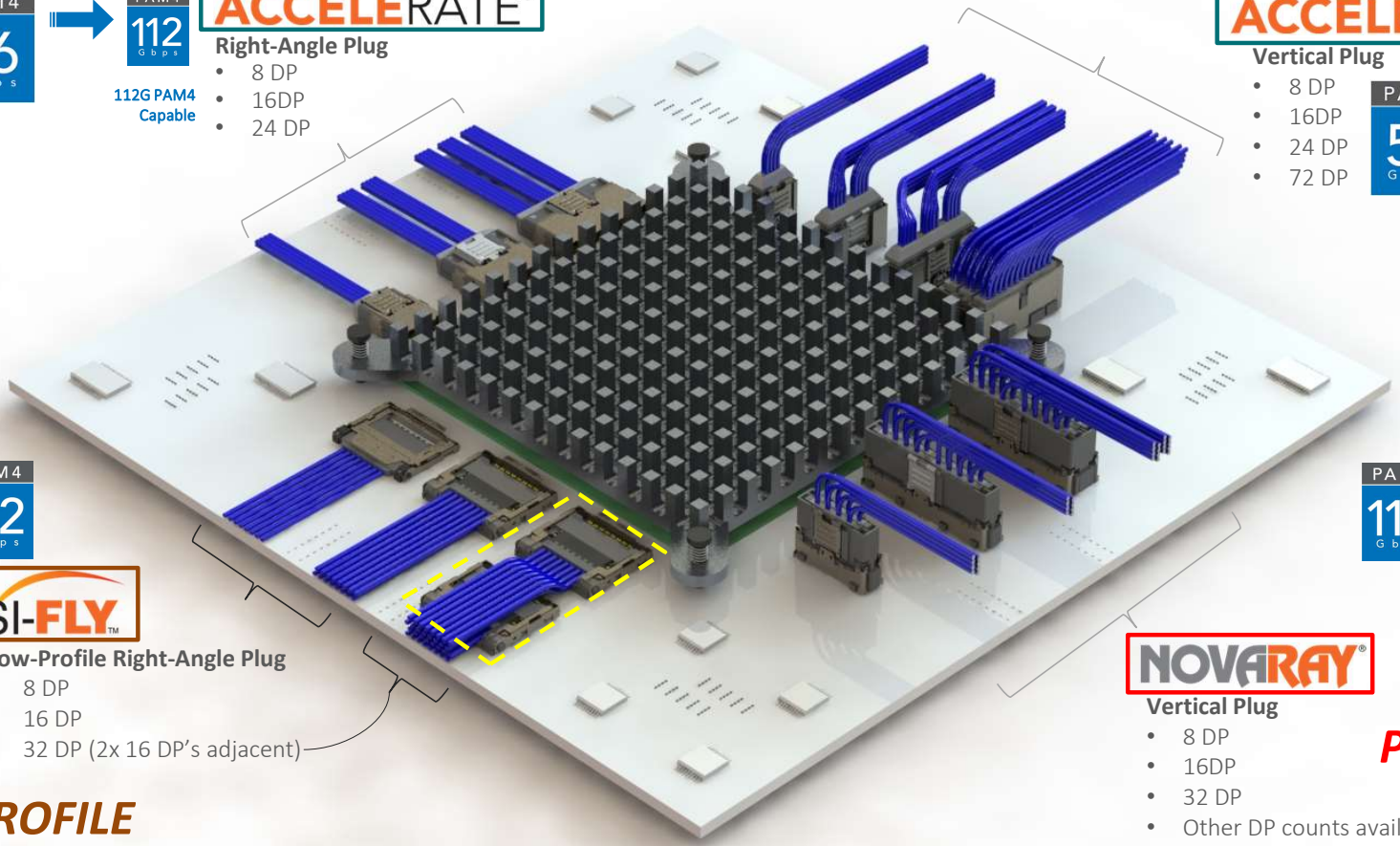
Cable System

PAM4 112 Gbps



FLYOVER OPTIMAL END 2 "ADJACENT-TO-CHIP PACKAGE" OPTIONS

HIGHEST DENSITY



PAM4 56 Gbps → PAM4 112 Gbps

112G PAM4 Capable

ACCELERATE®

Right-Angle Plug

- 8 DP
- 16DP
- 24 DP

ACCELERATE®

Vertical Plug

- 8 DP
- 16DP
- 24 DP
- 72 DP

PAM4 56 Gbps → PAM4 112 Gbps

112G PAM4 Capable

PAM4 112 Gbps

SI-FLY™

Low-Profile Right-Angle Plug

- 8 DP
- 16 DP
- 32 DP (2x 16 DP's adjacent)

PAM4 112 Gbps → PAMX 224 Gbps

NOVARAY®

Vertical Plug

- 8 DP
- 16DP
- 32 DP
- Other DP counts available

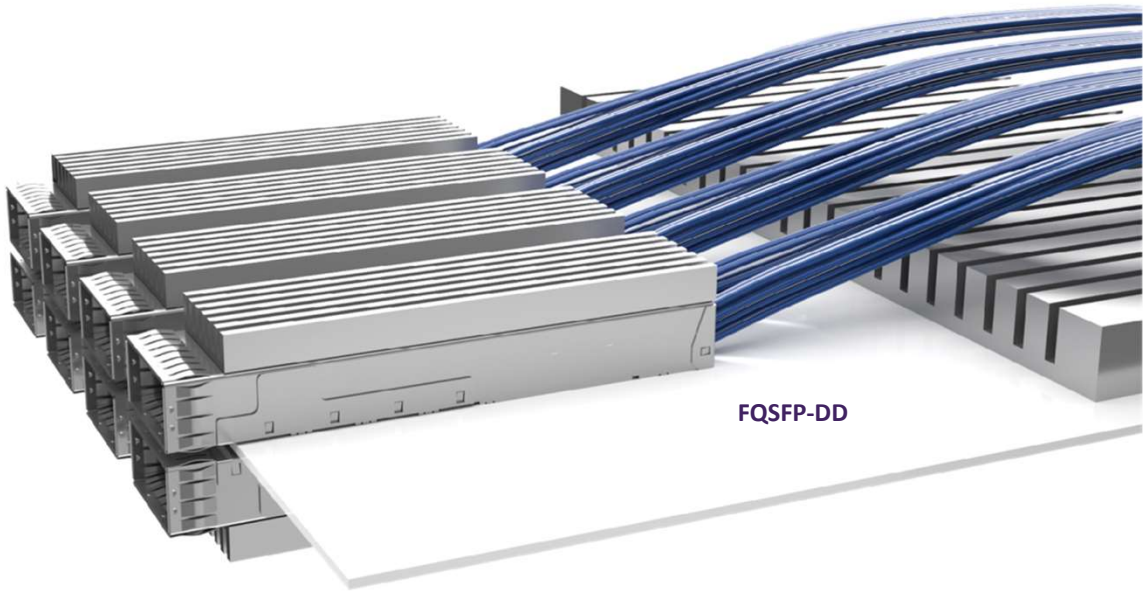
HIGHEST PERFORMANCE

LOWEST PROFILE

FLYOVER® QSFP DOUBLE DENSITY SYSTEM

FLYOVER® | NRZ 56 Gbps | PAM4 112 Gbps

Simplifies Board Layout and Reduces Thermal Challenges



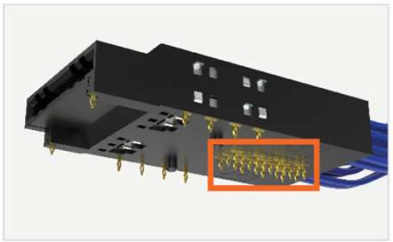
FQSFP-DD

FLYOVER® QSFP DOUBLE DENSITY

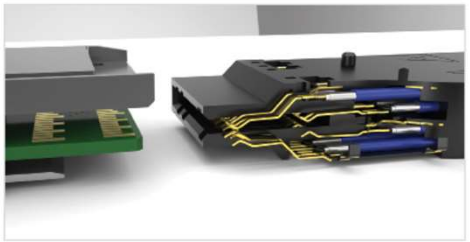
- 8 Channels (x8 bidirectional, 16 differential pairs)
- Up to 400 Gbps aggregate (56 Gbps PAM4)
- Belly–to–belly mating for maximum density
- Backward compatible with QSFP modules
- Multiple heat sink options available for optimal dissipation
- Variety of end 2 options
- Evaluation Kits available (REF-205605-X.XX-XX and REF-203423-X.XX-XX), visit samtec.com/kits

800G FLYOVER® DOUBLE DENSITY

- 8 Channels (x8 bidirectional, 16 differential pairs)
- Up to 800 Gbps aggregate (112 Gbps PAM4)
- Belly-to-belly mating for maximum density
- Backward compatible with QSFP & QSFP-DD modules
- Multiple heat sink options available for optimal dissipation
- Variety of end 2 options

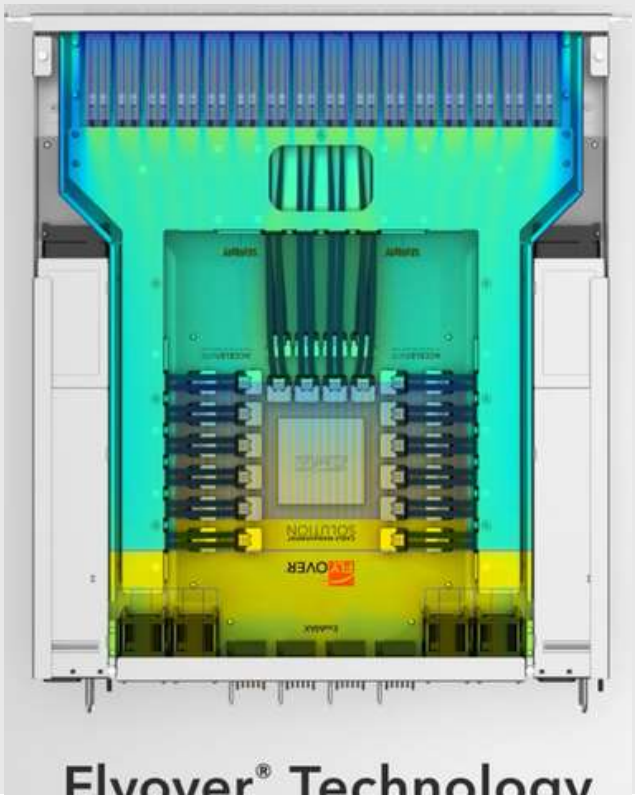


Sideband signals are routed through press–fit contacts for increased airflow

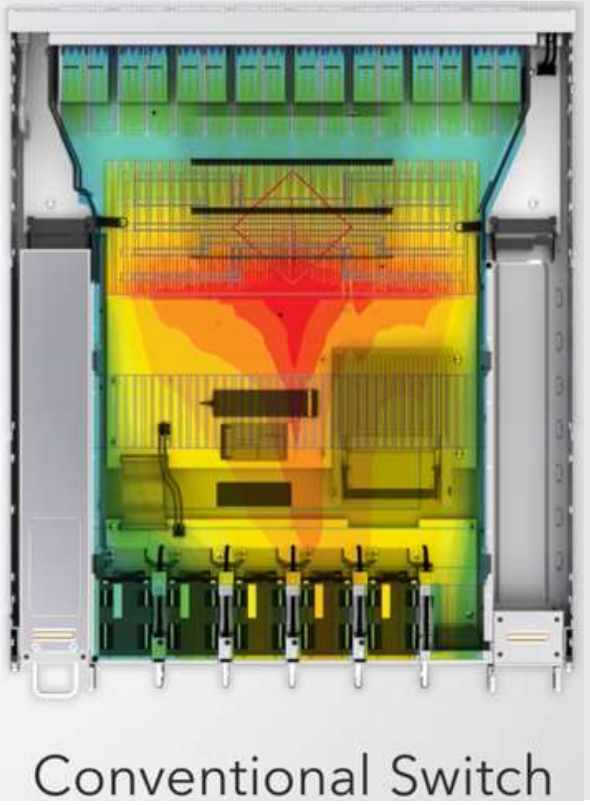


High–speed contacts directly soldered to Eye Speed® ultra low skew twinax

Cable Management Benefit



Flyover® Technology

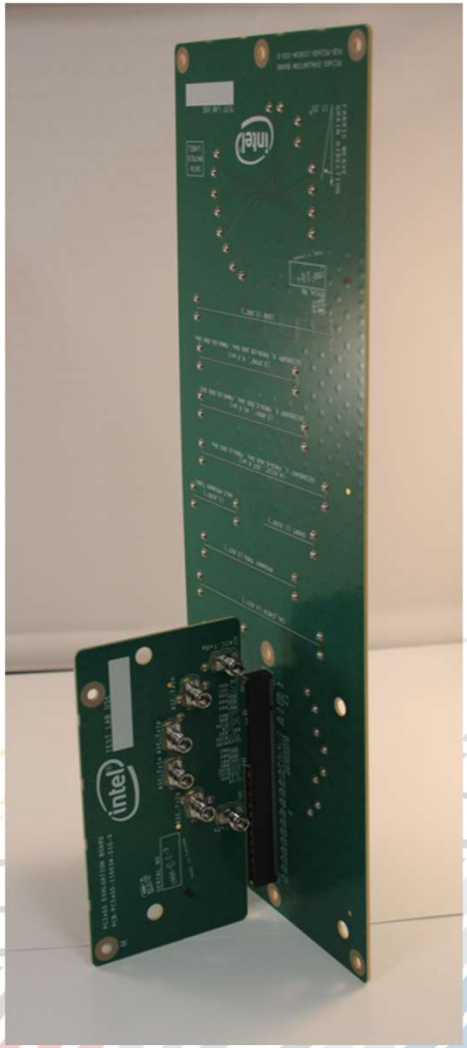


Conventional Switch

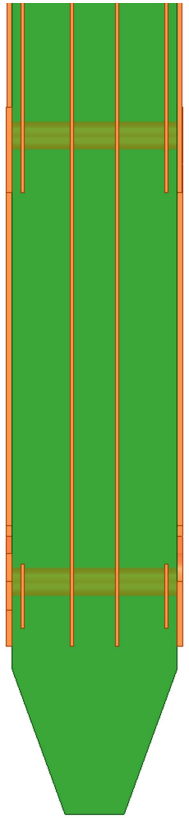
PCIe5 connector Characterization and Correlation

- Each kit consists of one a mated set of boards with fixtures
- PCB-110034 consists of a x16 PCIE-G5 connector where 7 differential pairs are routed to 2.4mm test points.
- P/N# PCIE-G5-16-01-X-DP-A_SAM
- 2.4mm female test points P/N# 0733870020
- Results are de-embedded and 1.0mm of 85 ohm trace remains
- Surface route of PCB contains inherent measurable FEXT that cannot be removed by de-embedding

Assembled Test Kit

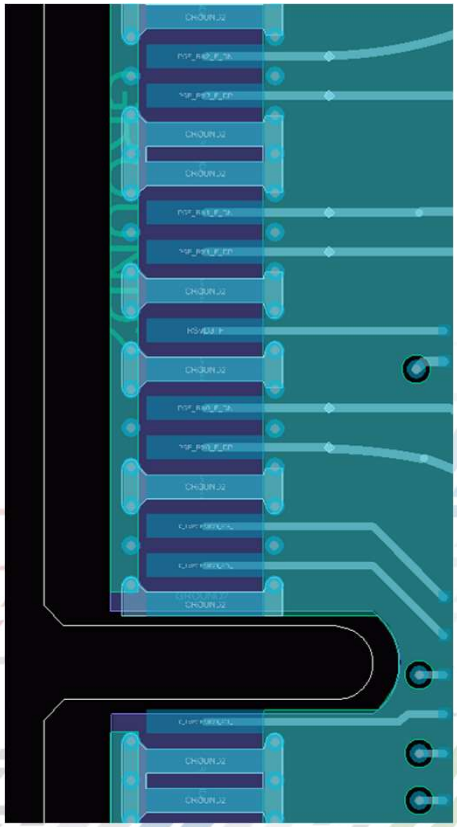


Cross Section

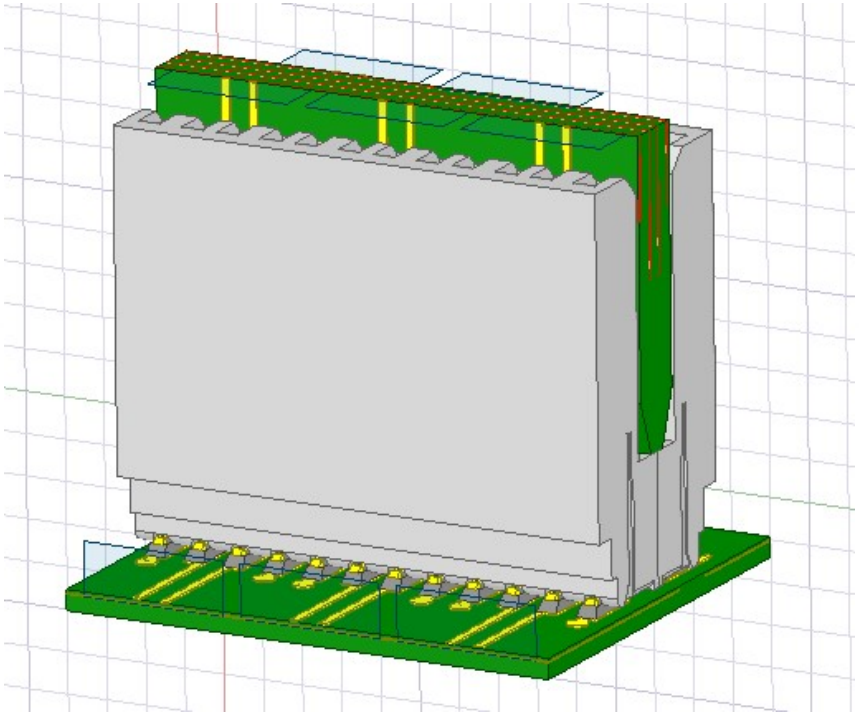


Stack Up:

Layer Number	LayerName	Material	Thickness	
			mils	mm
	TOP_SM	PSR-4000-BN	0.71	0.018
1	TOP	PLATED COPPER (0_5oz)	2.6	0.066
	CORE01	MEGTRON6 R-5775G (1x3313) (54%) C	3.94	0.1
2	P02	COPPER (0_5oz) VLP2	0.59	0.015
	DIEL01	MEGTRON6 R-5670G (1x1078) (72%) PP	3.9	0.099
	CORE02	MEGTRON6 R-5775G (2x3313) (54%) C	7.87	0.2
	DIEL02	MEGTRON6 R-5670G (1x1078) (72%) PP	3.9	0.099
3	P03	COPPER (0_5oz) VLP2	0.59	0.015
	CORE03	MEGTRON6 R-5775G (4x3313) (54%) C	15.75	0.4
4	P04	COPPER (0_5oz) VLP2	0.59	0.015
	DIEL03	MEGTRON6 R-5670G (1x1078) (72%) PP	3.9	0.099
	CORE04	MEGTRON6 R-5775G (2x3313) (54%) C	7.87	0.2
	DIEL04	MEGTRON6 R-5670G (1x1078) (72%) PP	3.9	0.099
5	P05	COPPER (0_5oz) VLP2	0.59	0.015
	CORE05	MEGTRON6 R-5775G (1x3313) (54%) C	3.94	0.1
6	BOTTOM	PLATED COPPER (0_5oz)	2.6	0.066
	BOTTOM_SM	PSR-4000-BN	0.71	0.018
		Total thickness over solder mask and plated copper	63.95	1.624



PCIE-G5 Model Geometry:



- NR_2021-0329_PCIE-G5_4x2_28p.s28p
- HFSS 2020 R1
- 0 to 50GHz, 10MHz Steps
- 1mm Microstrip PCB fixture included
- S-parameter Reference 50 ohms, Plots referenced to 42.5 ohms

S-parameter Pin Map

Part Name	PCIE-G5 High Speed Edge Card
Part#	PCIE-G5-04-01-X-DP-A-XX

Column

Row	B(Tx)	A(Rx)
12	12B(Tx)	12A(Rx)
13	13B(Tx)	13A(Rx)
14	14B(Tx)	14A(Rx)
15	15B(Tx)	15A(Rx)
16	16B(Tx)	16A(Rx)
17	17B(Tx)	17A(Rx)
18	18B(Tx)	18A(Rx)
19	19B(Tx)	19A(Rx)
20	20B(Tx)	20A(Rx)
21	21B(Tx)	21A(Rx)
22	22B(Tx)	22A(Rx)
23	23B(Tx)	23A(Rx)
24	24B(Tx)	24A(Rx)
25	25B(Tx)	25A(Rx)
26	26B(Tx)	26A(Rx)
27	27B(Tx)	27A(Rx)
28	28B(Tx)	28A(Rx)
29	29B(Tx)	29A(Rx)
30	30B(Tx)	30A(Rx)
31	31B(Tx)	31A(Rx)
32	32B(Tx)	32A(Rx)

Side 1
Baseboard

Diff Port #	Pin Name	Port #
1	14B	1
	15B	2
2	19B	3
	20B	4
3	23B	5
	24B	6
4	27B	7
	28B	8
5	16A	9
	17A	10
6	21A	11
	22A	12
7	25A	13
	26A	14

S-Parameters

Side 2
Edge Card

Port #	Pin Name	Diff Port #
15	14B	8
16	15B	
17	19B	9
18	20B	
19	23B	10
20	24B	
21	27B	11
22	28B	
23	16A	12
24	17A	
25	21A	13
26	22A	
27	25A	14
28	26A	

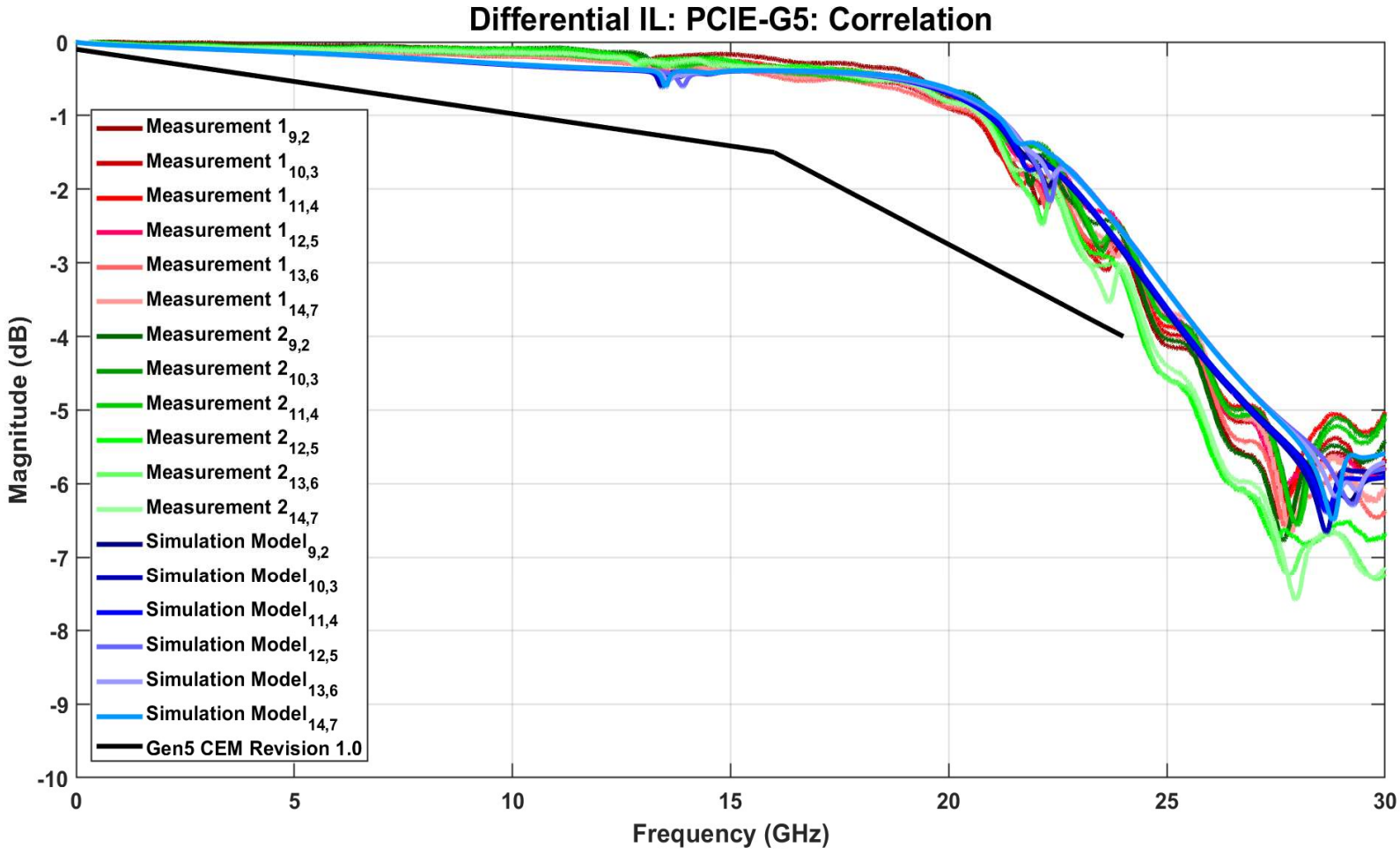
x	Ground pin
x x	Routed Pair
x	Terminated Pin
x	No Connect
x	Grounded Signal Pin

Part Name	PCIE-G5 High Speed Edge Card
Part#	PCIE-G5-04-01-X-DP-A-XX

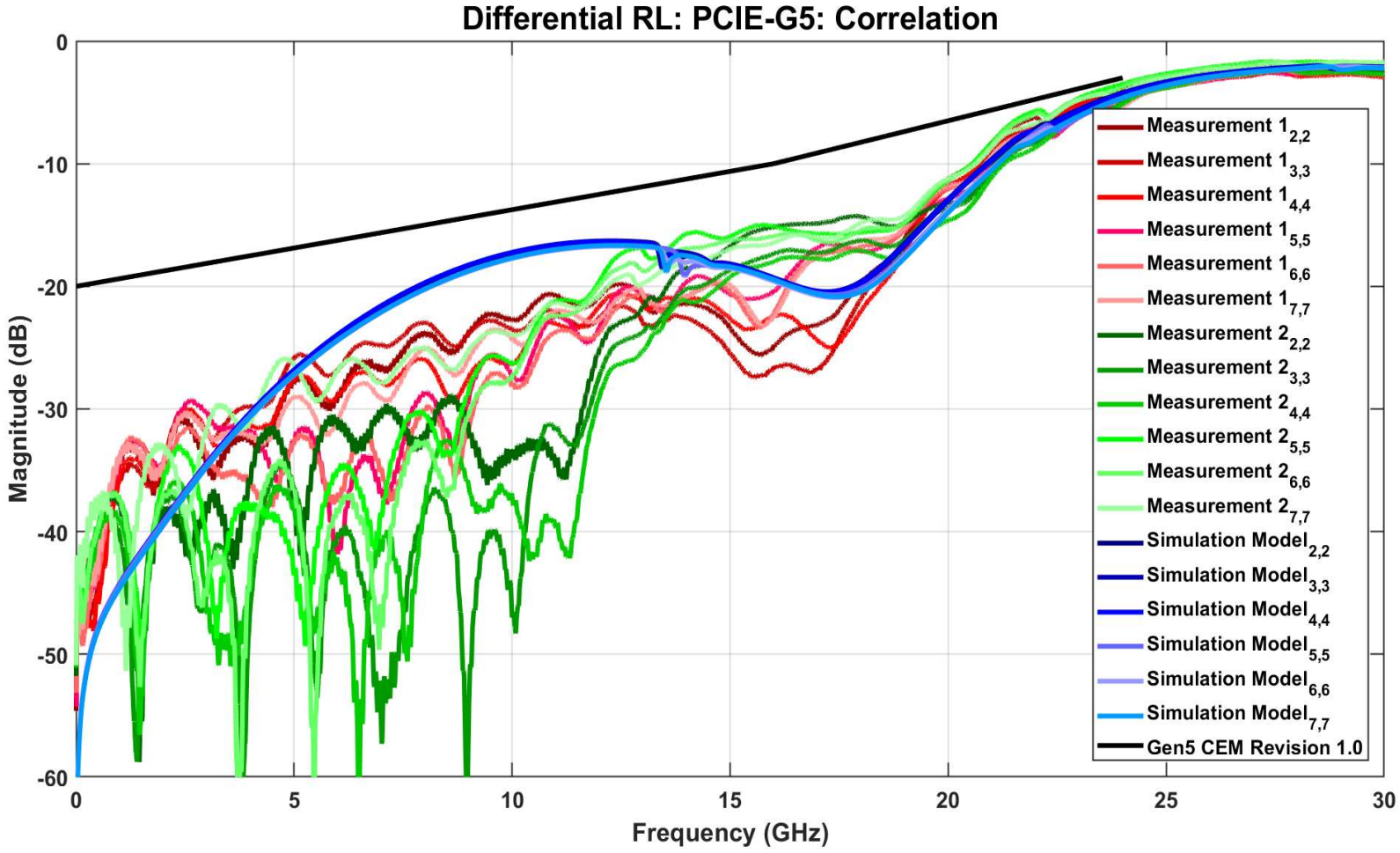
Column

Row	B(Tx)	A(Rx)
12	12B(Tx)	12A(Rx)
13	13B(Tx)	13A(Rx)
14	14B(Tx)	14A(Rx)
15	15B(Tx)	15A(Rx)
16	16B(Tx)	16A(Rx)
17	17B(Tx)	17A(Rx)
18	18B(Tx)	18A(Rx)
19	19B(Tx)	19A(Rx)
20	20B(Tx)	20A(Rx)
21	21B(Tx)	21A(Rx)
22	22B(Tx)	22A(Rx)
23	23B(Tx)	23A(Rx)
24	24B(Tx)	24A(Rx)
25	25B(Tx)	25A(Rx)
26	26B(Tx)	26A(Rx)
27	27B(Tx)	27A(Rx)
28	28B(Tx)	28A(Rx)
29	29B(Tx)	29A(Rx)
30	30B(Tx)	30A(Rx)
31	31B(Tx)	31A(Rx)
32	32B(Tx)	32A(Rx)

Differential Insertion Loss:



Differential Return Loss:



Crosstalk NEXT Pin Map:

Part Name	PCIE-G5 High Speed Edge Card
Part#	PCIE-G5-04-01-X-DP-A-XX

Column

Row	B(Tx)	A(Rx)
12	12B(Tx)	12A(Rx)
13	13B(Tx)	13A(Rx)
14	14B(Tx)	14A(Rx)
15	15B(Tx)	15A(Rx)
16	16B(Tx)	16A(Rx)
17	17B(Tx)	17A(Rx)
18	18B(Tx)	18A(Rx)
19	19B(Tx)	19A(Rx)
20	20B(Tx)	20A(Rx)
21	21B(Tx)	21A(Rx)
22	22B(Tx)	22A(Rx)
23	23B(Tx)	23A(Rx)
24	24B(Tx)	24A(Rx)
25	25B(Tx)	25A(Rx)
26	26B(Tx)	26A(Rx)
27	27B(Tx)	27A(Rx)
28	28B(Tx)	28A(Rx)
29	29B(Tx)	29A(Rx)
30	30B(Tx)	30A(Rx)
31	31B(Tx)	31A(Rx)
32	32B(Tx)	32A(Rx)

2 Aggressors

Side 1
Baseboard

Diff Port #	Pin Name	Port #
1	14B	1
	15B	2
2	19B	3
	20B	4
3	23B	5
	24B	6
4	27B	7
	28B	8
5	16A	9
	17A	10
6	21A	11
	22A	12
7	25A	13
	26A	14

S-Parameters

Side 2
Edge Card

Port #	Pin Name	Diff Port #
15	14B	8
16	15B	
17	19B	9
18	20B	
19	23B	10
20	24B	
21	27B	11
22	28B	
23	16A	12
24	17A	
25	21A	13
26	22A	
27	25A	14
28	26A	

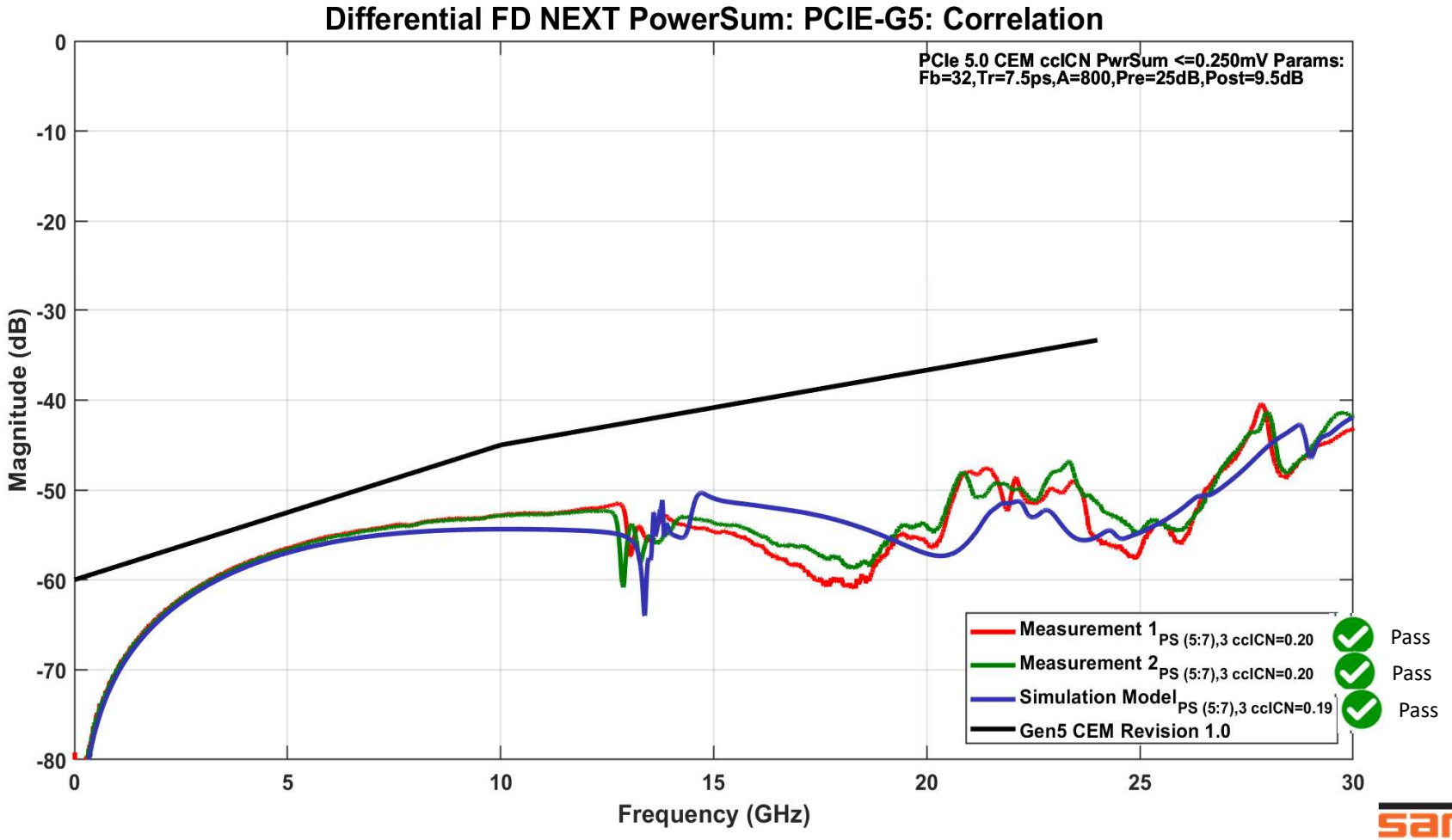
x	Ground pin
x x	Routed Pair
x	Terminated Pin
x	No Connect
x	Grounded Signal Pin

Part Name	PCIE-G5 High Speed Edge Card
Part#	PCIE-G5-04-01-X-DP-A-XX

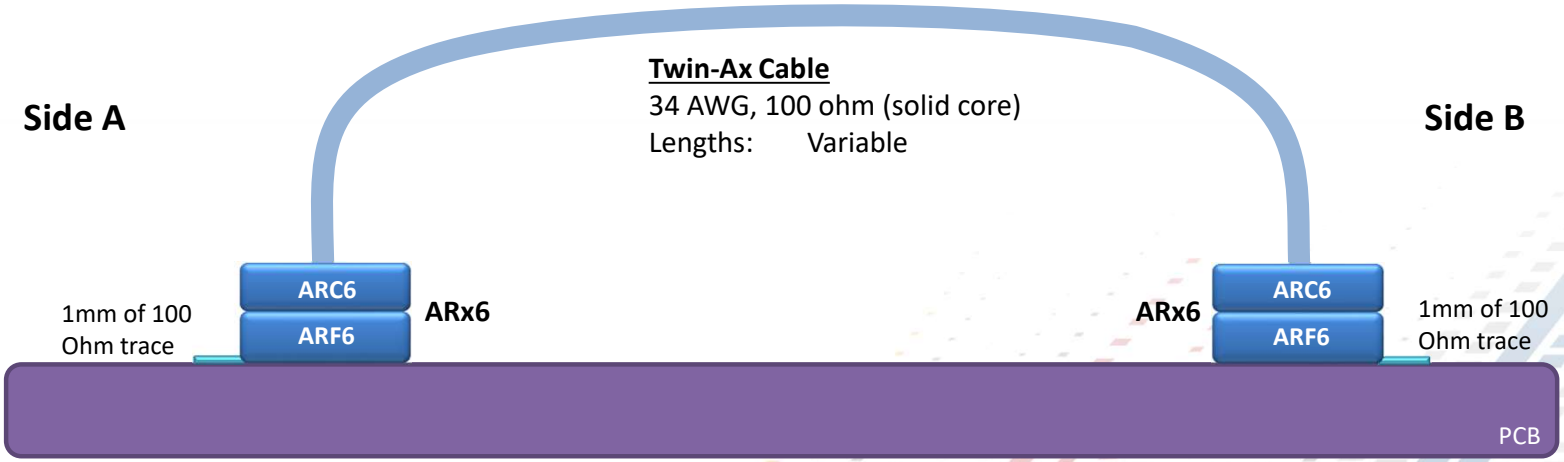
Column

	B(Tx)	A(Rx)
12	12B(Tx)	12A(Rx)
13	13B(Tx)	13A(Rx)
14	14B(Tx)	14A(Rx)
15	15B(Tx)	15A(Rx)
16	16B(Tx)	16A(Rx)
17	17B(Tx)	17A(Rx)
18	18B(Tx)	18A(Rx)
19	19B(Tx)	19A(Rx)
20	20B(Tx)	20A(Rx)
21	21B(Tx)	21A(Rx)
22	22B(Tx)	22A(Rx)
23	23B(Tx)	23A(Rx)
24	24B(Tx)	24A(Rx)
25	25B(Tx)	25A(Rx)
26	26B(Tx)	26A(Rx)
27	27B(Tx)	27A(Rx)
28	28B(Tx)	28A(Rx)
29	29B(Tx)	29A(Rx)
30	30B(Tx)	30A(Rx)
31	31B(Tx)	31A(Rx)
32	32B(Tx)	32A(Rx)

Differential FD NEXT: Power Sum



Modeled Cable Assembly



Applicable Part #'s

ARC6-16-XX.X-XX-XX-2-1 or ARC6-16-XX.X-XX-XX-3-1 mated with ARF6-16-X-X-X-X-XX
and
ARC6-24-XX.X-XX-XX-2-1 or ARC6-24-XX.X-XX-XX-3-1 mated with ARF6-24-X-X-X-X-XX

Model Port Mapping

Side A

PCB Footprint (Top View)

2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48	50	Pin#
G	17	18	G	19	20	G	21	22	G	23	24	G	25	26	G	27	28	G	29	30	G	31	32	G	Port #
G	1	2	G	3	4	G	5	6	G	7	8	G	9	10	G	11	12	G	13	14	G	15	16	G	Port #
1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47	49	Pin#

Side B

PCB Footprint (Top View)

2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48	50	Pin#
G	48	47	G	46	45	G	44	43	G	42	41	G	40	39	G	37	36	G	36	35	G	34	33	G	Port #
G	64	63	G	62	61	G	60	59	G	58	57	G	56	55	G	54	53	G	52	51	G	50	49	G	Port #
1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47	49	Pin#

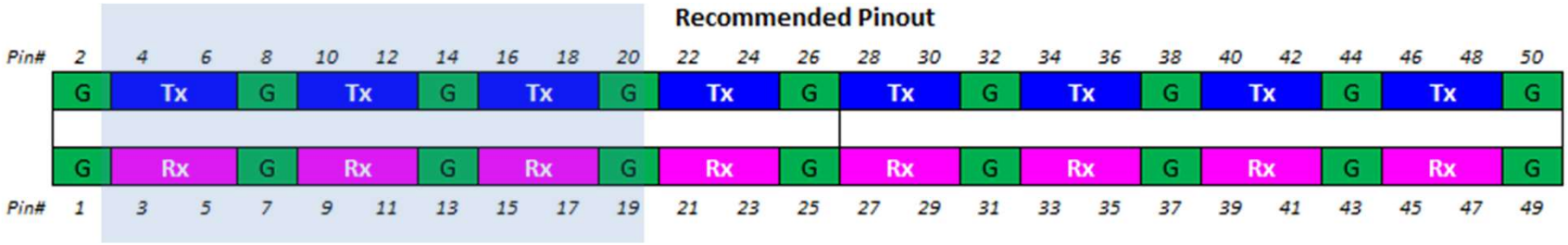
G = Ground

Wiring option -3 shown, models are also applicable to the -2 ARC6 wiring option due to connector symmetry.

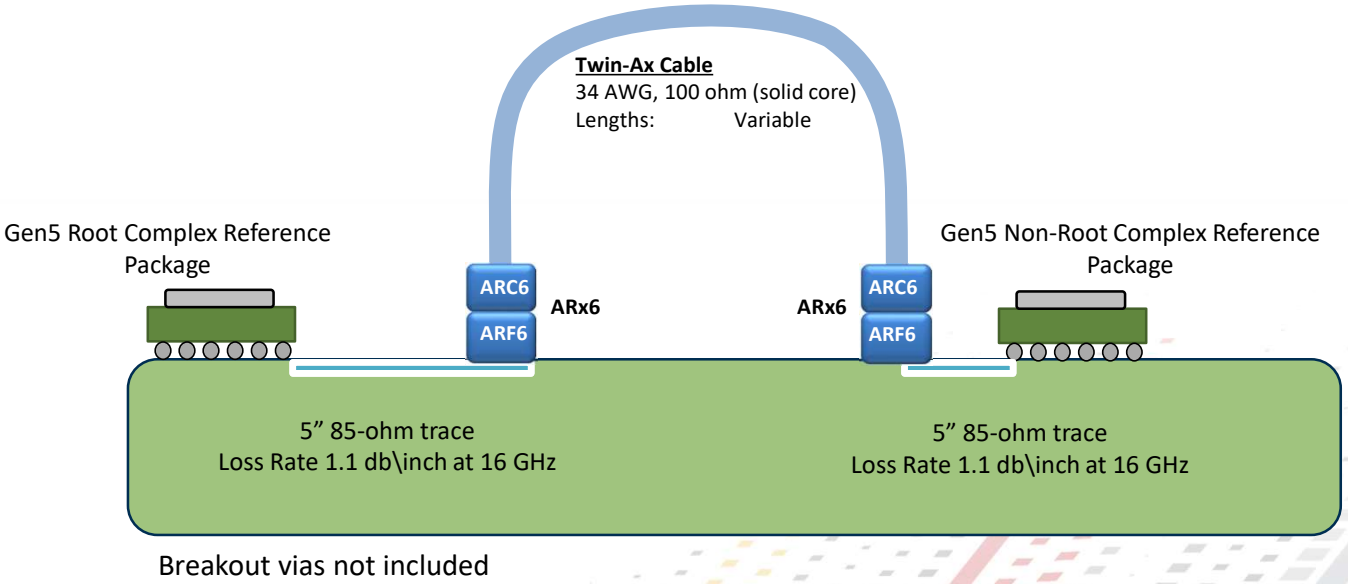
Channel Simulation with Recommended Pinout:

- It is recommended to split Transmit and Receive signal pairs on to separate rows as shown in the example below.

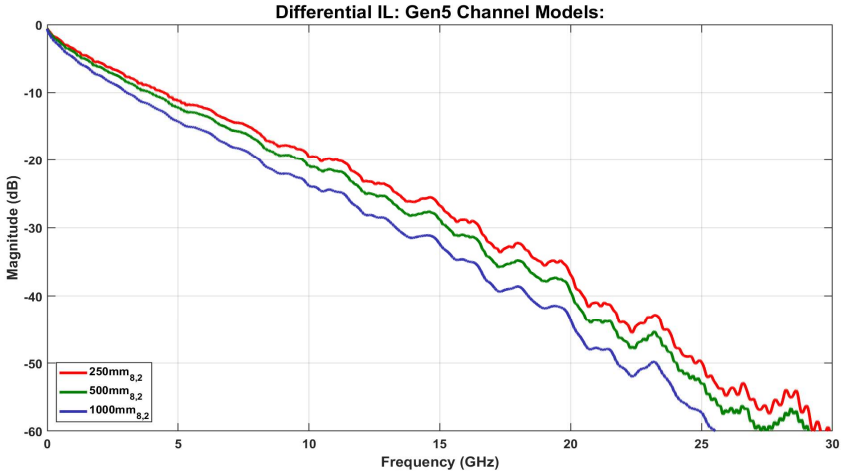
24 Port Simulation

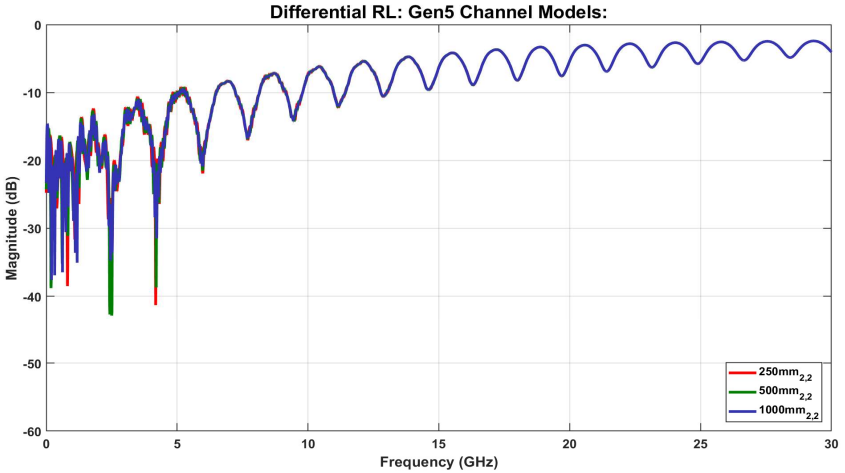


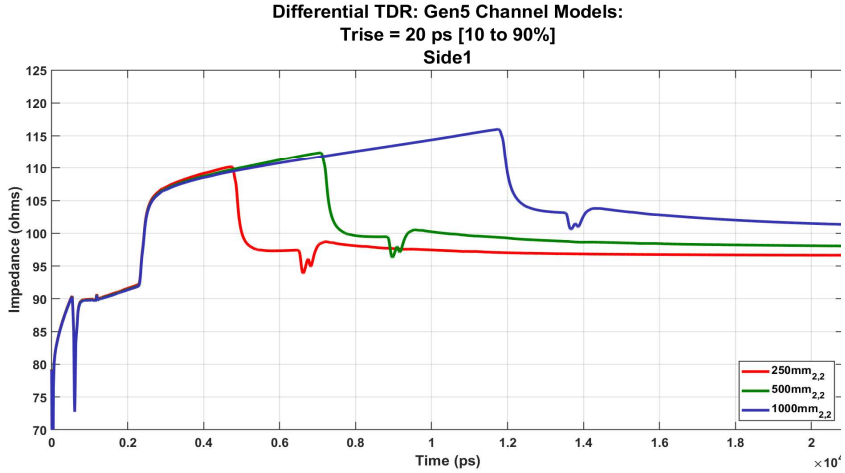
Configuration for PCIE Gen 5 Channel Simulation:

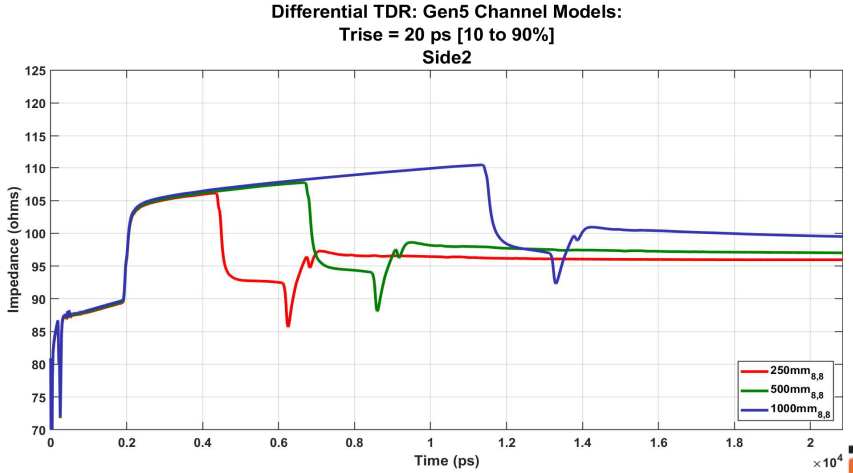


Gen5 Channel Response:

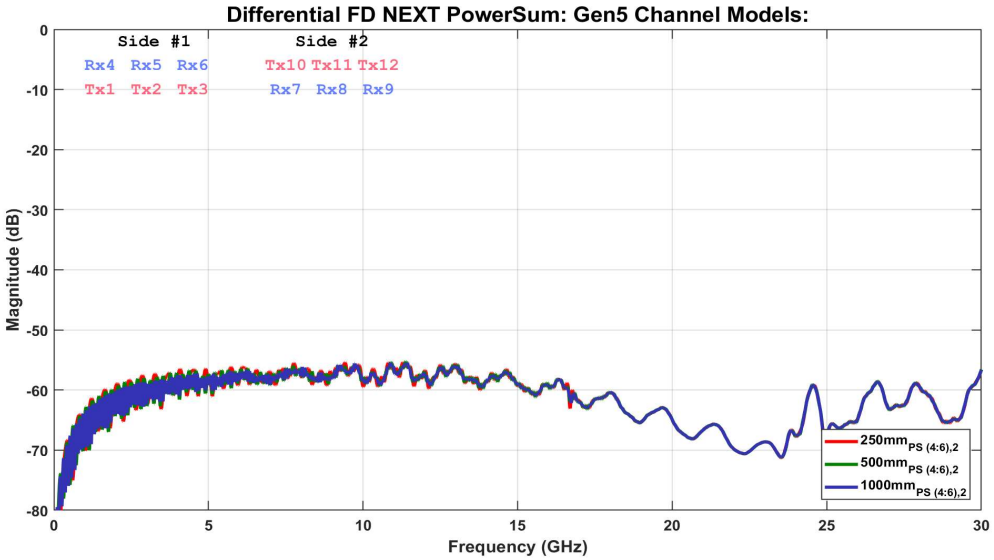


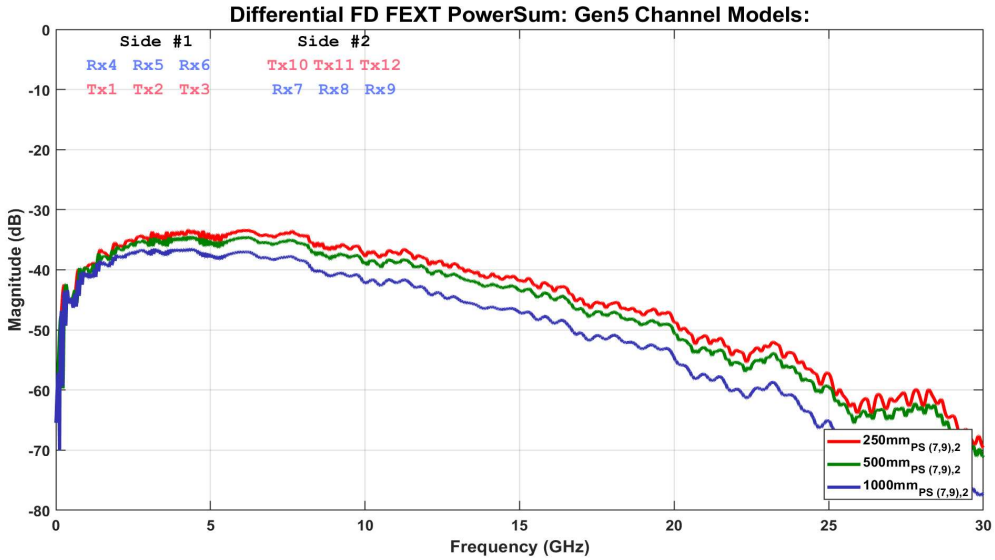




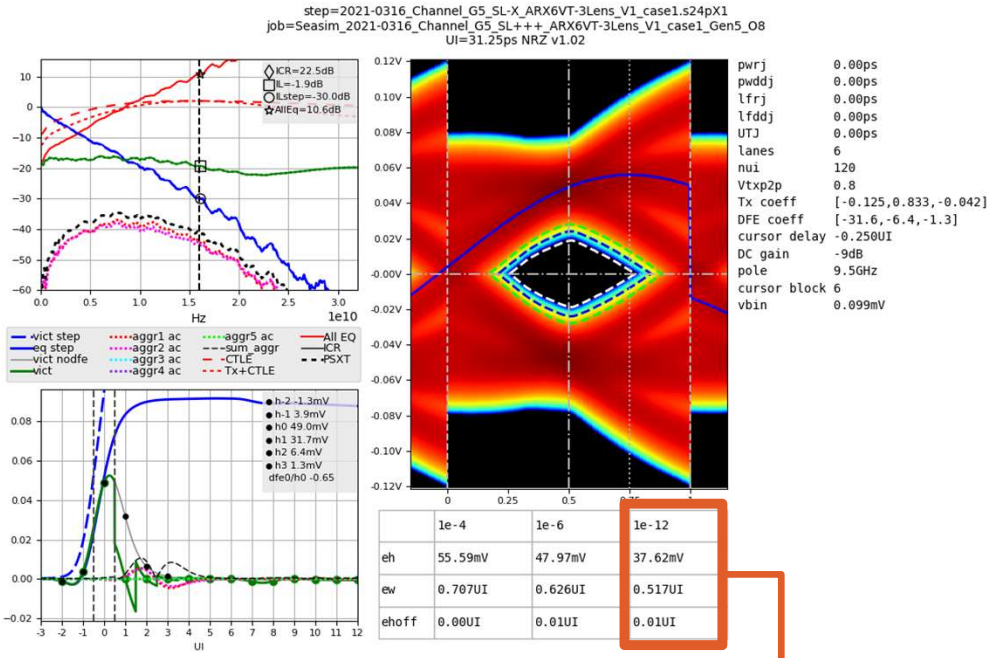


Gen5 Channel Response:

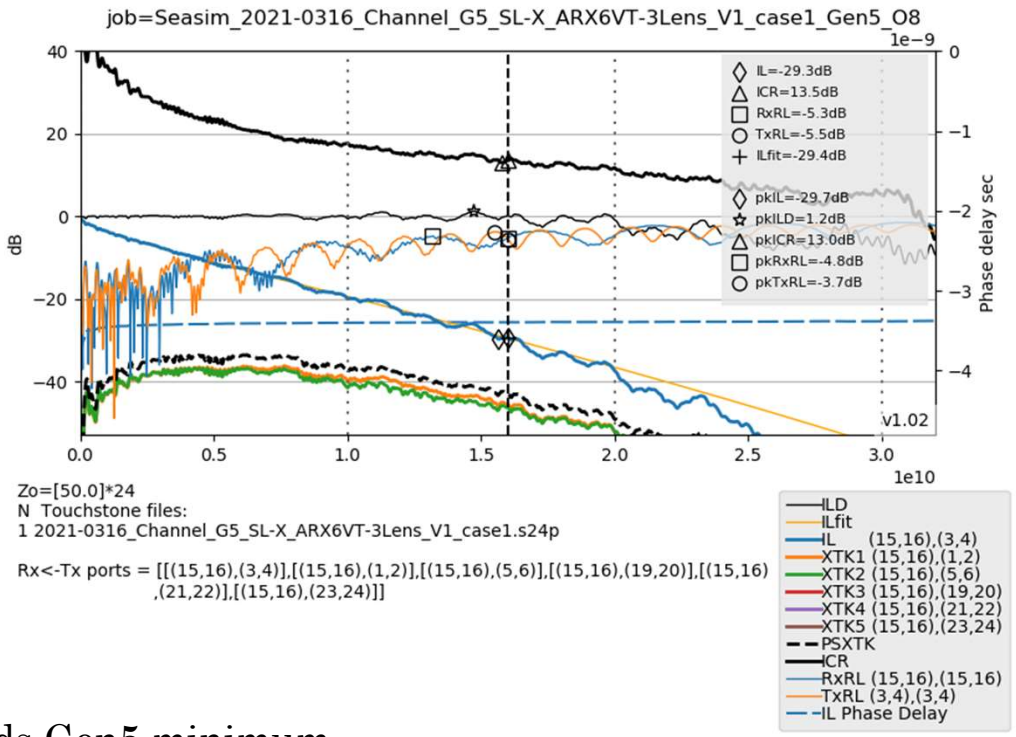




Gen5 Channel Simulation Results: 250mm

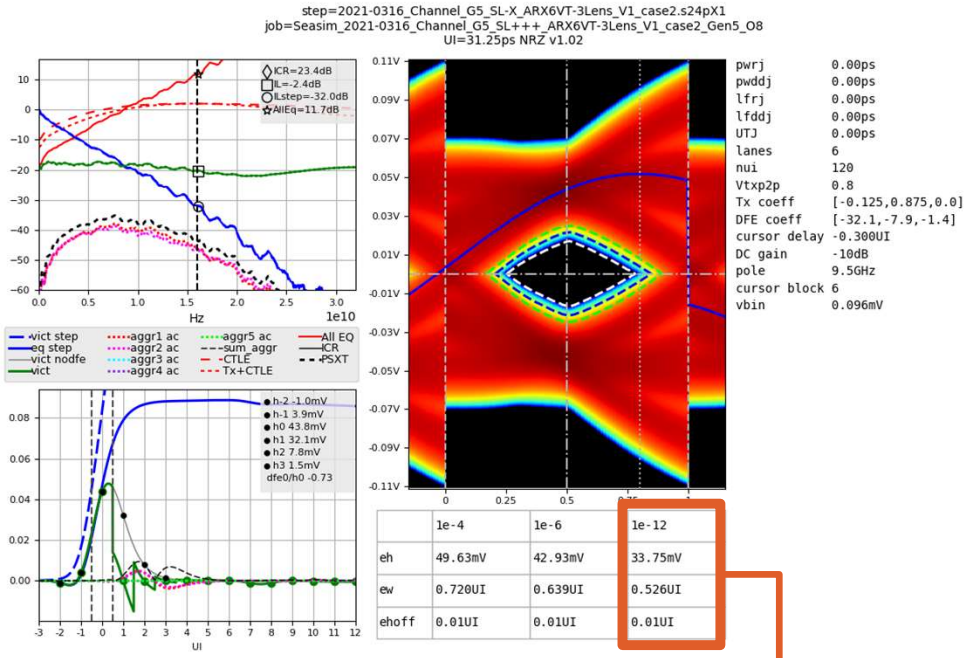


	1e-4	1e-6	1e-12
eh	55.59mV	47.97mV	37.62mV
ew	0.707UI	0.626UI	0.517UI
ehoff	0.00UI	0.01UI	0.01UI

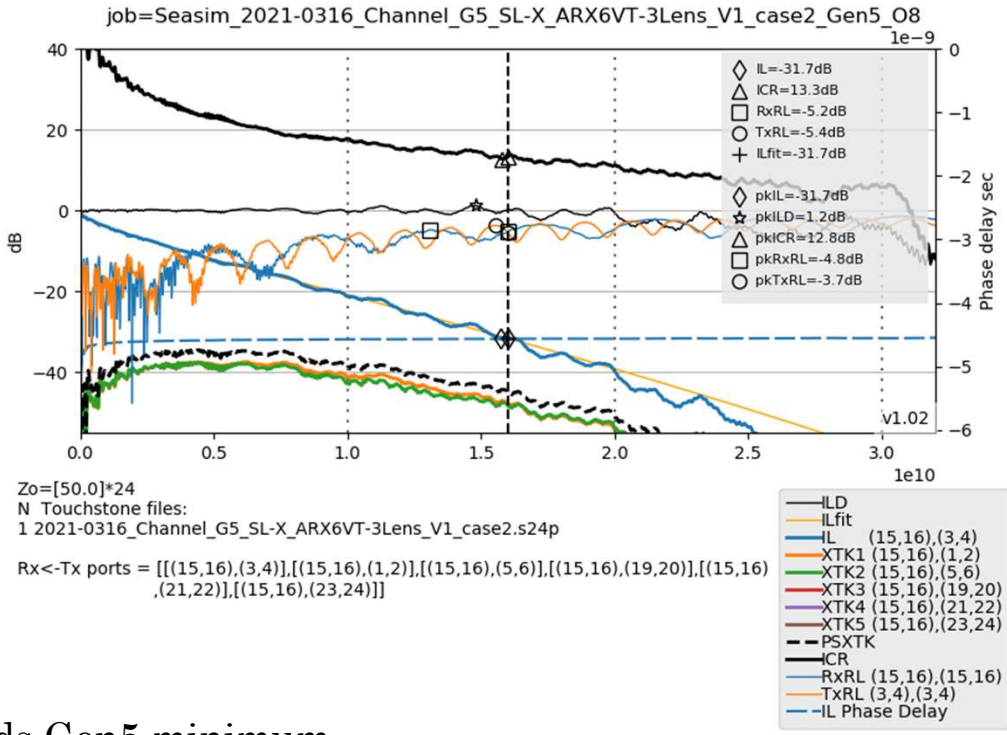


Exceeds Gen5 minimum requirement 15mV and 0.30UI

Gen5 Channel Simulation Results: 500mm

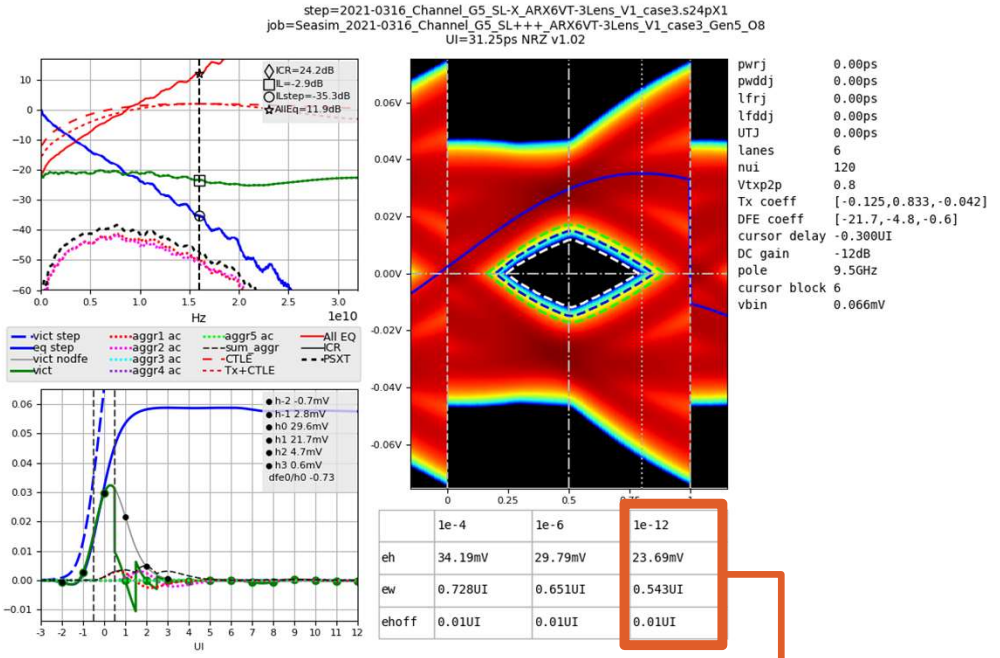


	1e-4	1e-6	1e-12
eh	49.63mV	42.93mV	33.75mV
ew	0.720UI	0.639UI	0.526UI
ehoff	0.01UI	0.01UI	0.01UI

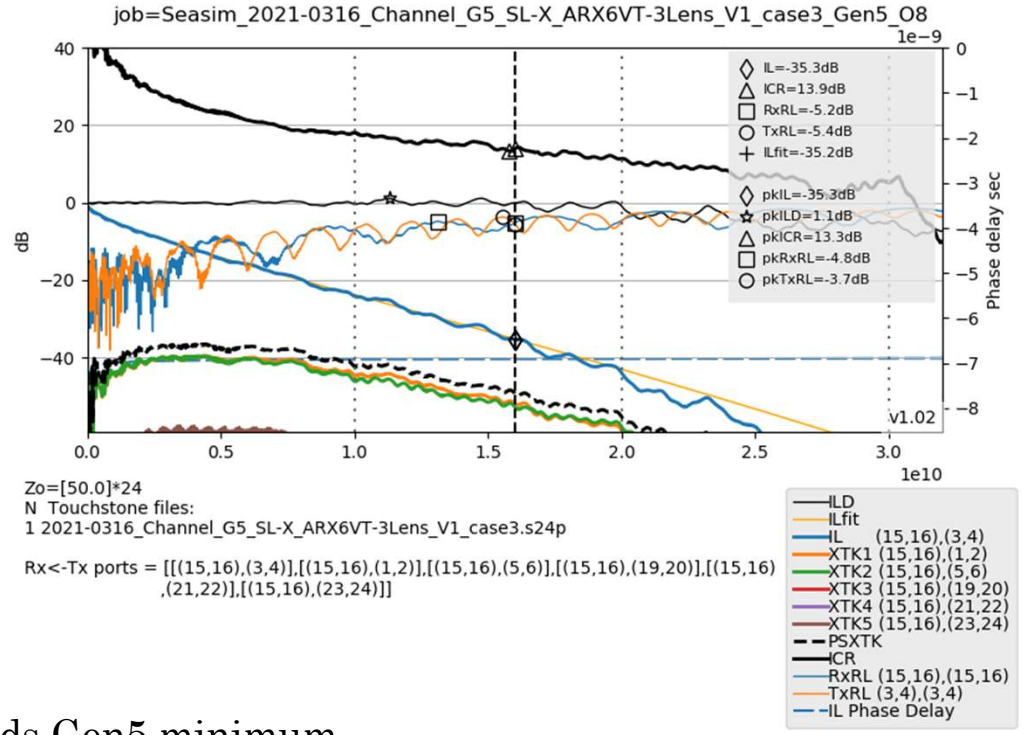


Exceeds Gen5 minimum requirement 15mV and 0.30UI

Gen5 Channel Simulation Results: 1000mm

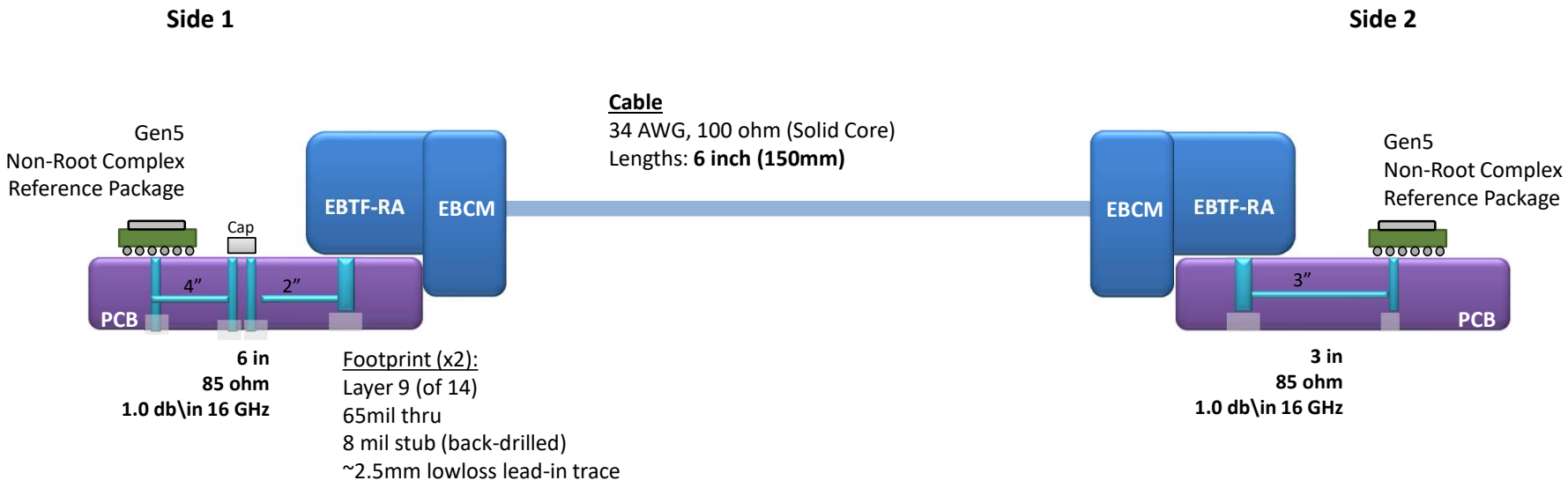


	1e-4	1e-6	1e-12
eh	34.19mV	29.79mV	23.69mV
ew	0.728UI	0.651UI	0.543UI
ehoff	0.01UI	0.01UI	0.01UI

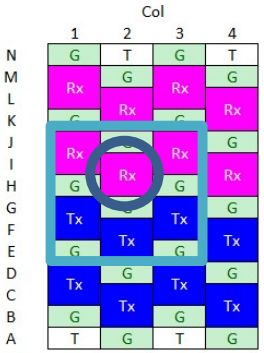


Exceeds Gen5 minimum requirement 15mV and 0.30UI

EBTX for PCIe Gen5 Channel Analysis:

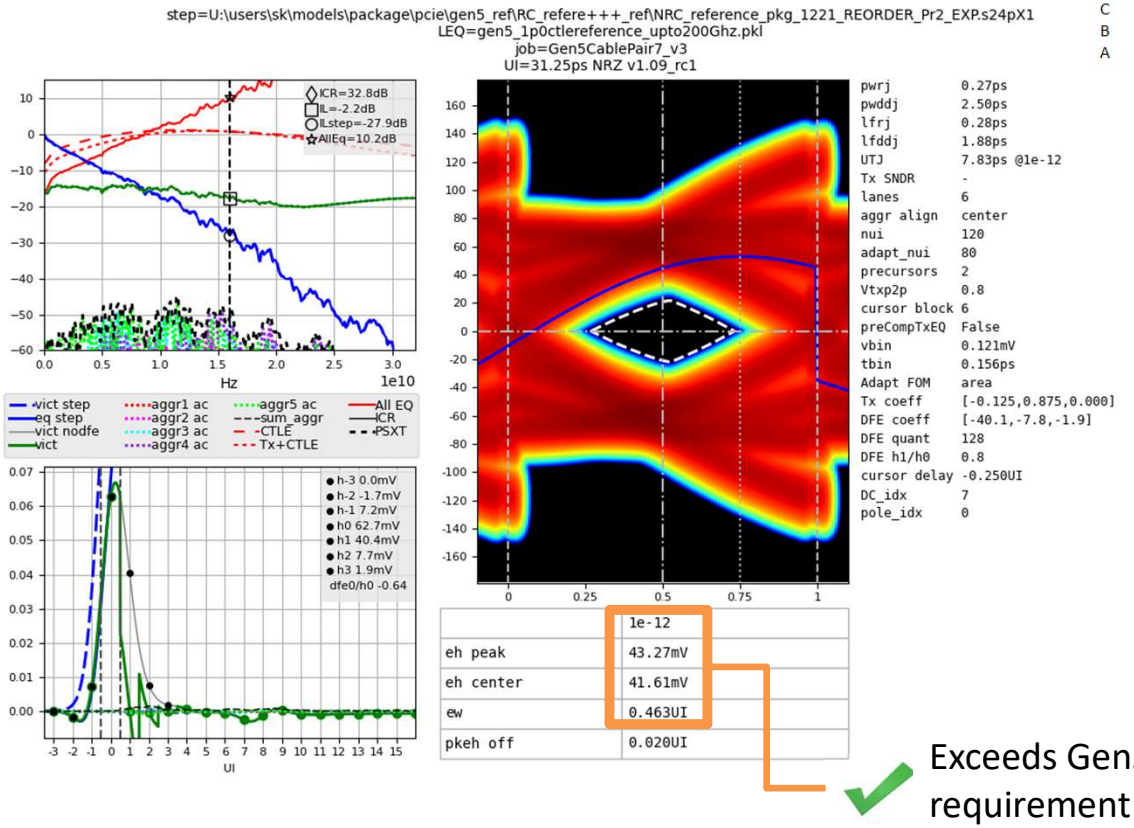


PCIe Gen5 Channel Analysis:



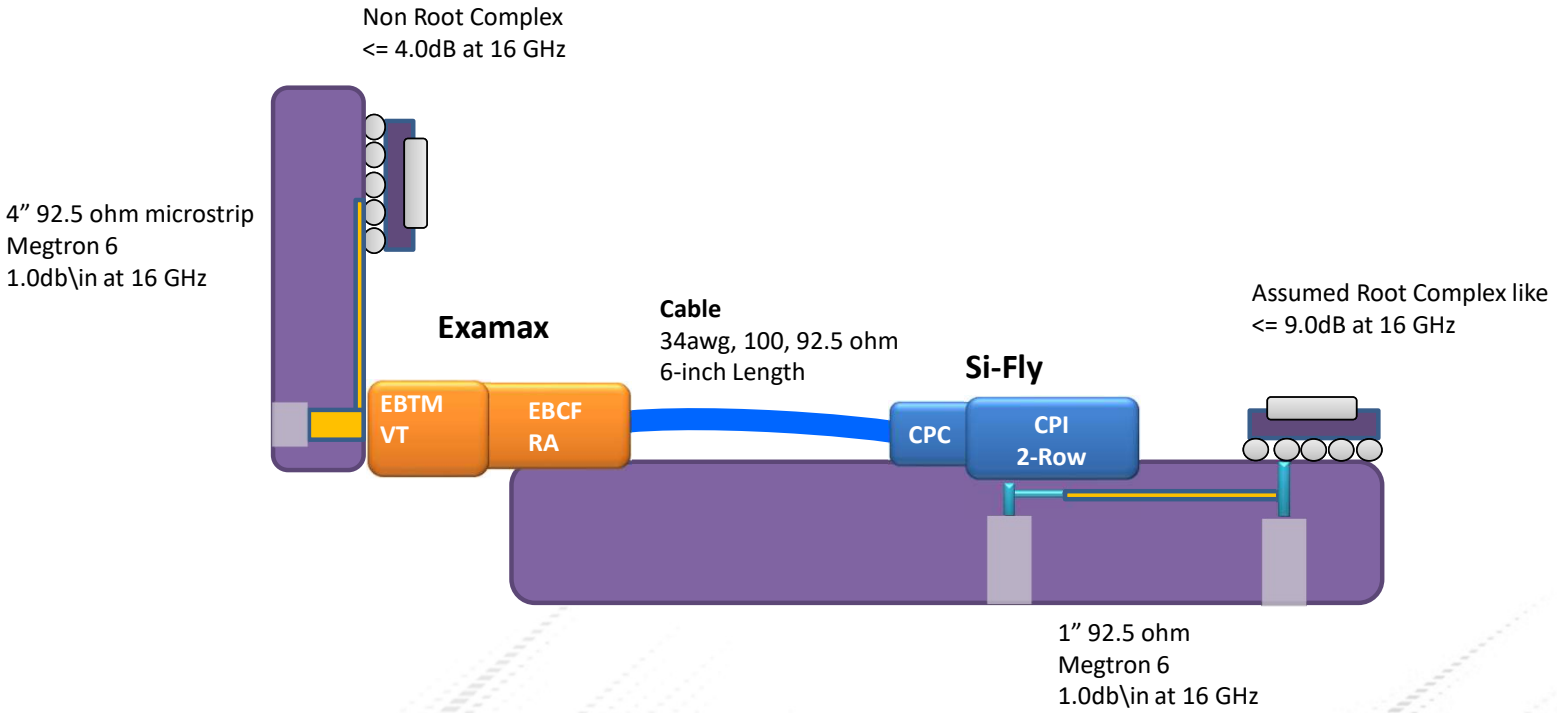
6 Pairs in Channel Simulation
Eye Opening on HI2

Middle of loss range and highest NEXT Crosstalk



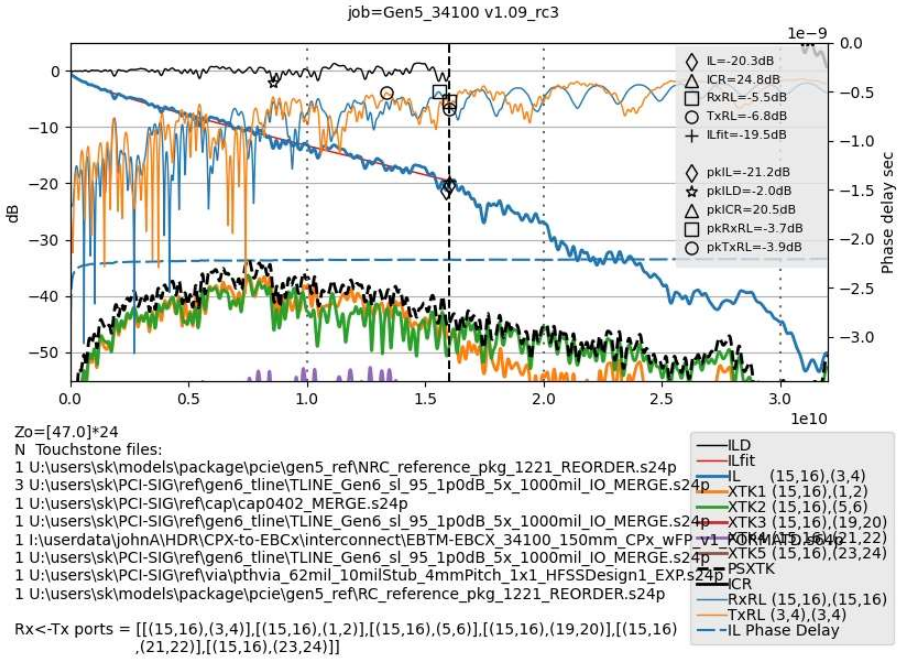
Exceeds Gen5 minimum requirement 15mV and 0.30UI

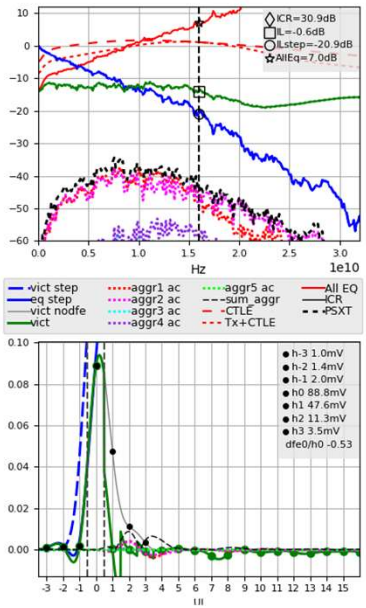
EBTx+ Si-Fly Channel Topology:

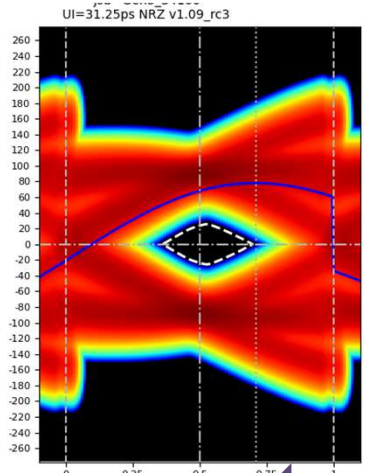


Gen5 Channel Simulation: 34-100 Cable

92.5 ohm PCB (95 ohm substituted)





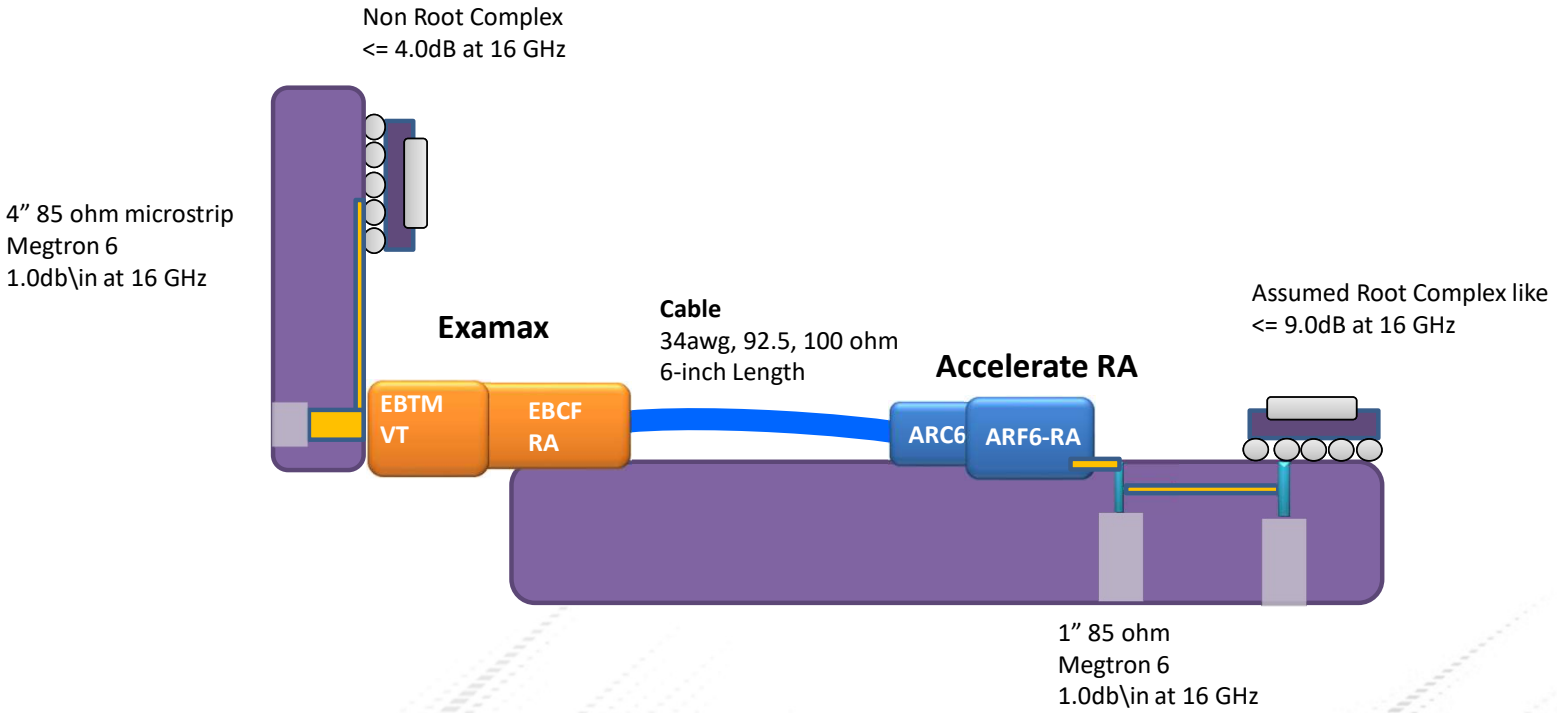


pwrj	0.27ps
pwdj	2.50ps
lfrj	0.28ps
lfdj	1.88ps
UTJ	7.83ps @1e-12
Tx SNDR	34.0dB
lanes	6
aggr align	center
nui	120
adapt_nui	80
precursors	3
Vtxp2p	0.8
cursor block	6
preCompTxEQ	False
vbin	0.160mV
tbin	0.156ps
Adapt FOM	area
TxFIR h1/h0	[0.55,0.50,0.45]
TxFIR quant	24
Tx coeff	[0.042,-0.167,0.792,0.000]
DFE coeff	[-47.2,-11.1,-4.2]
DFE quant	64
DFE h1/h0	0.8
cursor delay	-0.210UI
DC_idx	10
pole_idx	0

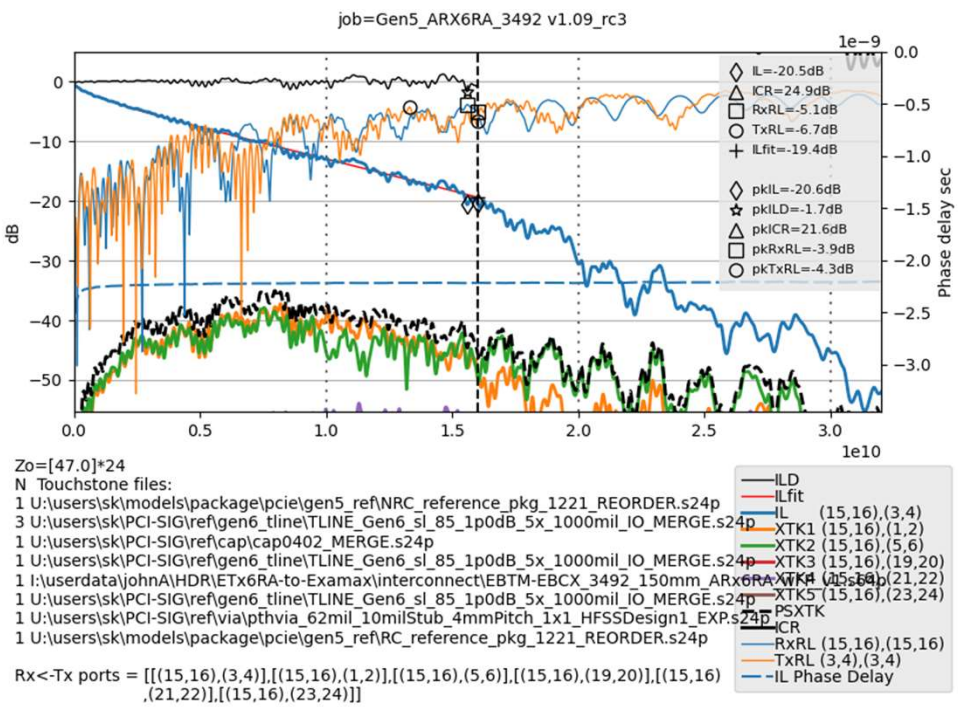
	1e-12
eh peak	51.16mV
eh center	47.60mV
ew	0.336UI
pkeh off	0.025UI

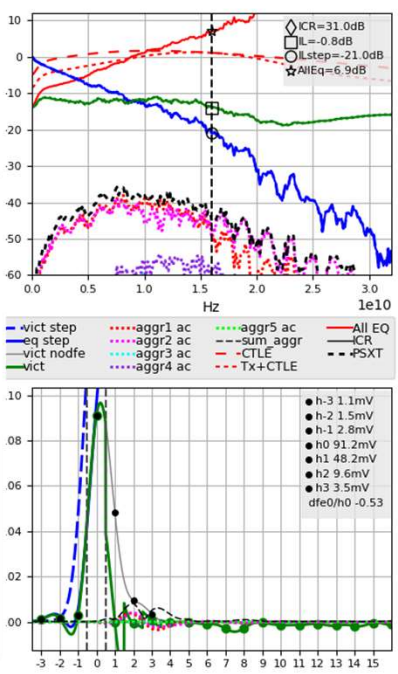
Exceeds 15mV\0.3UI Requirement

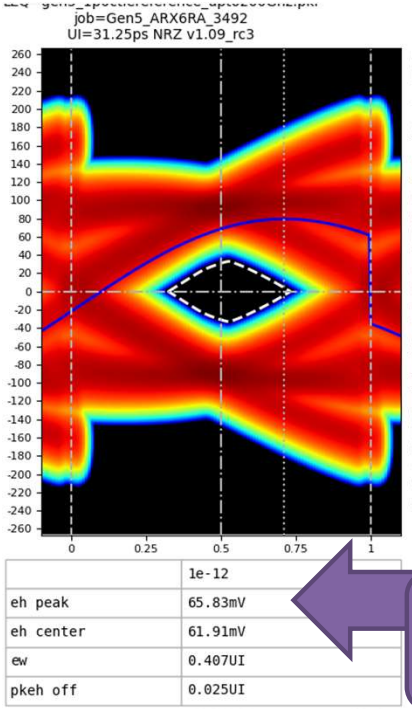
EBTx+ ARC6 Channel Topology:



Gen5 Channel Simulation: 34-92 Cable







pwrj	0.27ps
pwdj	2.50ps
lfrj	0.28ps
lfdj	1.88ps
UTJ	7.83ps @1e-12
Tx SNDR	34.0dB
lanes	6
aggr align	center
nui	120
adapt_nui	80
precursors	3
Vtxp2p	0.8
cursor block	6
preCompTxEQ	False
vbin	0.161mV
tbin	0.156ps
Adapt FOM	area
TxFIR h1/h0	[0.55,0.50,0.45]
TxFIR quant	24
Tx coeff	[0.042,-0.167,0.792,0.000]
DFE coeff	[-48.4,-10.0,-2.9]
DFE quant	64
DFE h1/h0	0.8
cursor delay	-0.210UI
DC_idx	10
pole_idx	0

	1e-12
eh peak	65.83mV
eh center	61.91mV
ew	0.407UI
pkeh off	0.025UI

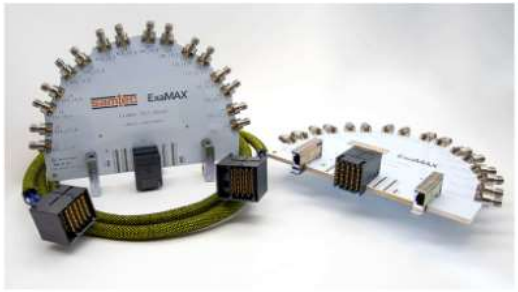
Exceeds 15mV\0.3UI Requirement

BOARD-TO-BOARD/ SI EVALUATION KITS:

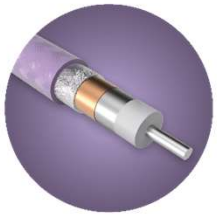



CABLE / SI EVALUATION KITS



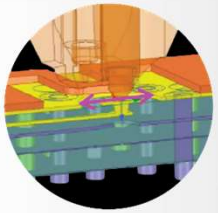


Microwave / Millimeter Wave Cable Assemblies & Interconnects



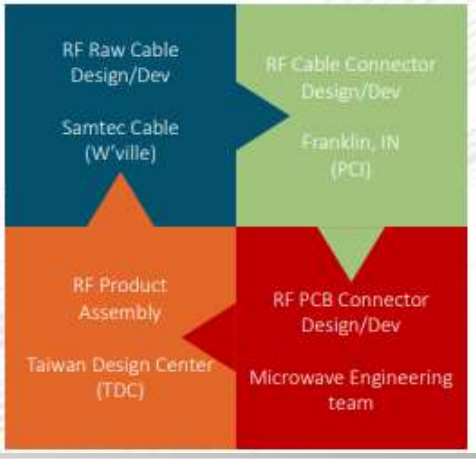
CABLES
Design & Fabrication
of Raw Cable
Cable Assemblies

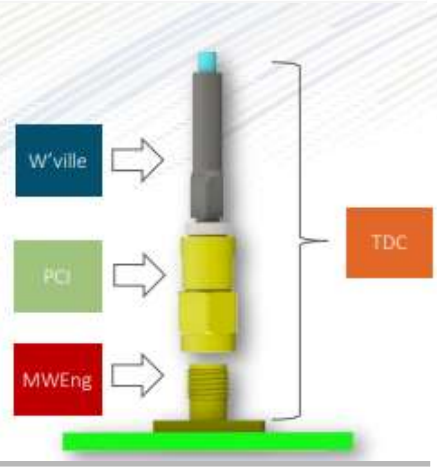
CONNECTORS
Design & Fabrication
Cable Connectors
Board Connectors



TECH SUPPORT
Launch Optimization
Simulation & Testing
Full System Optimization

Vertical Integration
=
Full System Support





PRECISION RF | Cable Assemblies, Board & Cable Connectors

1.00 mm
- DC to 110 GHz

1.35 mm
- DC to 90 GHz

1.85 mm
- DC to 65 GHz

SMPM/ SMP
- SMPM: DC to 65 GHz
- / SMP: DC to 40 GHz

2.40 mm
- DC to 50 GHz

2.92 mm
- DC to 40 GHz

3.50 mm
- DC to 34 GHz

SMA/SSMA
- DC to 18GHz/
- 26 GHz

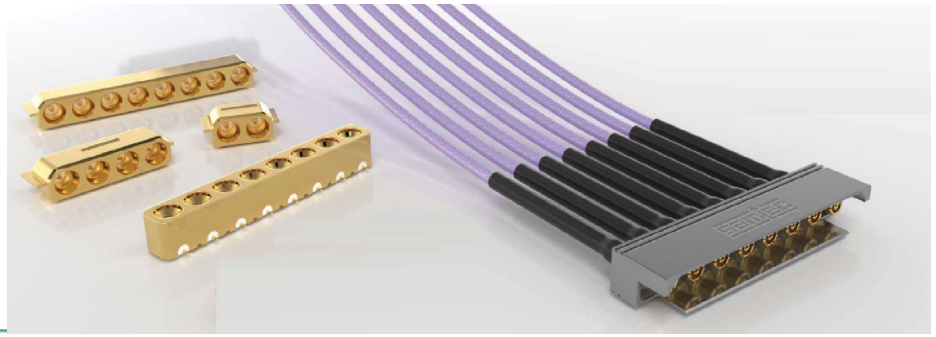
N
- DC to 18 GHz

samtec.com/PrecisionRF

GANGED SMPM SOLUTIONS

HIGH-DENSITY | SPACE-SAVING DESIGN | PUSH-ON

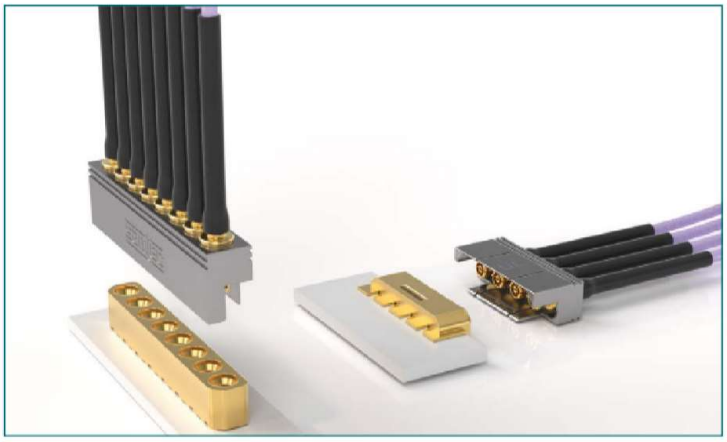
GC47+GPPC SERIES



Cable-to-Board

EDGE LAUNCH		VERTICAL LAUNCH	
Mated Sets		Mated Sets	
Block, Edge Mount	GPPC-EM	Block, Surface Mount	GPPC-SL
Cable Assembly	GC47 or GC86	Cable Assembly	GC47 or GC86

- Cable assembly end 2 options: ganged or individual industry standard RF connectors
- Cable type: .047" or .086" low-loss flexible
- Pitch: 3.56 mm (.140"); single-row



BULLSEYE® TEST POINT SYSTEM

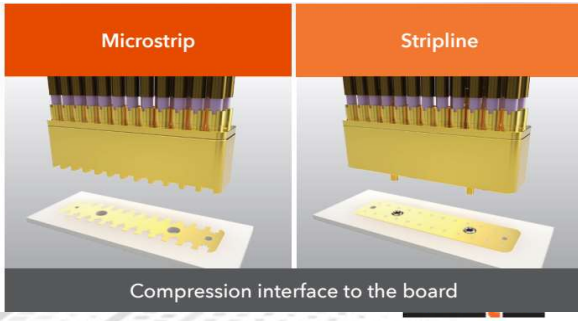
TEST AND MEASUREMENT

Performance **to 40/50/70 GHz**

HIGH-DENSITY • SPACE-SAVING DESIGN • SHORTER TRACE LENGTHS

Bulls Eye® High-Performance Test

- Compression interface to the board provides easy on/off and eliminates soldering costs
- High-density, space-saving design
- Enables smaller evaluation boards and shorter trace lengths
- Installation: While the attach process for each series is similar, each have unique specifications that need to be observed

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