DATA RATE EVOLUTION IN HIGH-SPEED TECHNOLOGIES AND CHALLENGES FOR HIGH-SPEED PCBS AND INTERCONNECTS WITH PCIE 5.0

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Make ideas real

DATA RATE EVOLUTION IN HIGH-SPEED DIGITAL EXAMPLE: PCIE

PCIe Spec.	Raw Bandwidth (per Lane)	Data Rate (Total)	Modulation NRZ / PAM	VNA BW requirement SOC test boards	VNA BW requirement (PCBs / Cable Assemblies)
…					
PCIe 4.0	16.0 Gbps	16.0 GT/s	NRZ	25GHz	20GHz
PCIe 5.0	32.0 Gbps	32.0 GT/s	NRZ	50GHz	40GHz
PCIe 6.0	64.0 Gbps	64.0 GT/s	PAM4	50GHz (spec. in progress)	40GHz (spec. in progress)
…					

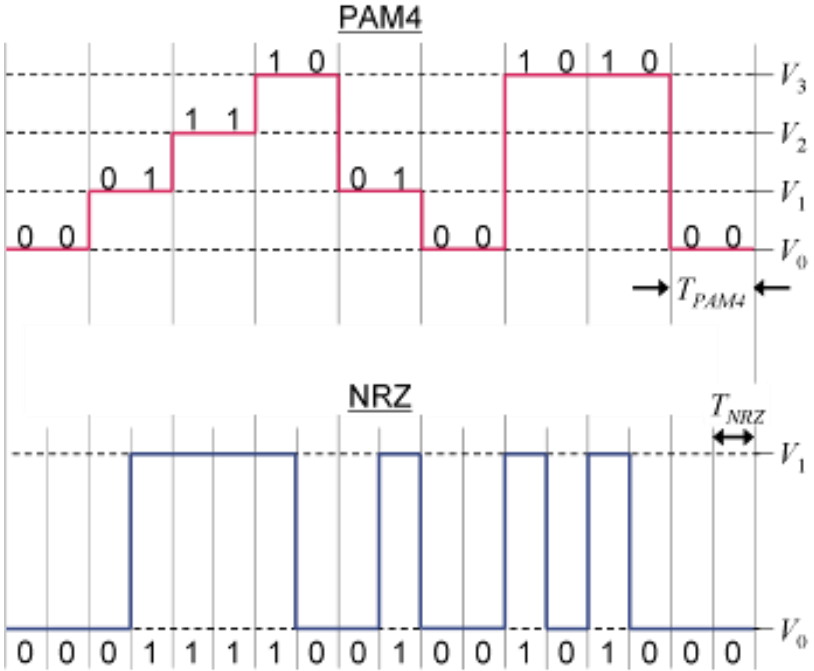
Note:

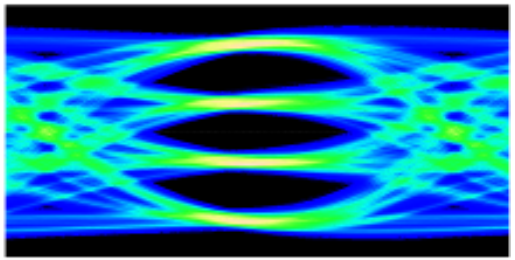
- GT/s = GTransfers / sec
- Gbps = Gbit / sec

DATA RATE EVOLUTION IN HIGH-SPEED DIGITAL EXAMPLE: IEEE 802.3

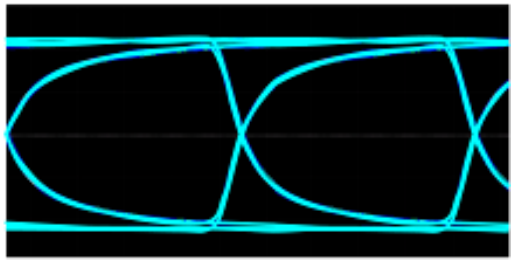
IEEE Spec.	Copper Cables	Backplanes	Signalling Bandwidth (per Lane)	Modulation NRZ / PAM	VNA BW requirement (PCBs / Cable Assemblies)
…	…	…	…		
802.3by 802.3bj	25GBASE-CR 100GBASE-CR4	25GBASE-KR 100GBASE-KR4	25Gbps	NRZ	25GHz
802.3cd	50GBASE-CR1 100GBASE-CR2 200GBASE-CR4	50GBASE-KR1 100GBASE-KR2 200GBASE-KR4	50Gbps	PAM4	26.56GHz
802.3ck	100GBASE-CR1 200GBASE-CR2 400GBASE-CR4	100GBASE-KR1 200GBASE-KR2 400GBASE-KR4	100Gbps	PAM4	50GHz (spec. in progress)
…					

MODULATION FORMATS: PAM4 VS. NRZ





$BW_{PAM4} = ½\ BW_{NRZ}$



Eye height for PAM4 is 1/3 of eye height for NRZ: 20 log (1/3) = -9.5 dB

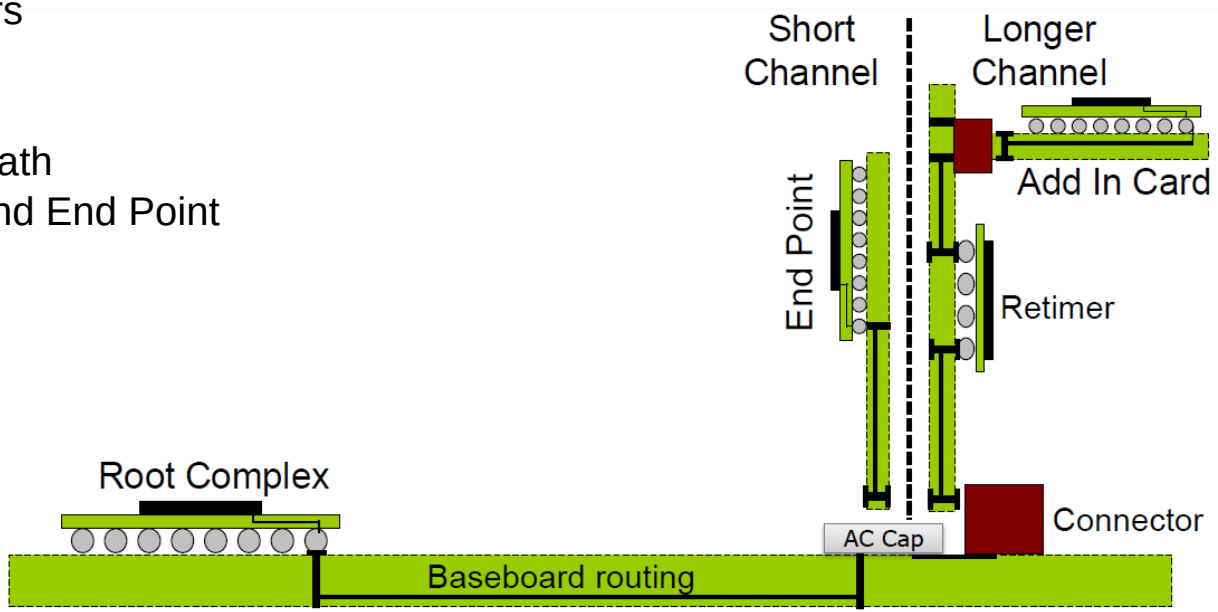
→ higher sensitivity to noise and crosstalk

REQUIREMENTS AND CHALLENGES FOR PCBS AND INTERCONNECTS IN PCIE 5.0 AND BEYOND

REQUIREMENTS AND CHALLENGES FOR PCBS AND INTERCONNECTS IN PCIE 5.0 AND BEYOND

- impedance mismatches - discontinuities at packages, vias, connectors

  Example: PCIe 5.0
  discontinuities on signal path
  between Root Complex and End Point

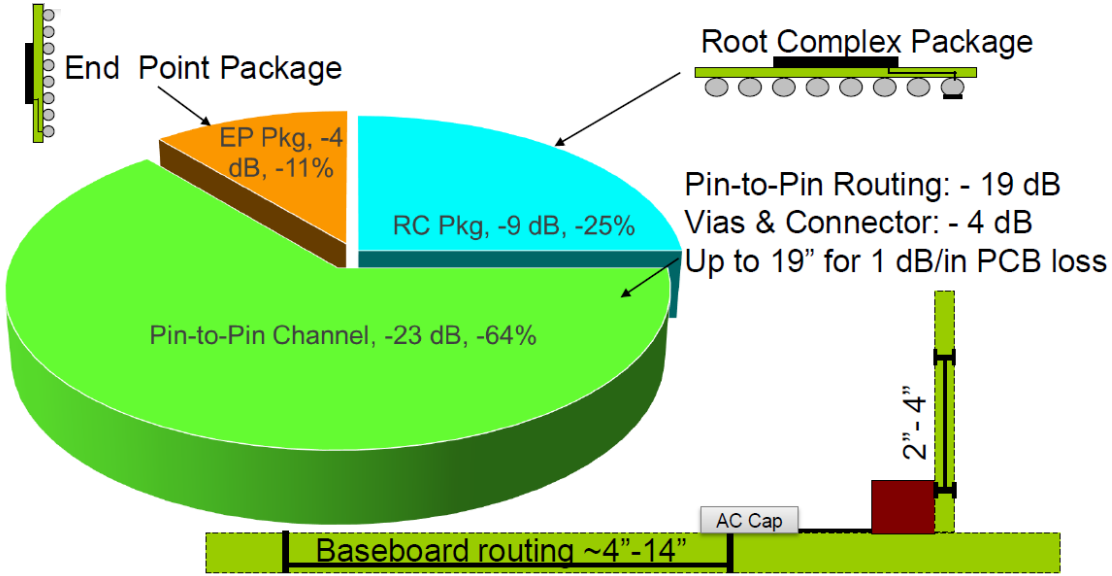


Source: PCI-SIG Developers Conference 2019; PCIe®5.0 Electrical Update

REQUIREMENTS AND CHALLENGES FOR PCBS AND INTERCONNECTS IN PCIE 5.0 AND BEYOND

- losses and frequency response of PCB material
  - PCB signal traces will be by-passed by cables (lower loss) example: Samtec Flyover

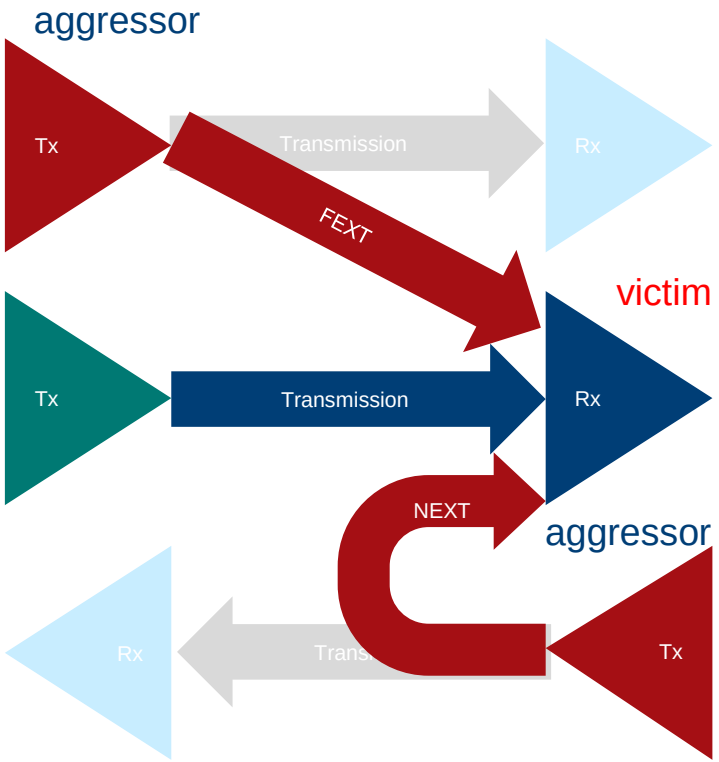
Example: PCIe 5.0
total loss budget:
36 dB @ 16GHz



Source: PCI-SIG Developers Conference 2019; PCIe®5.0 Electrical Update

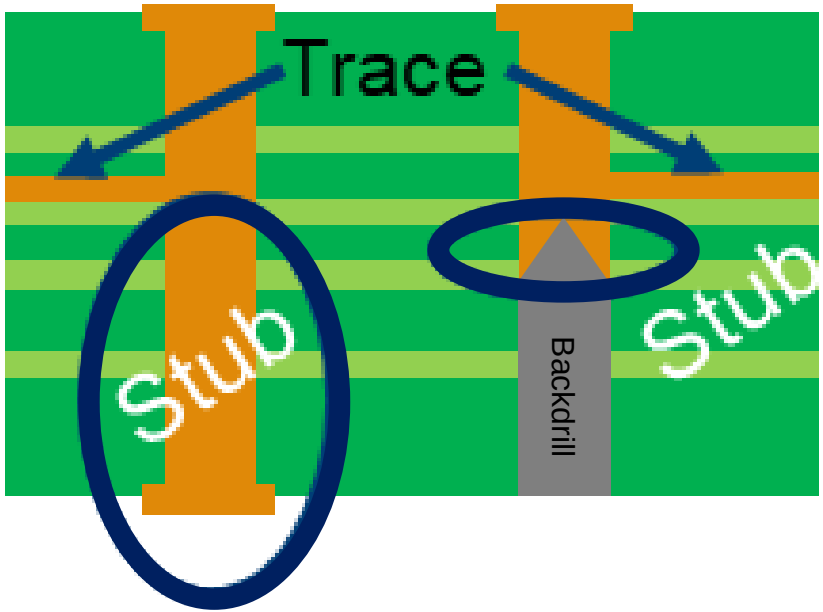
REQUIREMENTS AND CHALLENGES FOR PCBS AND INTERCONNECTS IN PCIE 5.0 AND BEYOND

- crosstalk:
  - near end crosstalk: NEXT
  - far end crosstalk: FEXT
- multiple aggressors: power sum
  - multi-disturber NEXT: MDNEXT
  - multi-disturber FEXT: MDFEXT



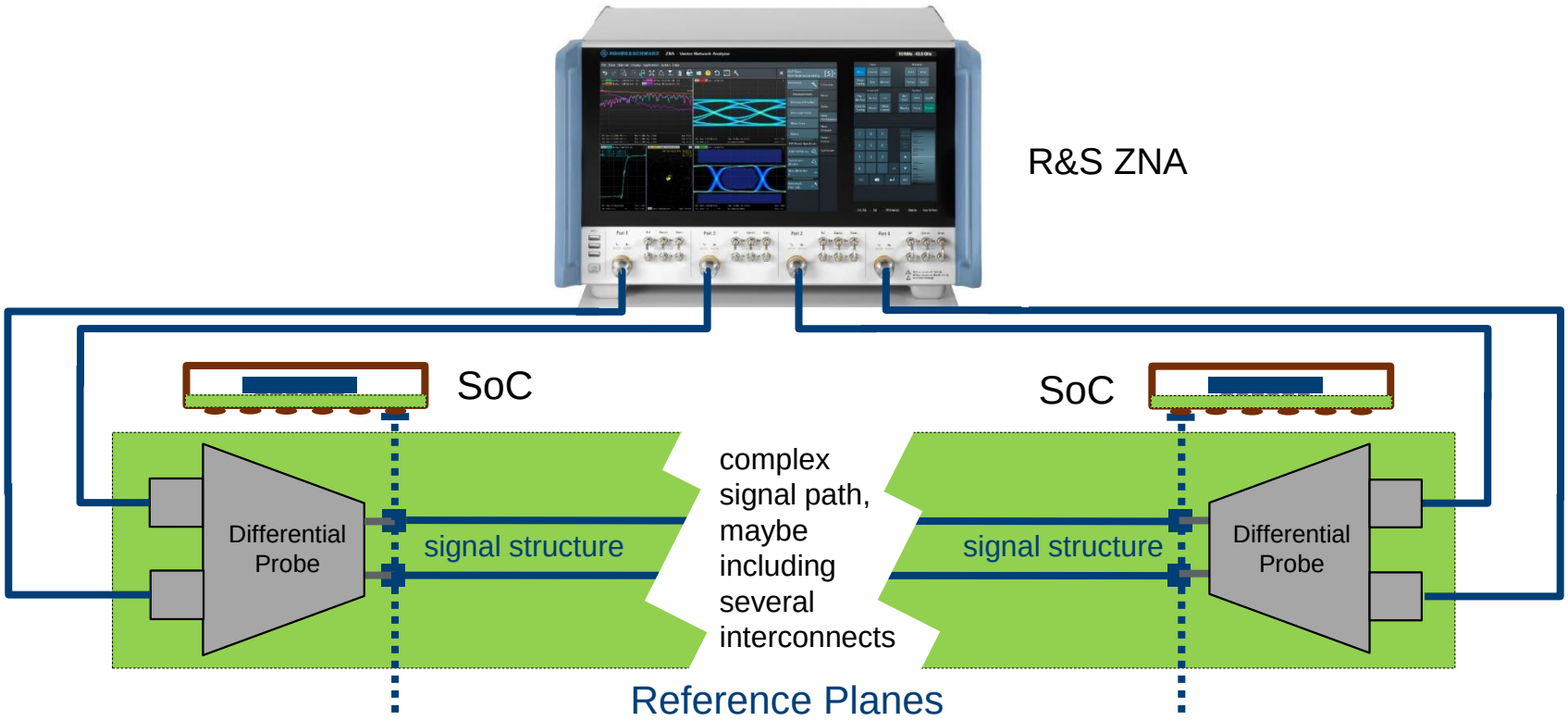
REQUIREMENTS AND CHALLENGES FOR PCBS AND INTERCONNECTS IN PCIE 5.0 AND BEYOND

- mitigate resonant structures, e.g.:
  - via stubs (→ backdrill)
  - fiber weave effects

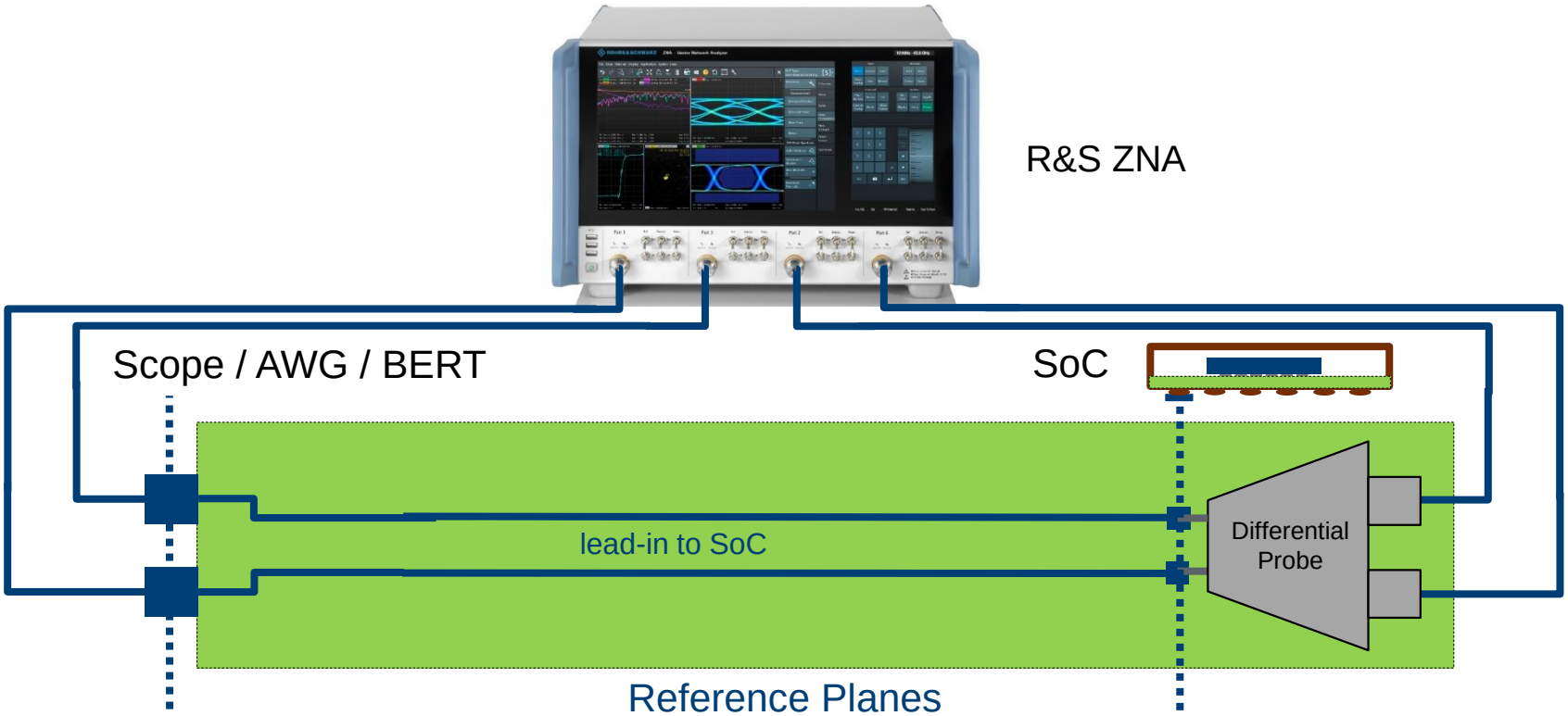


ACCESSING THE TRANSMISSION CHANNEL AND DE-EMBEDDING LEAD-INS AND LEAD-OUTS

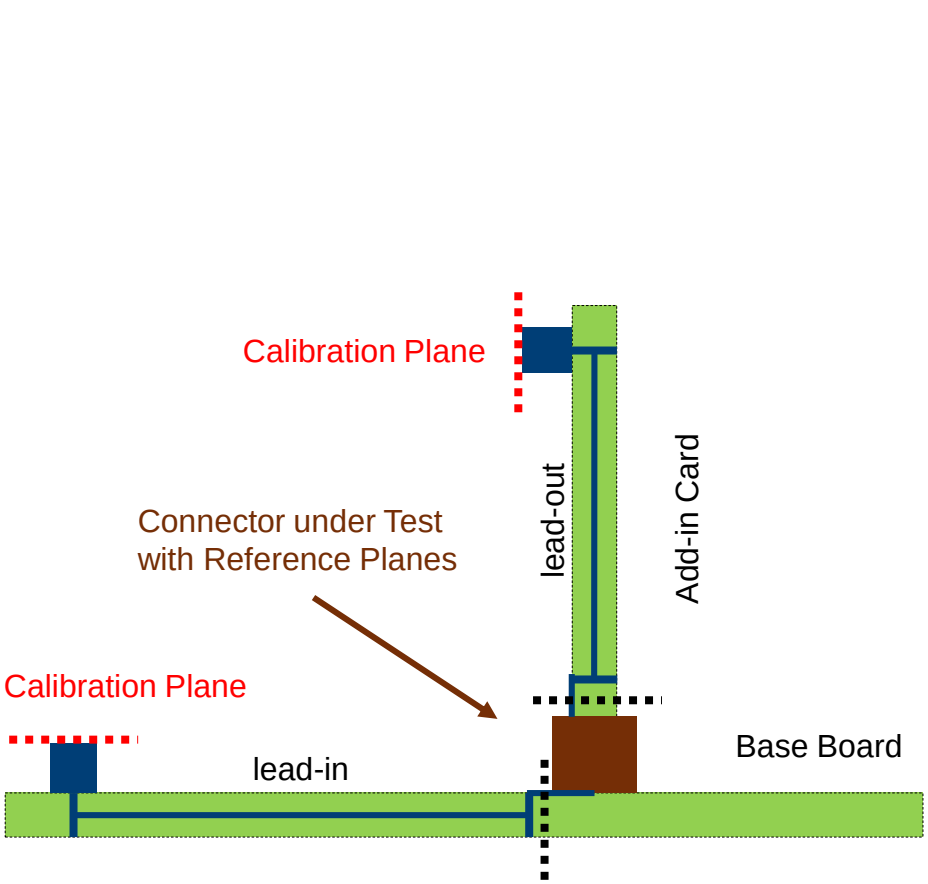
EXAMPLE #1: CHANNEL BETWEEN TWO SOCS

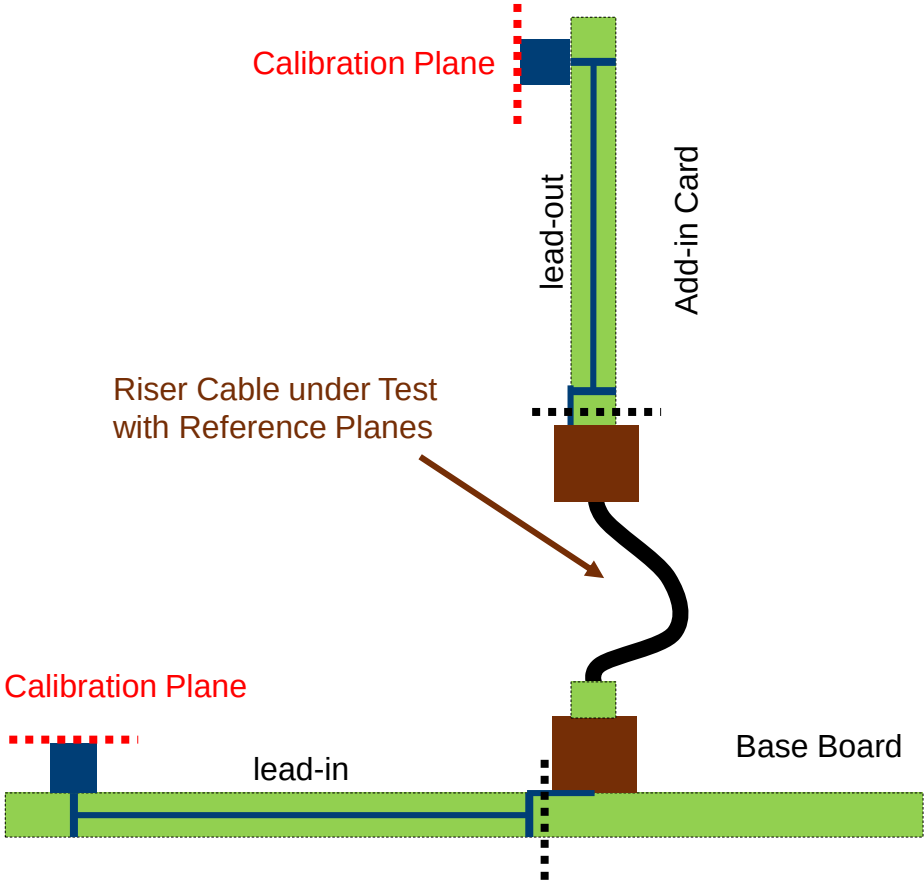


EXAMPLE #2: TEST BOARD W. LEAD-IN FOR SOC VALIDATION



EXAMPLE #3: PCIE CEM CONNECTOR / PCIE RISER CABLE





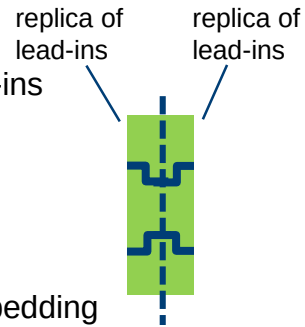
ACCURATE TEST FIXTURE MODELLING AND DE-EMBEDDING: GENERAL CONCEPT

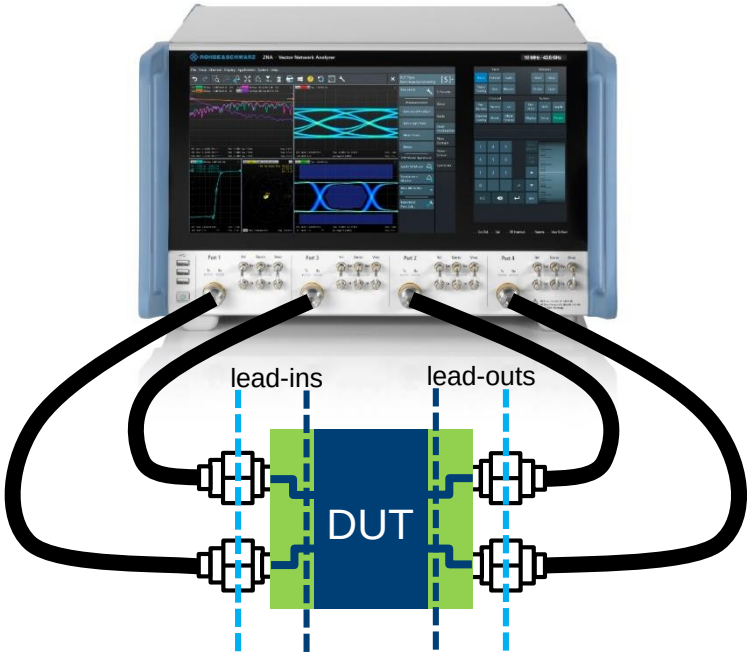
Challenge: DUT without coaxial connectors

- setup can only be calibrated up to the coaxial connectors of the test fixture
- test fixture (lead-ins / lead-outs) needs to be characterized, i.e. modelled
- test fixture models are used to de-embed the DUT from the total ‚Fixture – DUT – Fixture' structure
- reference planes are shifted to DUT

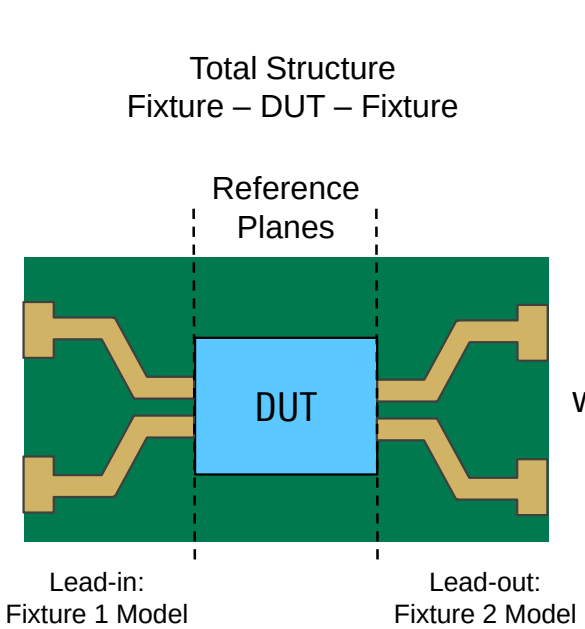
Traditional Solution:

- 2x-Thru de-embedding, modelling the lead-ins and lead-outs from a 2x-Thru replica
- limitation:
  - replica of lead-in ≠ lead-in
  - replica of lead-out ≠ lead-out
- new solution: impedance corrected de-embedding

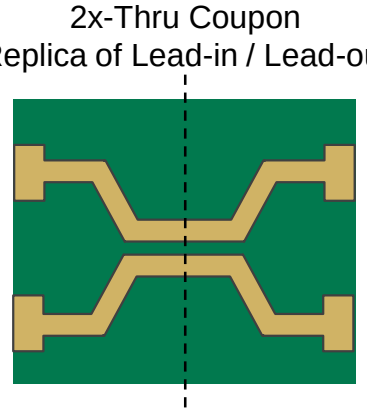




ACCURATE TEST FIXTURE MODELLING AND DE-EMBEDDING: HOW IT WORKS



with

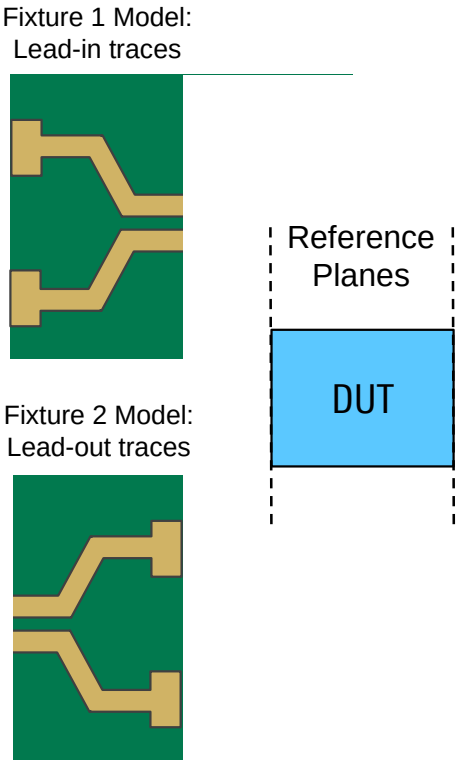


Traditional 2x-Thru de-embedding:
fixture models were only derived from 2x-Thru Coupon (replicas)

But:
replicas typically have different impedance profiles than actual lead-ins / lead-outs!

Therefore:
use modern de-embedding with impedance correction

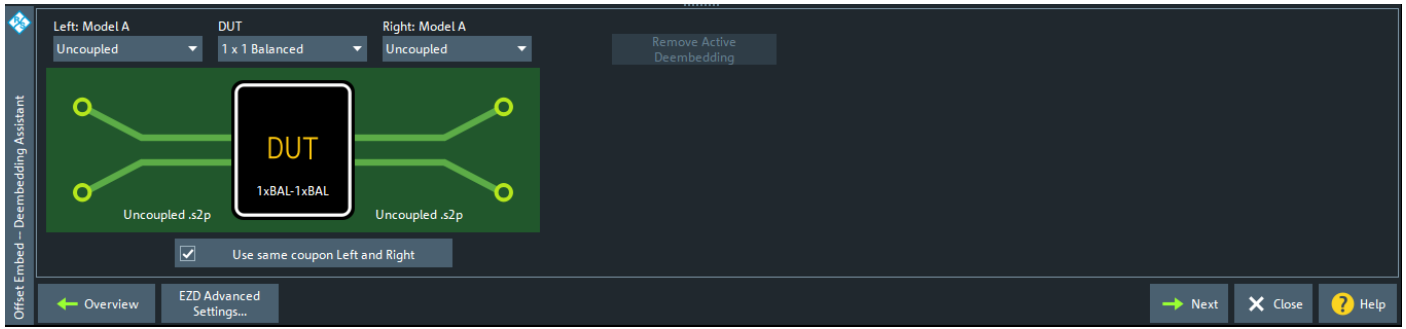
Tool



R&S DE-EMBEDDING ASSISTANT: ZNA, ZNB / ZNBT AND ZND WORKFLOW WITH IMPEDANCE CORRECTION

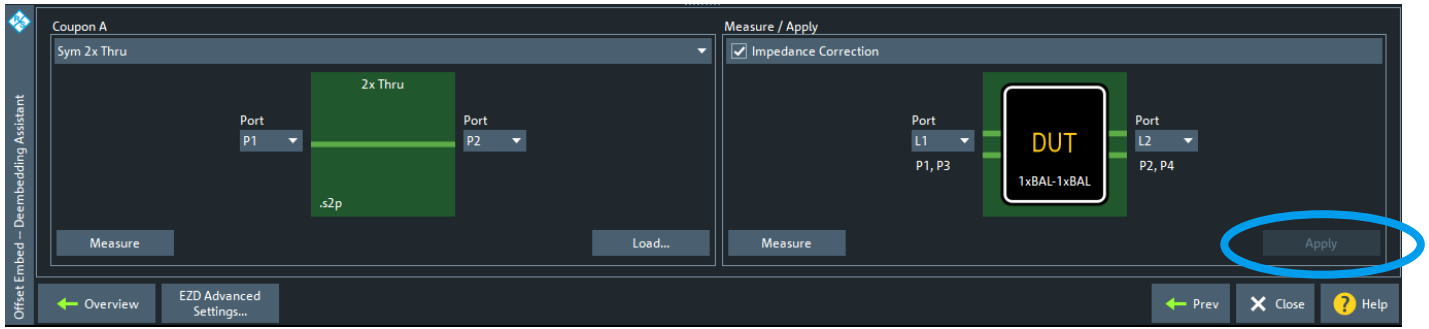
R&S De-embedding Assistant with Impedance Correction: Example ZNx-K220 / ISD

Step 1:
select topology
- DUT
- lead-in
- lead-out



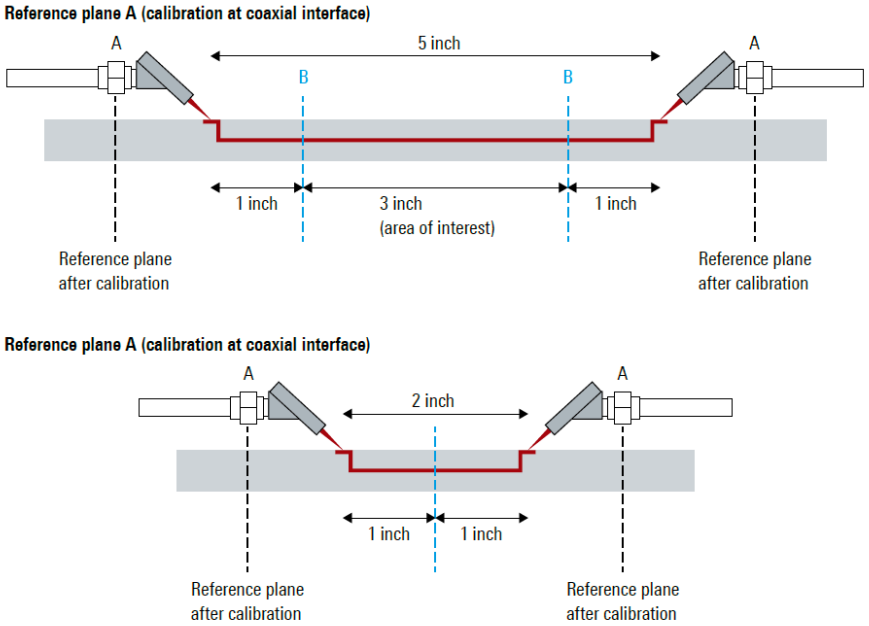
Step 2:
measurements
- coupon(s)
- total structure

Step 3:
apply



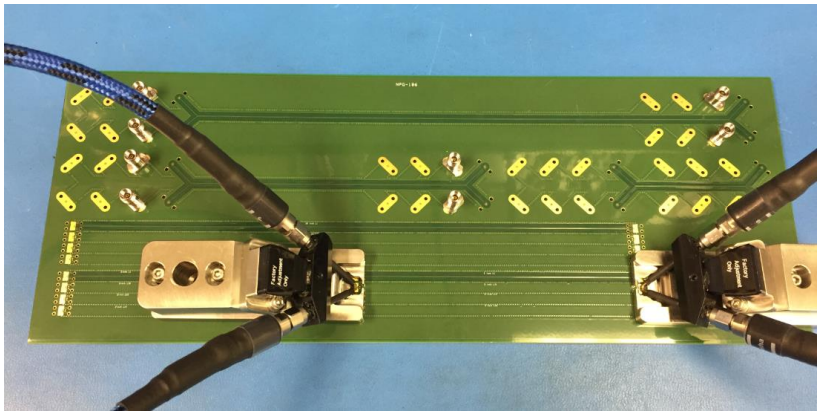
SPECIAL CASE: PCB VERIFICATION INSERTION LOSS / INCH WITH INTEL DELTA-L 4.0

Principle of Delta-L Measurement



Setup with Delta-L 4.0 Probes:

Example with PacketMicro Probes



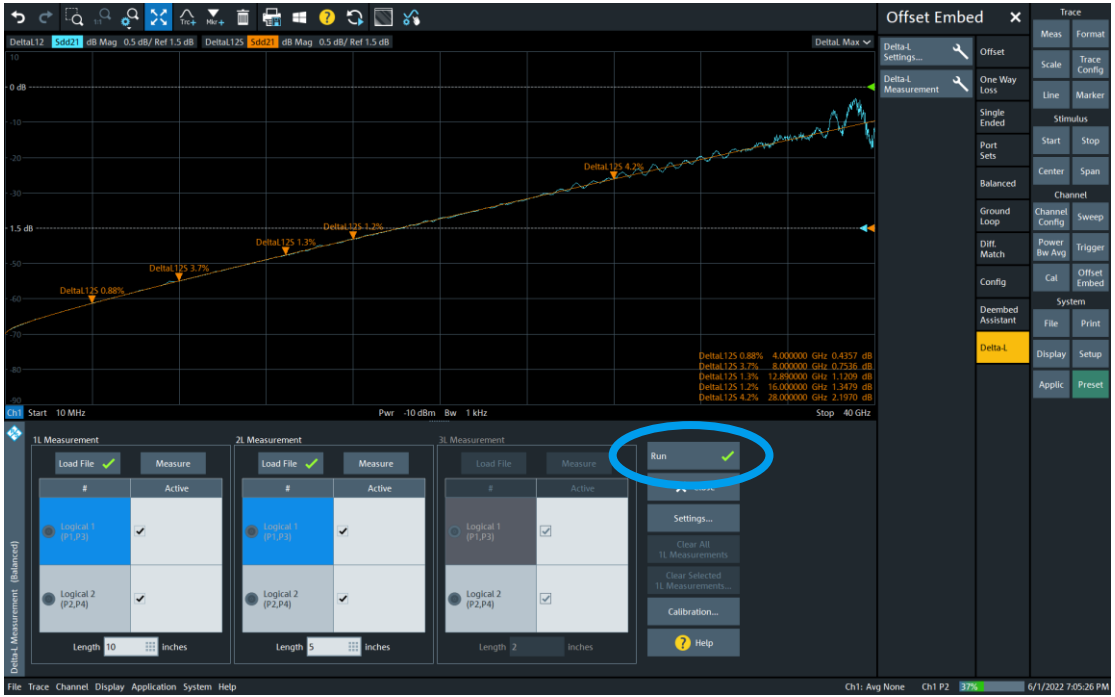
R&S IMPLEMENTATION IN ZNA, ZNB / ZNBT AND ZND DELTA-L 4.0 WORKFLOW

R&S Workflow Integration for Delta-L 4.0: Example for 2L Measurement

Step 1:
Structure 1, e.g. 10 inch

Step 2:
Structure 2, e.g. 5 inch

Step 3:
Run

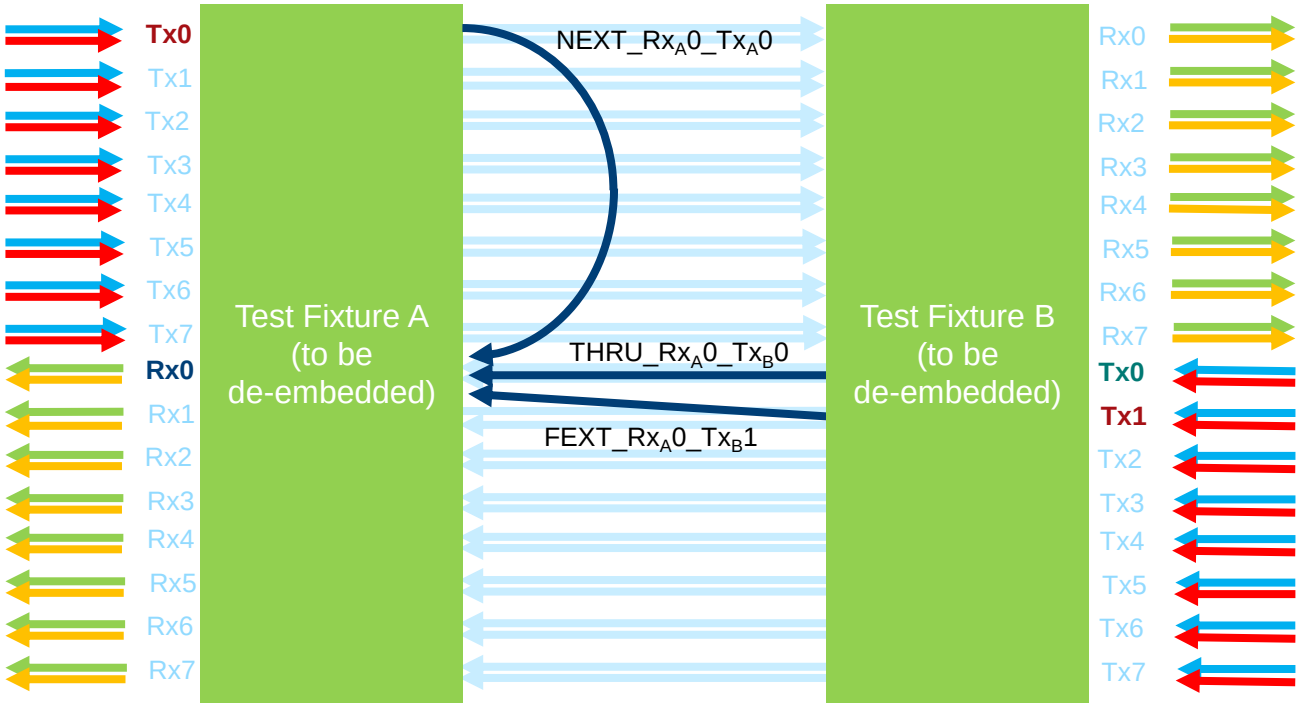


MEASUREMENTS ON PCIE 5.0 CABLE ASSEMBLIES

PCIE 5.0 CABLE ASSEMBLY: EXAMPLE FOR X8 CABLE PERFORMANCE REQUIREMENTS

Frequency Range:
- 10 MHz - 24 GHz

Performance Criteria:
- return loss
  method of waiver: iRL
- near-end crosstalk NEXT
  and power sum MDNEXT
  method of waiver: ccICN
- far-end crosstalk FEXT
  and power sum MDFEXT
  method of waiver: ccICN
- intra-pair skew: EIPS
- inter-pair skew (lane-to-lane)



TYPICAL PCIE 5.0 MEASUREMENTS

Frequency Domain:

- return loss, insertion loss
- crosstalk: NEXT, FEXT
- derived values:
  - iRL (integrated return loss)
  - ccICN (component contribution integrated crosstalk noise)
  - EIPS (effective intra-pair skew)

Time Domain:

- inter-pair skew
- impedance profile

R&S ZNA

R&S ZNB

R&S ZNrun

R&S ZNBT

R&S OSP320

THANK YOU