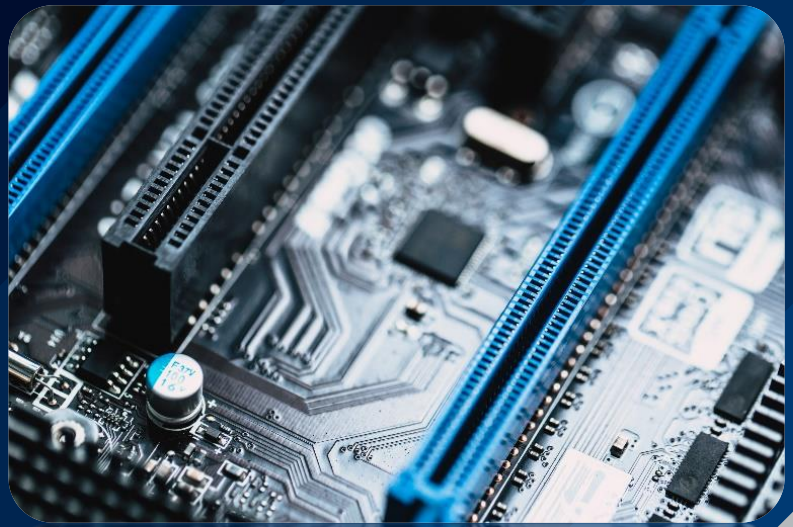
TEST SOLUTION FOR PCIE GEN5 RISER CABLE



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Business Development and Marketing Dept.

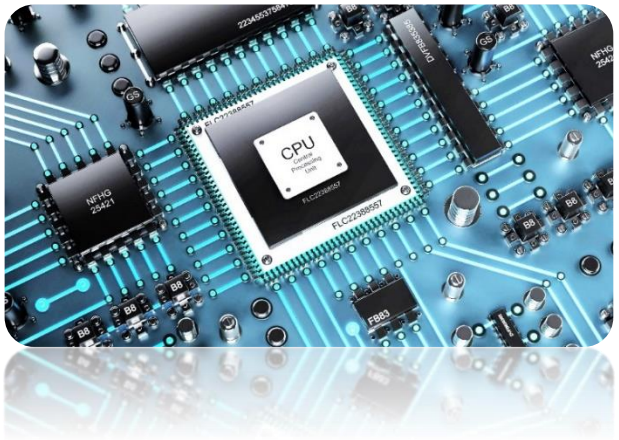
ROHDE&SCHWARZ
Make ideas real

samtec

ALLION AIoT EXPERT

AGENDA

- PCIe Interface Introduction and Overview
- PCIe Gen5 CEM/Riser Test Considerations and Test Items
- R&S Test Solution for PCIe Gen5 CEM and Riser Cable
- Demo: PCIe Gen5 Riser Cable Testing



PCI EXPRESS (PCIe) OVERVIEW

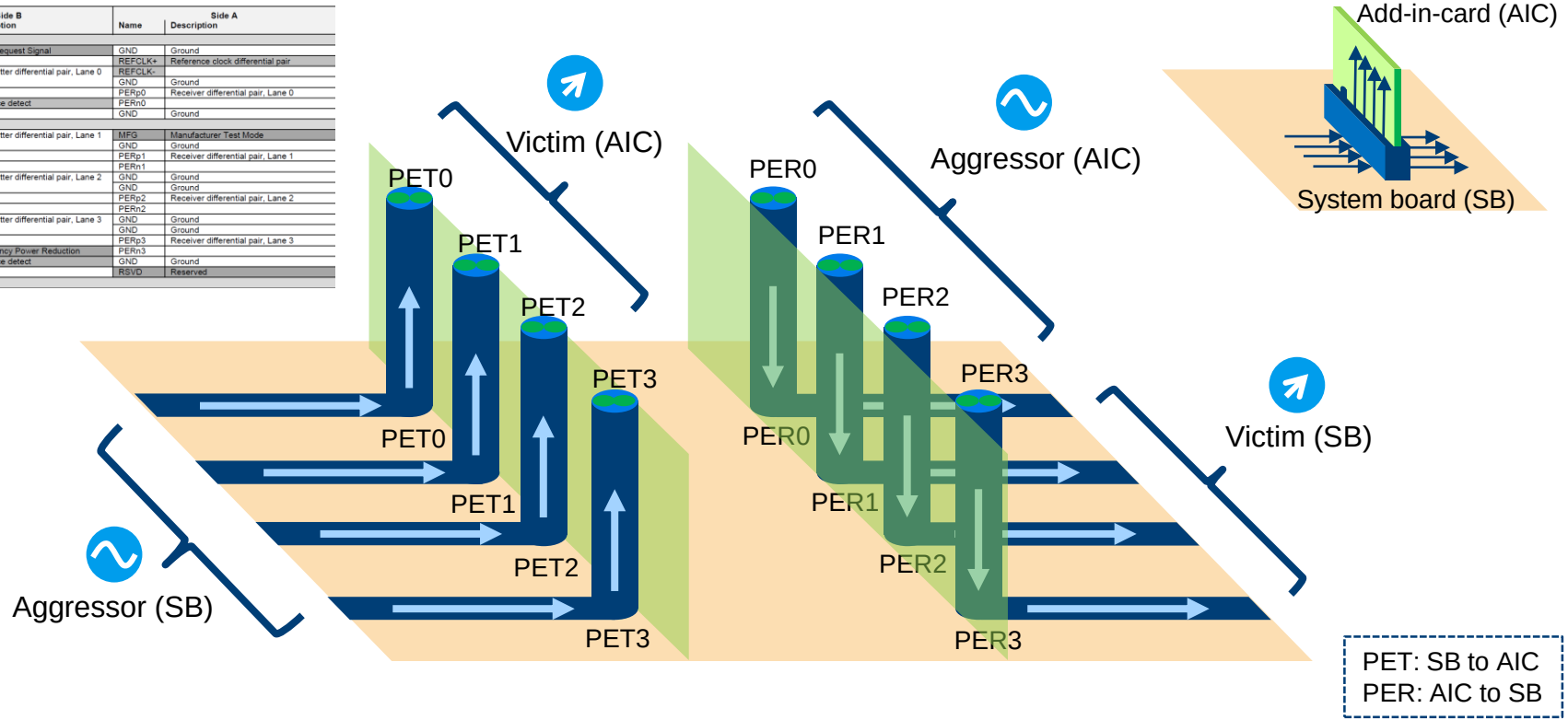
- Introduced in 2004
- Peripheral Component Interconnect Express is the de facto standard to connect high performance IO devices to the rest of the system. Eg. NICs, NVMe, graphics, TPUs
- Computer to Peripheral Communication
- Overseen by PCI-SIG
- Full-duplex bidirectional
- Backwards compatibility
- Connection Interface
  - CEM / Gen Z / MCIO
  - U.2 / M.2

Gen	Transfer Rate	Total x 16 BW	Coding	VNA required, GHz (for Interface)
1.0	2.5 GT/s	4 GB/s	8b/10b	-
2.0	5.0 GT/s	8 GB/s	8b/10b	-
3.0	8.0 GT/s	~ 15.8 GB/s	128b/130b	6.5 GHz
4.0	16.0 GT/s	~ 31.5 GB/s	128b/130b	12 GHz
5.0	32.0 GT/s	~ 63 GB/s	128b/130b	24 GHz
6.0	64.0 GT/s 32 GBd	~ 121 GB/s	242b/256b (PAM4)	~ 24 GHz (spec. in progress)
7.0	128.0 GT/s 64 GBd	~242 GB/s	242b/256b (PAM4)	~ 48 GHz (spec. in progress)

PCIE GEN5 CEM/RISER TEST CONSIDERATIONS

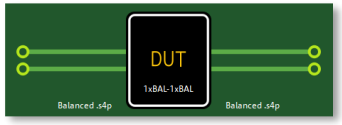
PCIE SIGNAL FLOW IN BASEBOARD AND ADD-IN-CARD

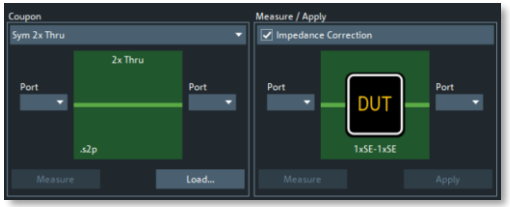
Pin #	Side B Name	Side B Description	Side A Name	Side A Description
Mechanical Key				
12	CLKREQ#	Clock Request Signal	GND	Ground
13	GND	Ground	REFCLK+	Reference clock differential pair
14	PETp0	Transmitter differential pair, Lane 0	REFCLK-	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Presence detect	PERn0	
18	GND	Ground	GND	Ground
End of the x1 Connector				
19	PETp1	Transmitter differential pair, Lane 1	MFG	Manufacturer Test Mode
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair, Lane 2	GND	Ground
24	PETn2		GND	Ground
25	GND	Ground	PERp2	Receiver differential pair, Lane 2
26	GND	Ground	PERn2	
27	PETp3	Transmitter differential pair, Lane 3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Receiver differential pair, Lane 3
30	PWRBRK#	Emergency Power Reduction	PERn3	
31	PRSNT2#	Presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
End of the x4 connector				

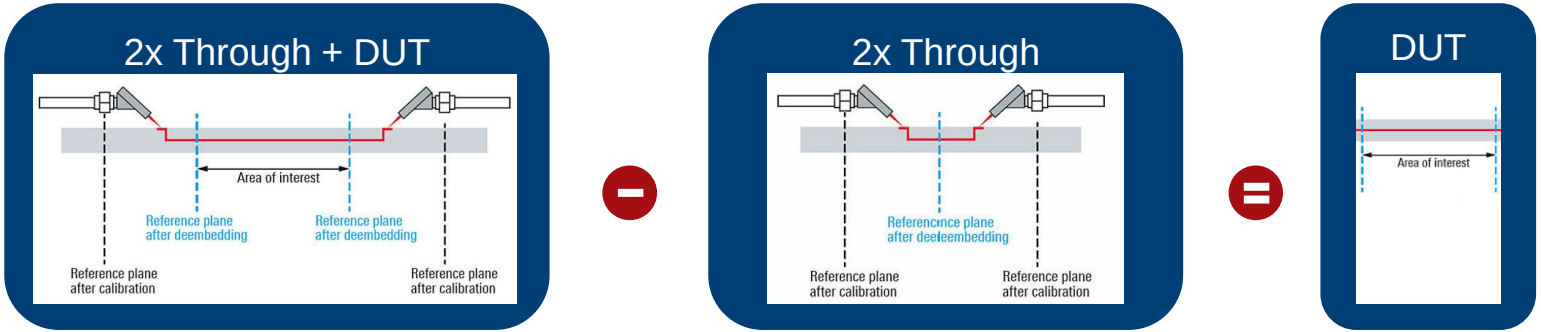


PCIE GEN5 CEM/RISER TEST CONSIDERATIONS

TWO-STEPS DE-EMBEDDING TECHNIQUES







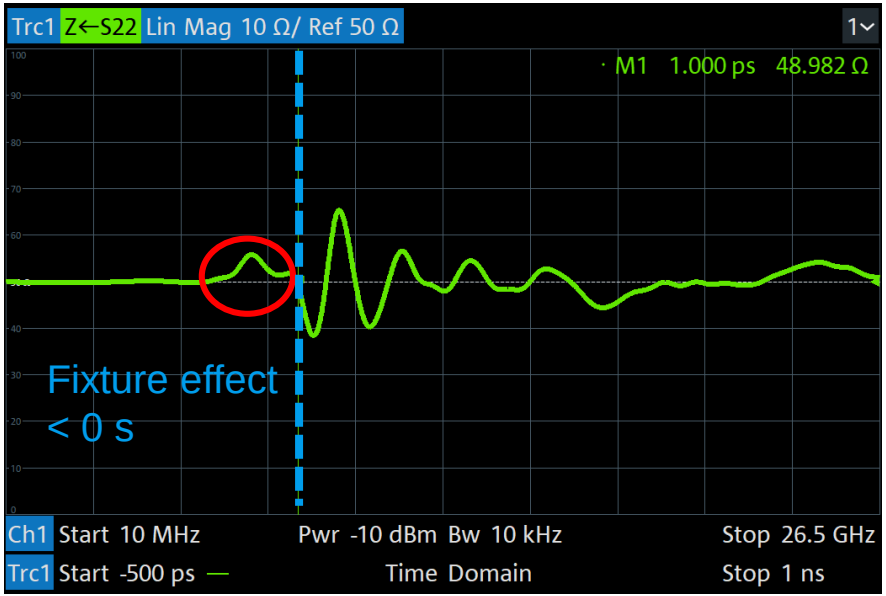
- Industry accepted SW algorithms
  - ISD: In-Situ De-embedding
  - SFD: Smart Fixture De-embedding
  - EZD: Eazy De-embedding

Test Coupon	ISD	SFD	EZD
2x Thru	√	√	√
1x Open	√	√	
1x Short	√	√	
1x Open + 1 x Short	√		

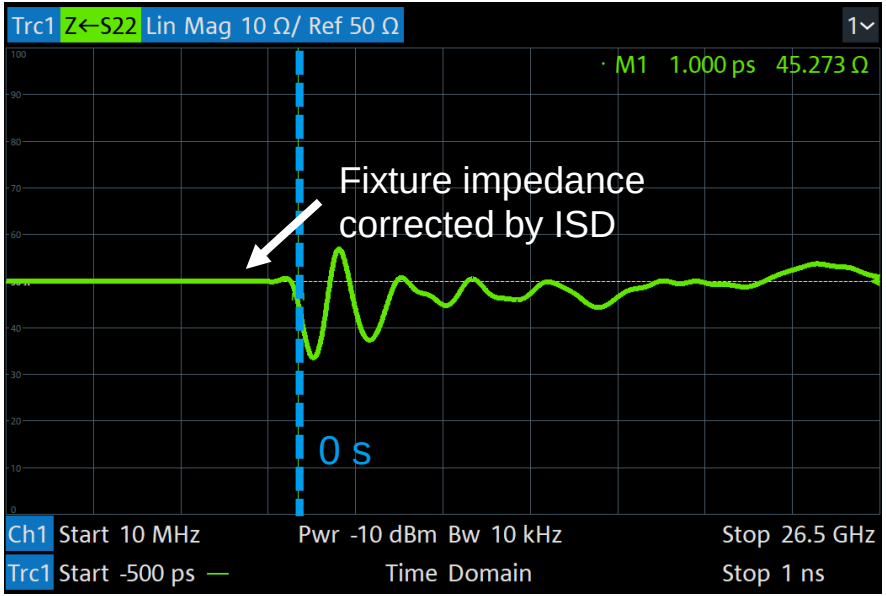
PCIE GEN5 CEM/RISER TEST CONSIDERATIONS

TRL VS. DE-EMBEDDING TECHNIQUES

TRL Cal Kit



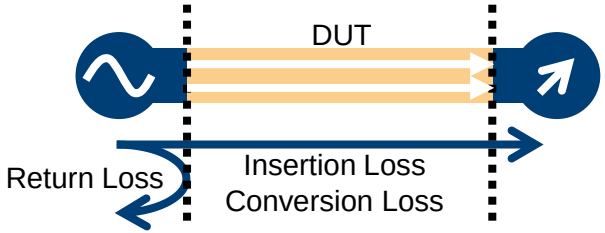
De-embed Algorithm



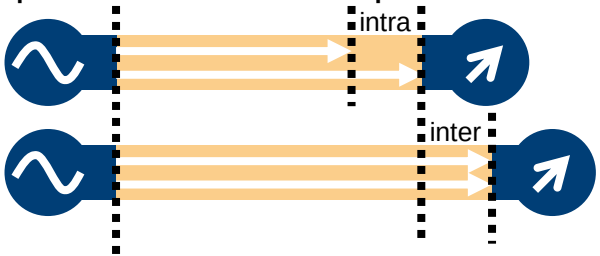
PCIE GEN5 CEM/RISER TEST ITEMS

BASIC TEST ITEMS

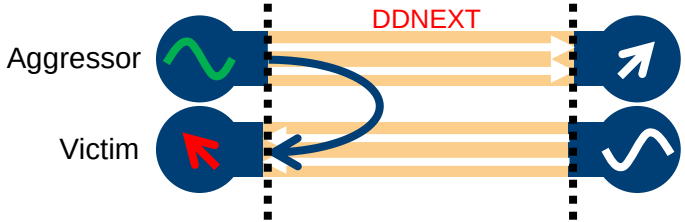
- Differential Insertion Loss (DDIL)
- Differential Return Loss (DDRL)
- Differential-to-Common Mode Conversion Loss



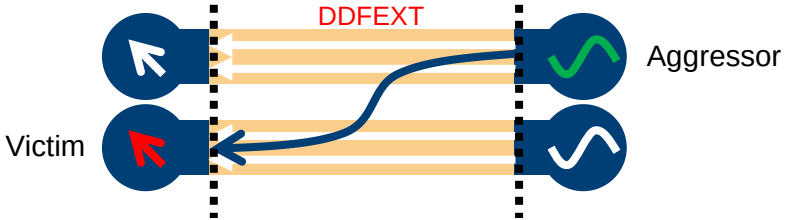
- Inter-pair Skew and Intra-pair Skew



- Differential Near End Crosstalk (DDNEXT)



- Differential Far End Crosstalk (DDFEXT)

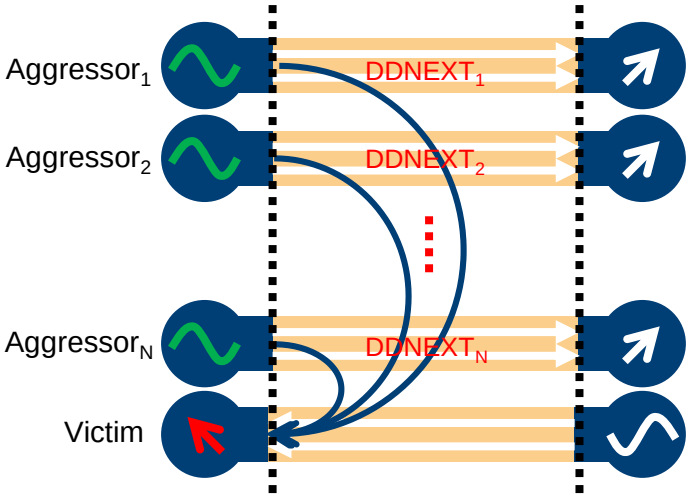


PCIE GEN5 CEM/RISER TEST ITEMS

ADVANCED TEST ITEMS

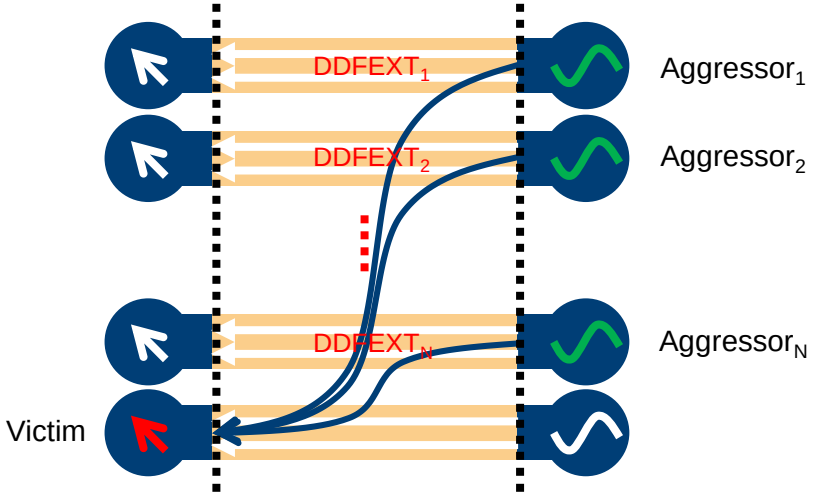
- Multiple Disturber Near End Crosstalk (MDNEXT)

Linear form: $MDNEXT(f) = \sum_{i=1}^{N} DDNEXT_i(f)$



- Multiple Disturber Far End Crosstalk (MDFEXT)

Linear form: $MDFEXT(f) = \sum_{i=1}^{N} DDFEXT_i(f)$

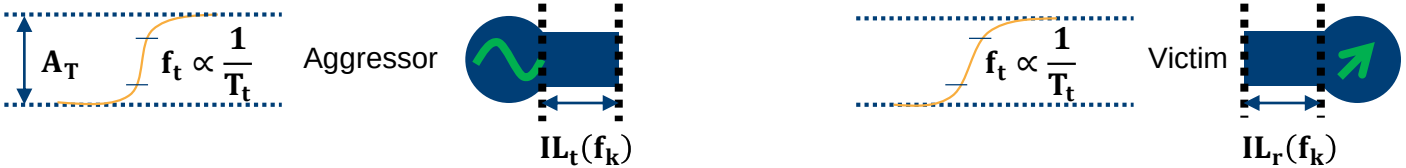


PCIE GEN5 CEM/RISER TEST ITEMS

ADVANCED TEST ITEMS

- Component Contribute Integrated Crosstalk Noise ($ccICN_{NEXT}$ and $ccICN_{FEXT}$)
- Effective voltage of power sum of MDNEXT or MDFEXT
- Weighting function:

$$W_n(f_k) = \left(\frac{A_T}{f_b}\right)^2 \mathrm{sinc}^2\left(\frac{f_k}{f_b}\right) IL_t(f_k) IL_r(f_k) \left[\frac{1}{1+\left(\frac{f_k}{f_t}\right)^4}\right]\left[\frac{1}{1+\left(\frac{f_k}{f_r}\right)^4}\right]$$



- Effective voltage (V_{rms}):

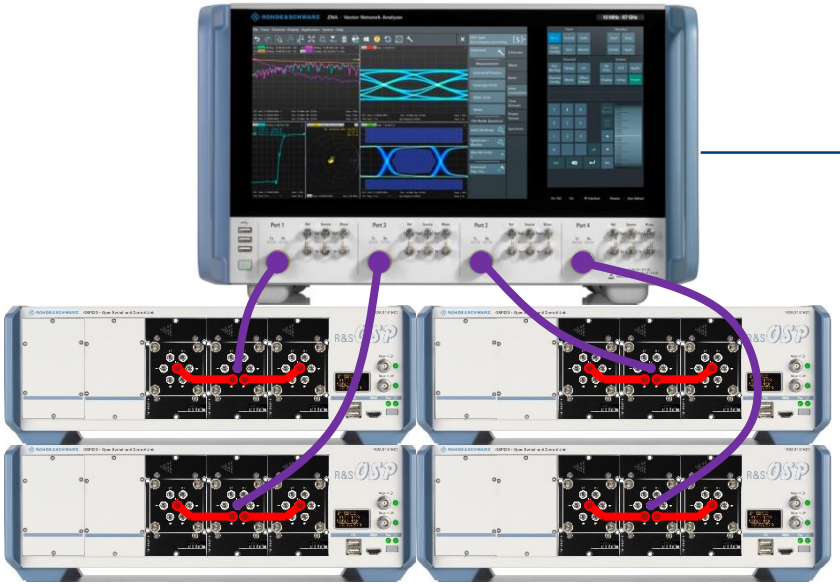
$$ccICN_{NEXT}(f_k) = \sqrt{\frac{1}{2}\Delta f \sum_{k=1}^{N} W_n(f_k) MDNEXT(f_k)}$$

$$ccICN_{FEXT}(f_k) = \sqrt{\frac{1}{2}\Delta f \sum_{k=1}^{N} W_n(f_k) MDFEXT(f_k)}$$

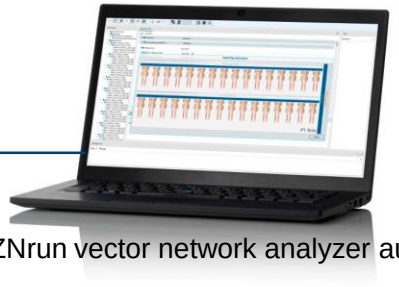
TEST SOLUTION FOR PCIE CEM/RISER CABLE TESTING

64-PORT SETUP

R&S®ZNA/ R&S®ZNB vector network analyzer



R&S®OSP Open Switch and Control Platform



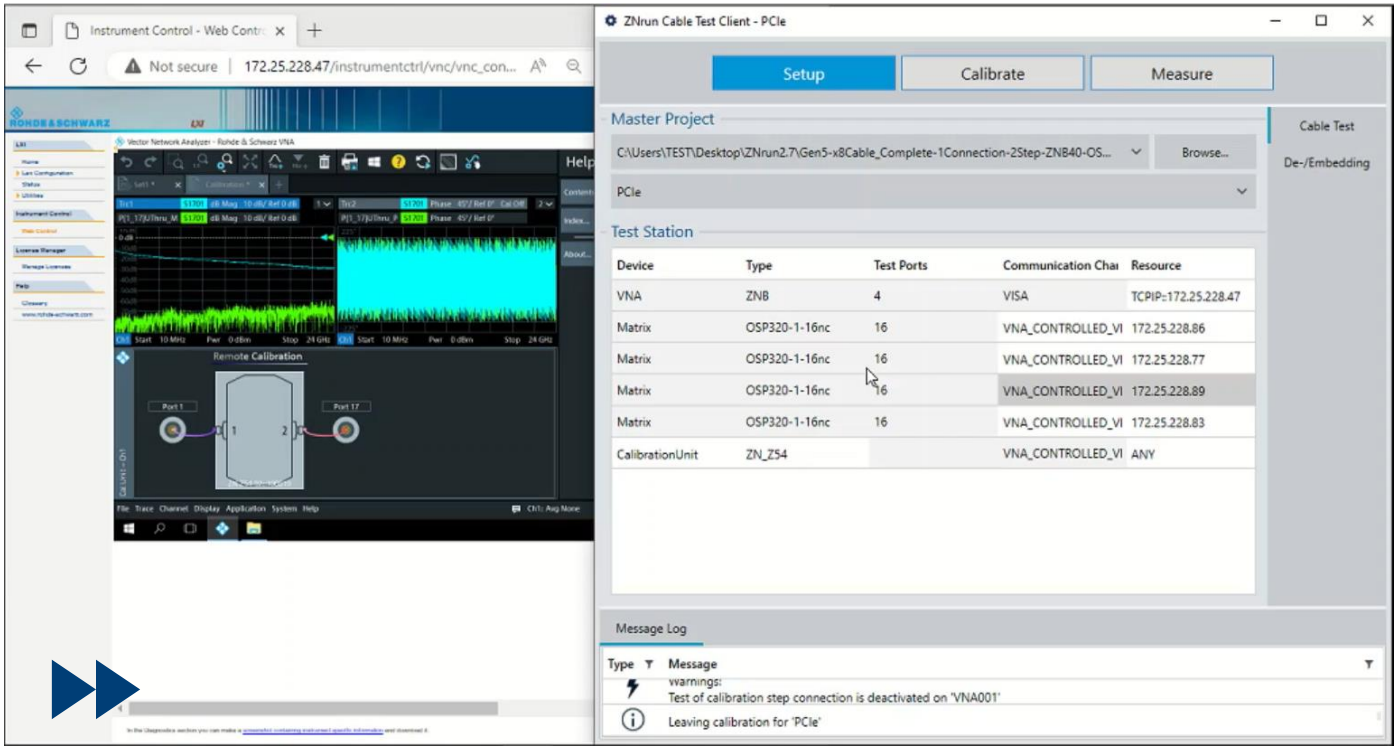
R&S®ZNrun vector network analyzer automation suite

- Multiport extendable setup: 8-/12-/24-/32-/48-/64-port
- ZNrun automation suite handles
  - Switching topology
  - Test items
  - Calibration/measurement optimization
  - Compliance/pre-compliance reporting

TEST SOLUTION FOR PCIE CEM/RISER CABLE TESTING

64-PORT CALIBRATION

connections: 63 vs. 768



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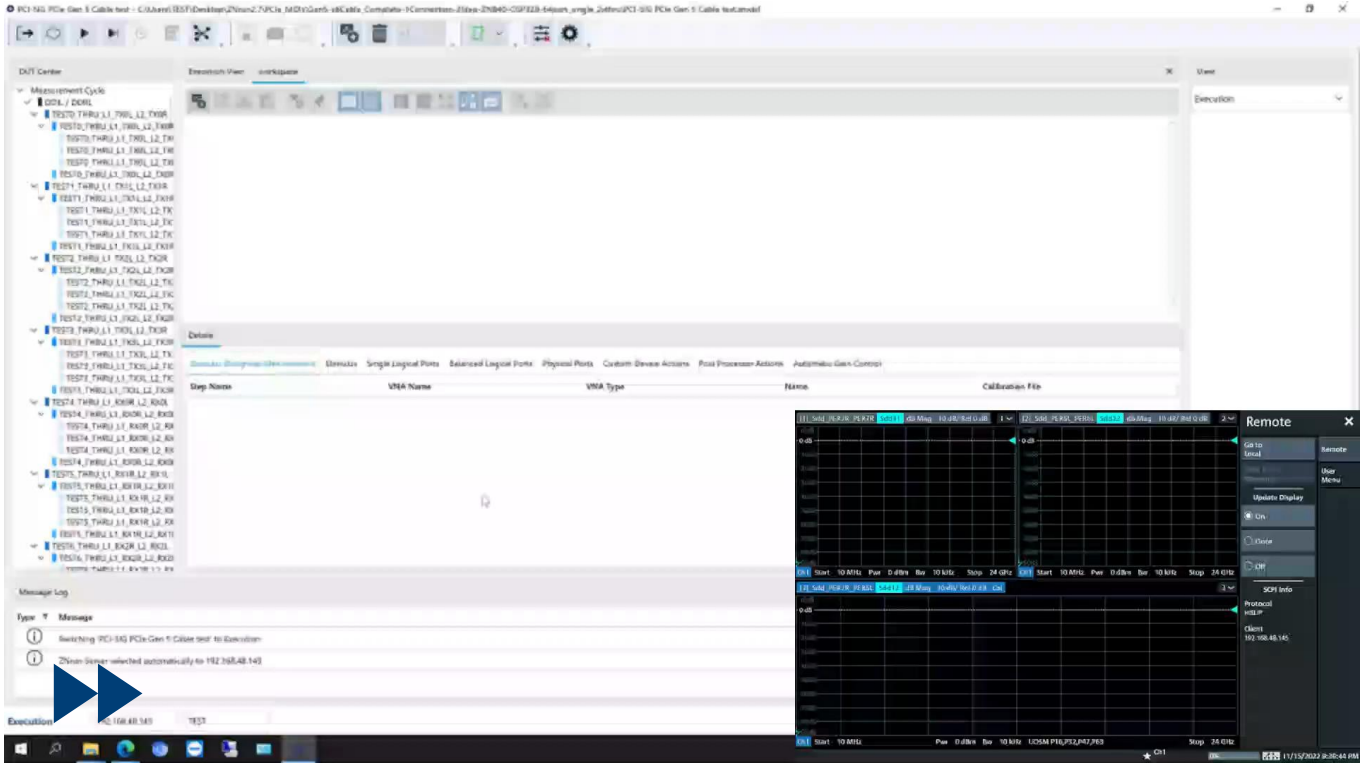
TEST SOLUTION FOR PCIE CEM/RISER CABLE TESTING

64-PORT PCIE GEN5 RISER CABLE MEASUREMENT



DDIL/DDRL

↓

DDNEXT_L

↓

DDNEXT_R

↓

DDFEXT_L

↓

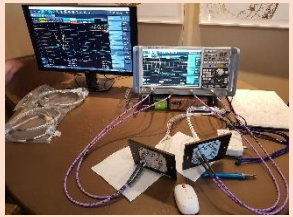
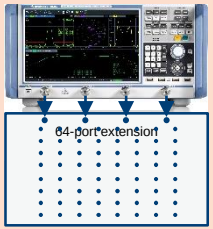
DDFEXT_R

↓

Done!

TEST SOLUTION FOR PCIE CEM/RISER CABLE TESTING

ESTIMATION OF TOTAL MEASUREMENT TIME

Items	Conventional 4-port VNA	Conventional – 64-port	R&S solution – 64-port
Picture			
Calibration time 	3 connections (4-port) 4 min	256x 3 connections (4-port) 1024 min	63 connections 60 min
Reconnection effort	256x re-connections 512 min per cable	No reconnection (depend on fixture)	No reconnection (depend on fixture)
Measurement time	15 min per cable	15 min per cable	15 min per cable
Apply de-embed	Manual	Automated	Automated
Total measurement time (1 cable)	531 min = 8h 51 min	1039 min = 17h 19 min	75 min = 1h 15 min
Total measurement time (10 cable)	5274 min = 3 days 15h 54 min 11 working days (8 hour/day)	1174 min = 19h 34 min 2.5 working days (8 hour/day)	210 min = 3h 30 min About half day

R&S®ZNA/ R&S®ZNB vector network analyzer

R&S®OSP Open Switch and Control Platform

R&S®ZNrun vector network analyzer automation suite

PCIE RISER CABLE TESTING DEMONSTRATION