

Webinar

# ADVANCED EYE ANALYSIS GET TO YOUR RESULTS FASTER

Guido Schulze, Product Manager Oscilloscopes  
Alessandro Cappelletti, Application Engineer Oscilloscopes

**ROHDE & SCHWARZ**

Make ideas real



# OUTLINE

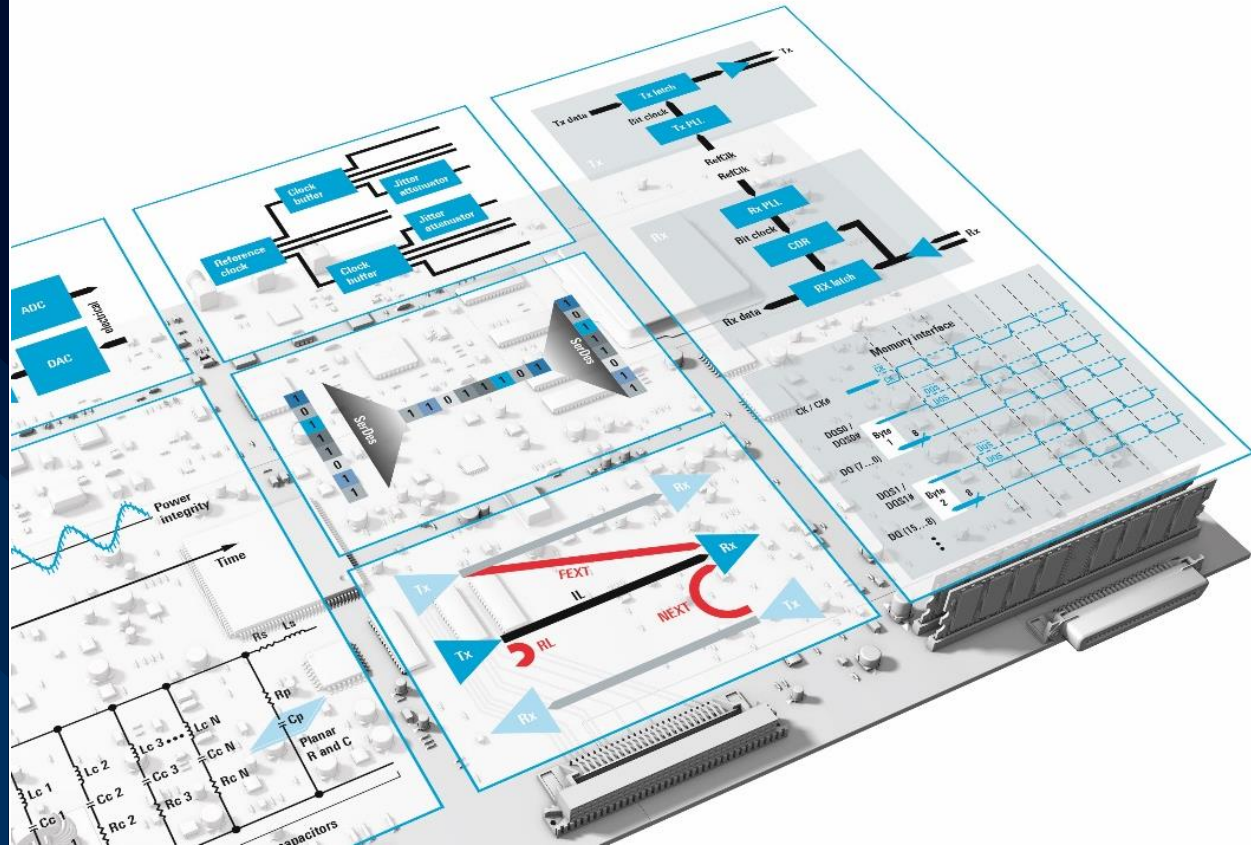
- ▶ What can go wrong on Highspeed Interfaces
- ▶ Eye Diagram Basics
- ▶ Traditional Eye Analysis Approaches
- ▶ New HW-CDR Approach
- ▶ From Quick “AHA” to the Details
- ▶ Live Demonstration
- ▶ Summary



# HIGHSPEED DIGITAL INTERFACES

- ▶ Signal integrity challenges due to increasing data rates
- ▶ Interference issues due to increasing level of integration

**Signal Integrity analysis:  
T&M needs to collect  
statistical data fast.**

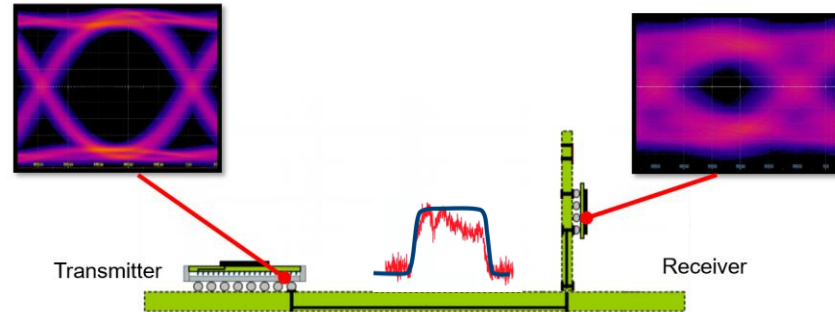


# HIGH SPEED DIGITAL INTERFACES

## WHAT COULD POSSIBLY GO WRONG?

### Common signal integrity problems:

- ▶ Channel-related effects
  - Signal loss/attenuation
  - Reflections due to impedance mismatches
  - Ringing (overshoot/undershoot)
  - Crosstalk
- ▶ Transmitter effects
  - Rise/fall imbalance
  - Timing jitter
- ▶ External sources (can be intermittent)
  - EMI within or from outside the components in the system
  - Noise from power and distribution networks
  - Interferer from other functional cores

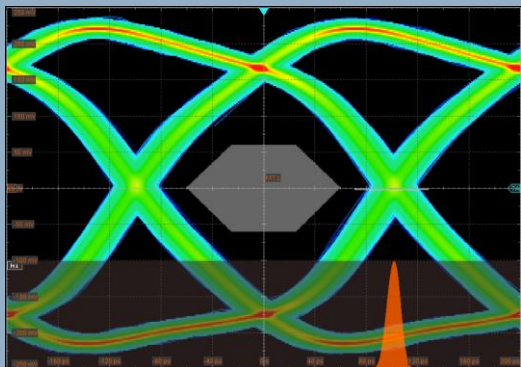


# HIGH SPEED DIGITAL INTERFACES

## Dedicated Tests for Verification & Debugging

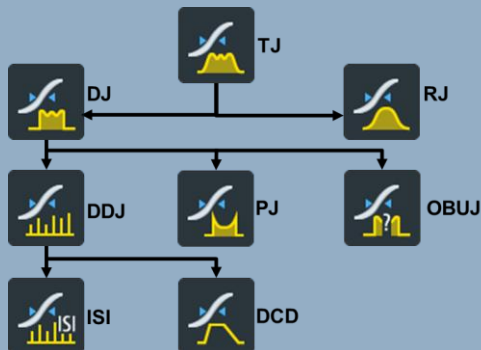
### Eye Diagram

- Fast update rate for statistical confidence
- Clock-Data-Recovery (CDR)
- Mask tests, Histogram



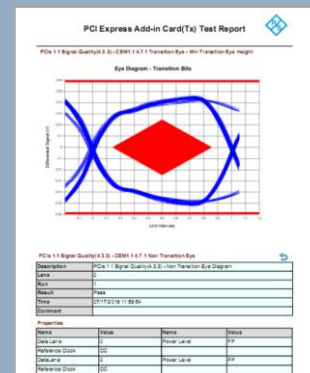
### Jitter & Noise Analysis

- Break-down of jitter and noise into individual components for characterization & debugging



### Automated Compliance Tests

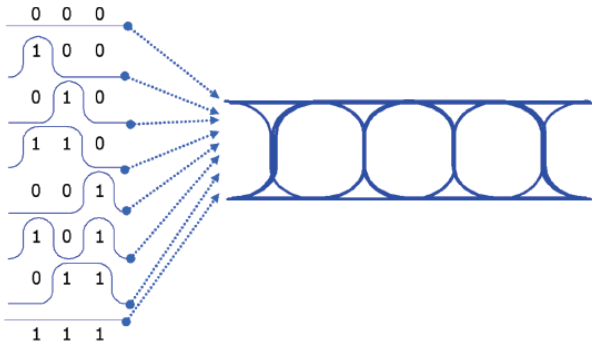
- Verify compliance of the physical layer to interface standards and report results



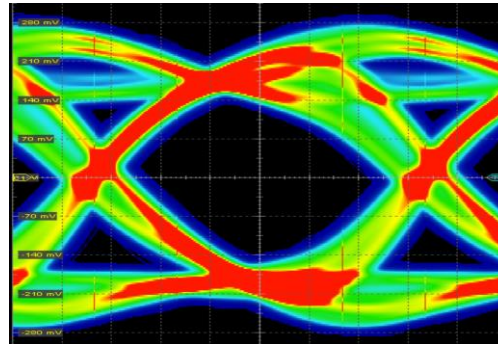
# EYE DIAGRAM BASICS

# EYE DIAGRAM INTRODUCTION

- ▶ Graphical tool for the evaluation of the quality and integrity of data signals
- ▶ Superposition of multiple signal waveform segments aligned to well-defined reference time instants
  - Waveform segments commonly correspond to a data symbol
  - Reference clock provides timing information for alignment (e.g. symbol start instant)



Superposition of bit sequences form the eye diagram

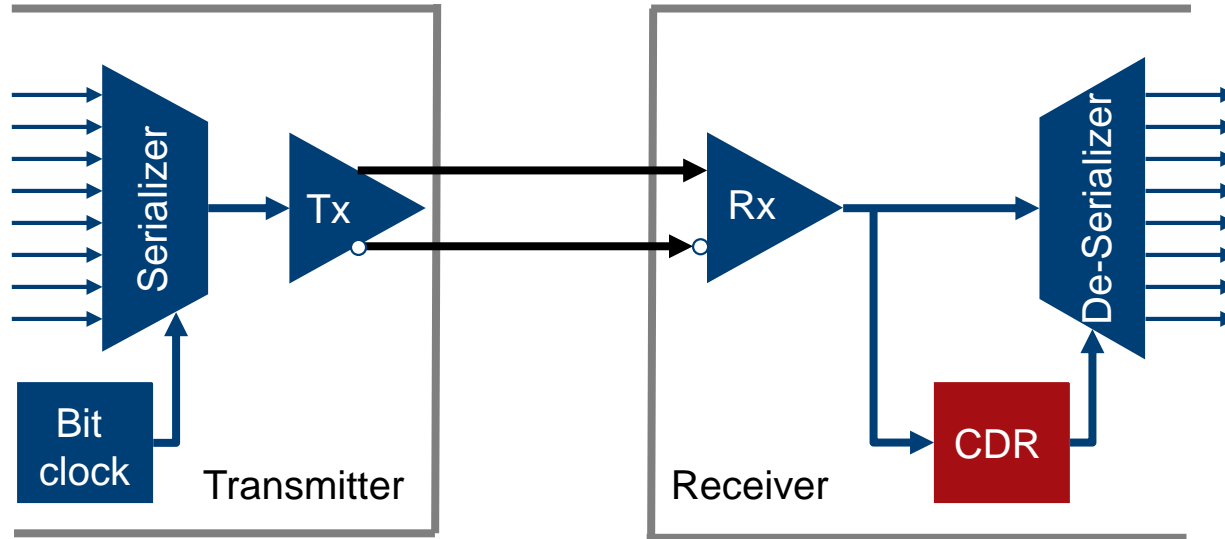


Eye diagram with color-coded frequency

# REFERENCE CLOCK GENERATION FOR EYE DIAGRAMS

## CLOCK-DATA-RECOVERY

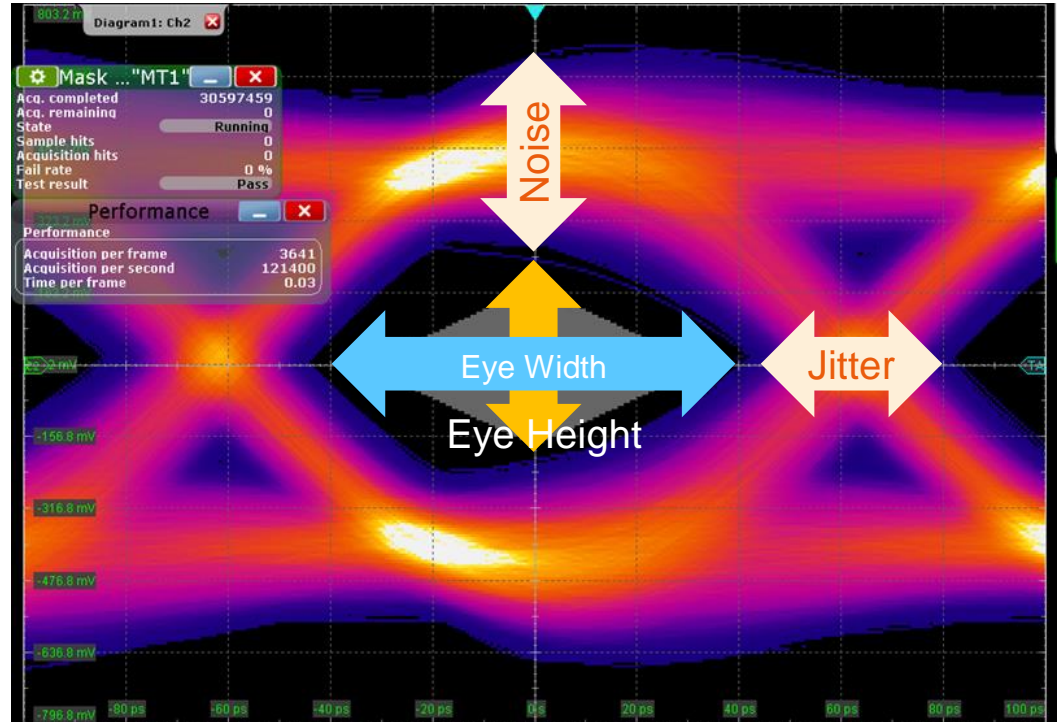
- ▶ Timing reference can be from a reference clock (parallel clock signal) or from the data signal itself (embedded clock signal)
- ▶ Clock data recovery is typically uses a Phase Locked Loop (PLL) or Delay Locked Loop (DLL)





# INFORMATION CONTAINED IN AN EYE DIAGRAM

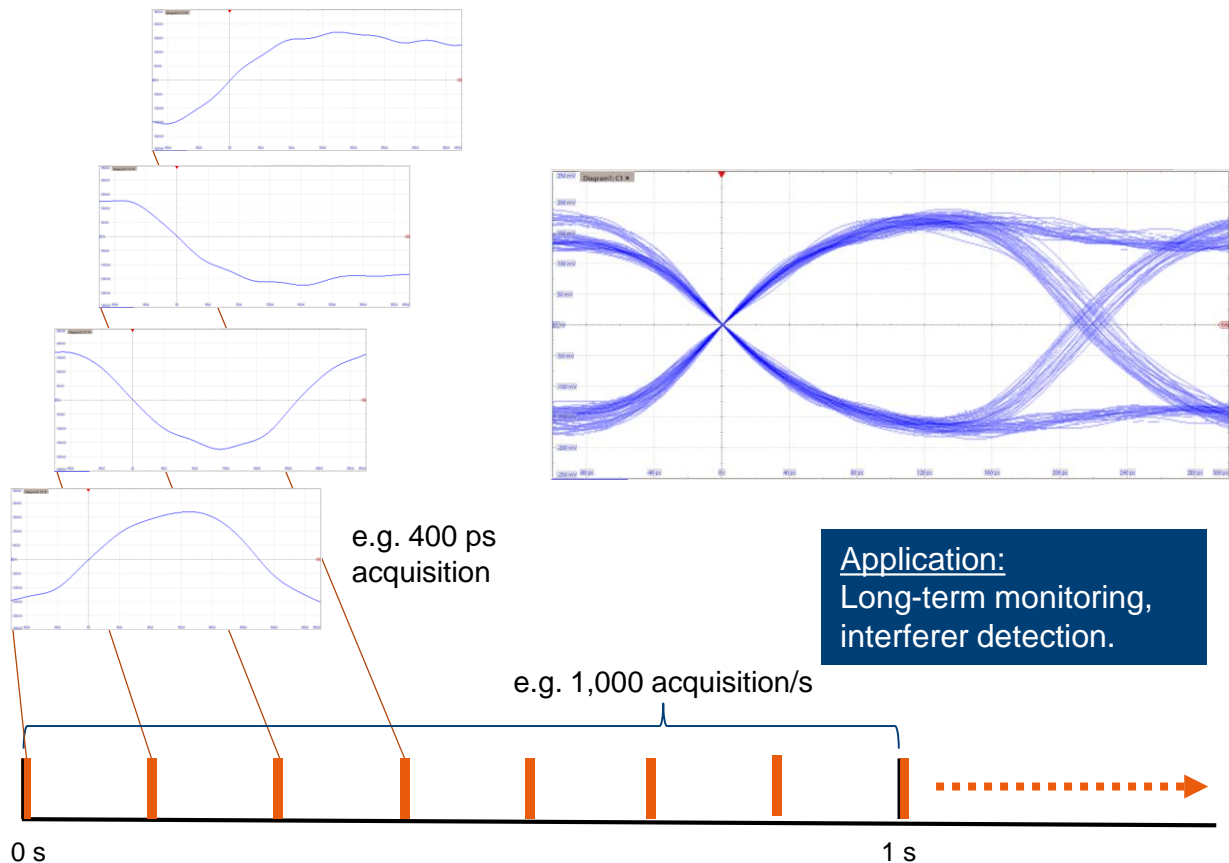
- ▶ Timing jitter: peak to peak, standard deviation
- ▶ Noise: peak to peak, standard deviation
- ▶ Eye width: the minimum time interval over which no signal transition will occur
- ▶ Eye height: the minimum amplitude over which the signal level occur
- ▶ Eye parameters are based on statistics and require large sample size for repeatable measurements



# TRADITIONAL EYE DIAGRAM APPROACHES

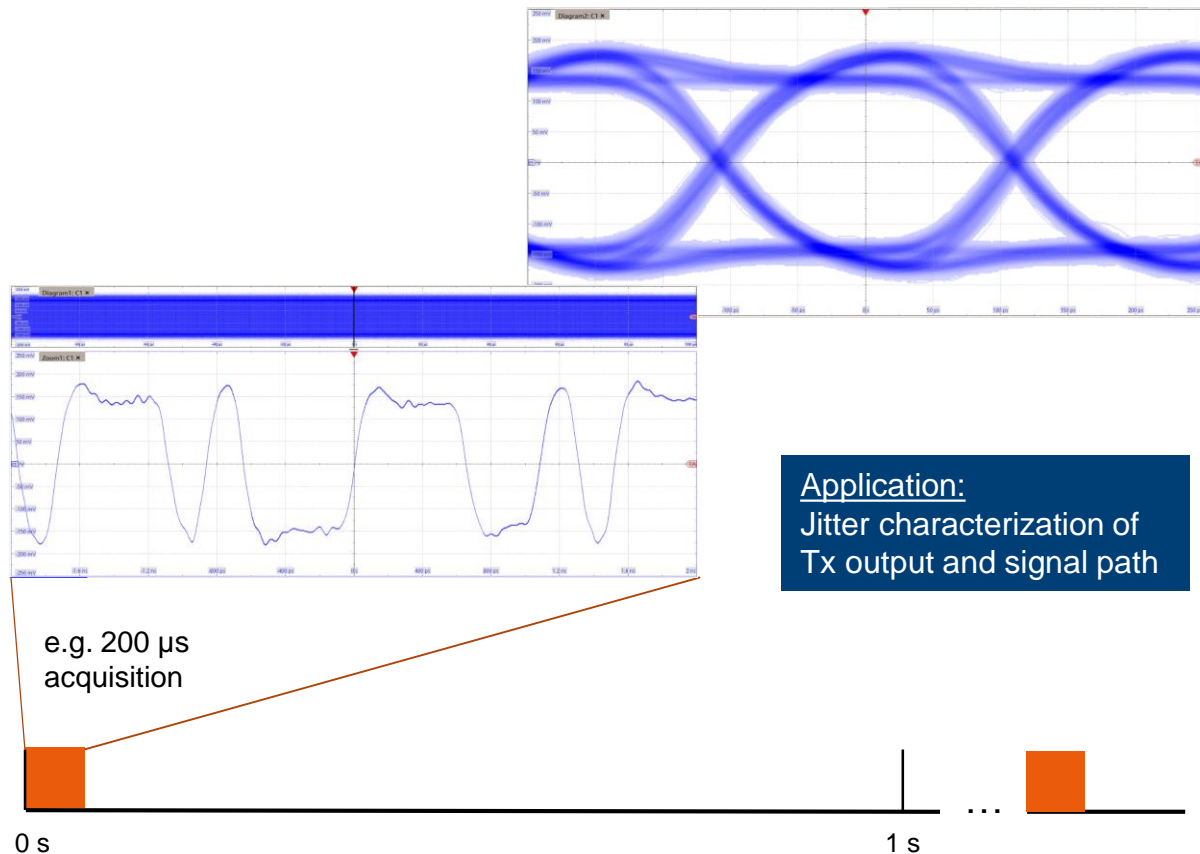
# “LIVE EYE”: CONTINUED ACQUISITION

- ▶ Continued acquisition of waveforms with short acquisition time
  - Trigger: “Edge”, rise/fall
  - Acquisition time:  $\sim 2$  UI
  - Persistent display mode to form a Data Eye
- ▶ Application:
  - Long-term monitoring, interferer detection

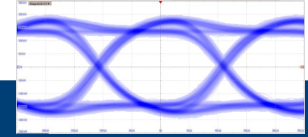
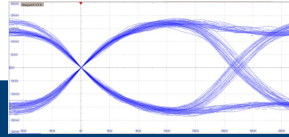


# BIT SEQUENCE: SINGLE ACQUISITION

- ▶ Acquisition of waveform with long acquisition time
  - Trigger: “Edge”, rise
  - Acquisition time: ~1M UI
  - SW-CDR to form a Data Eye
- ▶ Application:
  - Jitter/Noise characteristic of device & channel



# COMPARISON OF THE 2 APPROACHES

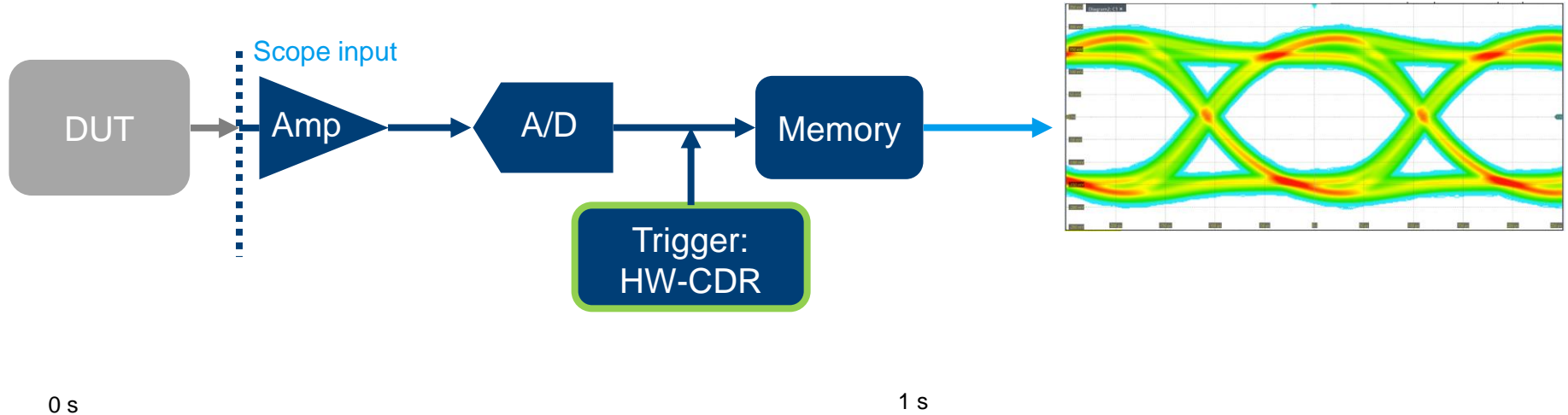


	<b>“Live Eye”</b>	<b>Bit sequence</b>
Application	<ul style="list-style-type: none"> <li>- long-term monitoring</li> <li>- detection of interferer</li> </ul>	<ul style="list-style-type: none"> <li>- characterization of transmitter and signal path</li> </ul>
Pro's	<ul style="list-style-type: none"> <li>- very easy setup for first glance</li> </ul>	<ul style="list-style-type: none"> <li>- CDR to analyze signal based on embedded clock</li> <li>- conform to standards test definition</li> </ul>
Con's	<ul style="list-style-type: none"> <li>- “edge“ trigger not suitable for jitter analysis</li> <li>- cannot capture non-transitional bits</li> </ul>	<ul style="list-style-type: none"> <li>- SW-CDR setup is more complex than “edge” trigger</li> <li>- new CDR locking for every acquisition “wastes” acquisition memory</li> <li>- long processing</li> </ul>

**R&S APPROACH – CDR TRIGGER IN HW**

# HW-BASED CLOCK-DATA-RECOVERY TRIGGER

- ▶ Eye Analysis based on Hardware implemented Clock-Data-Recovery (CDR)
  - CDR is part of the Trigger circuitry
  - CDR locks once and runs continuously
  - CDR is applicable for both Eye approaches: Bit sequence and Individual bits („Live Eye“)



# DETAILS OF CDR TRIGGER

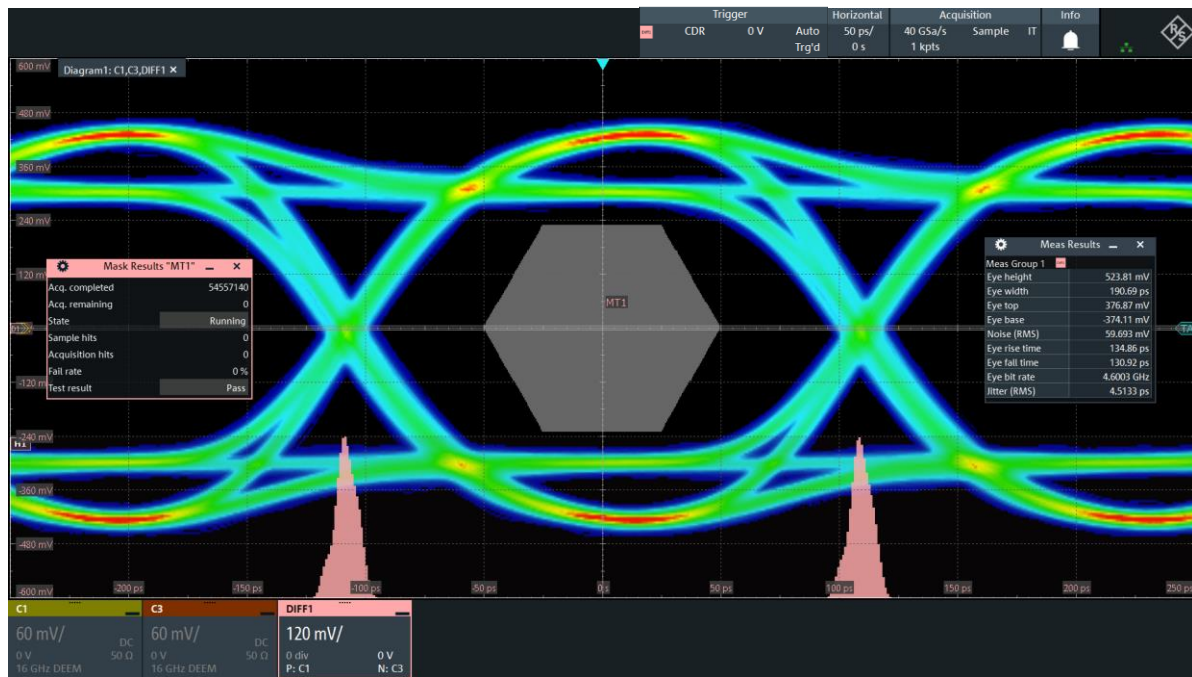
- ▶ Source:
  - any analog channels
- ▶ Combinable with:
  - differential signal math and real-time deembedding
- ▶ Nominal bit rate:
  - 21 kbps to 16 Gbps
- ▶ Configurable BW:
  - 1/500 to 1/3000 of nominal bit rate
- ▶ CDR timing can be saved as math waveform

The image displays two screenshots from a software interface. The top screenshot shows the 'Trigger' configuration window. On the left is a vertical menu with options: CDR, Edge, Glitch, Width, Runt, Window, Timeout, Interval, Slew rate, Setup & Hold, State, Pattern, Serial pattern, TV, and CDR (highlighted in blue). The main area is divided into sections: 'Trigger on' (Single event), 'Mode / Holdoff' (Type: CDR), 'Conditioning' (Source: C1 Channel 1), 'Action' (Data level: 0 V), and 'Qualify' (Nominal bit rate: 16 Gbps). A 'Hardware CDR' dropdown is visible at the bottom. A blue arrow points from the 'CDR' menu item to the 'Trigger' window. The bottom screenshot shows the 'Hardware CDR' configuration window. It includes fields for 'Source' (C1 Channel 1), 'Serial standard' (USB 3.2 Gen 2), 'Data level' (0 V), and 'Sampling time' (600 mUI). Below these are 'Bit rate estimation' settings: 'Nominal bit rate' (10 Gbps) and 'Estimate bit rate' button. 'Algorithm settings' include 'Bandwidth' (14.9925 MHz) and 'Rel. bandwidth' (667). A 'Back' button is at the bottom. To the right of the Hardware CDR window is a vertical list of signal standards: Custom, USB2.0, USB 3.2 Gen 1, USB 3.2 Gen 2 (highlighted in blue), Displayport 1.1, Displayport 1.2, Fibre Channel 1x, Fibre Channel 2x, Fibre Channel 4x, Fibre Channel 8x, HDMI 1.2, HDMI 1.4, HDMI 2.0, PCIe Gen 1, PCIe Gen 2, SATA Gen 1, SATA Gen 2, SATA Gen 3, SAS Gen 1, SAS Gen 2, SAS Gen 3, Thunderbolt 10G, and XAUJ.



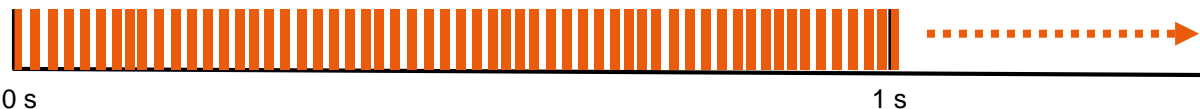
# HW-CDR TRIGGER FOR "LIVE EYE"

- ▶ Options: RTP-K136/137
- ▶ HW-CDR up to 8/16 Gbps
  - Trigger individual bits based on embedded clock
- ▶ Benefits
  - Fast results due to high acquisition rate
  - Continuously CDR running as time reference
  - Combinable with HW implemented Histogram and Mask Test
  - Combinable with Realtime Deembedding



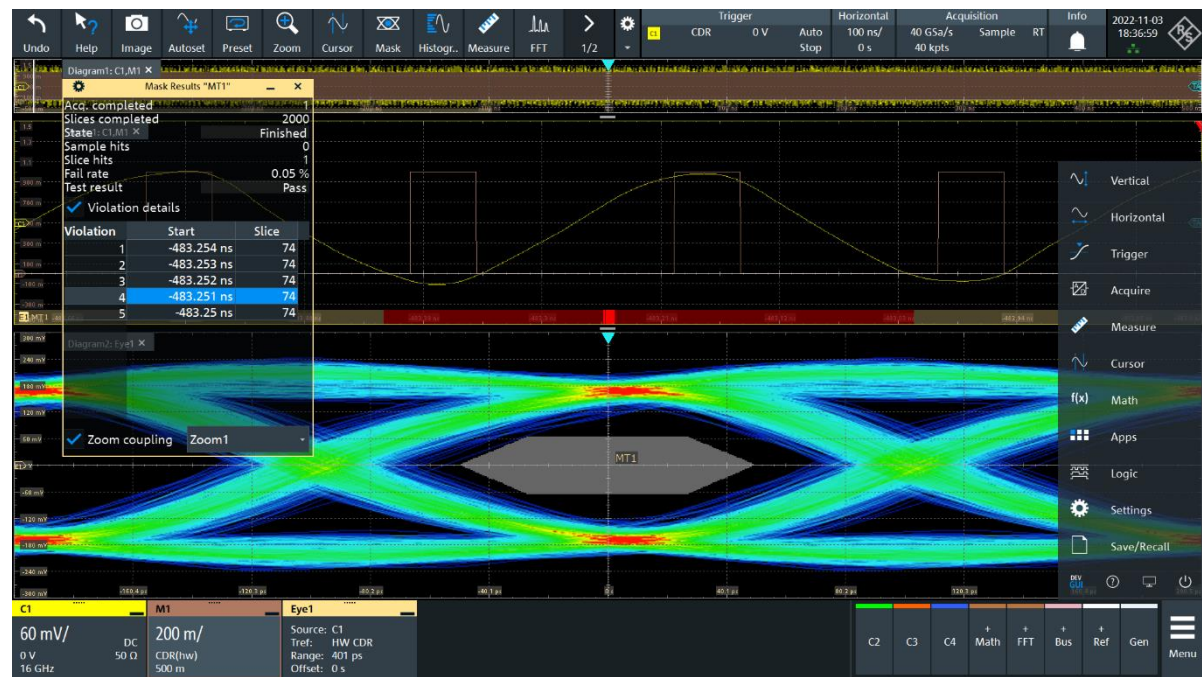
## Signal-integrity debugging:

- Fast glance on Jitter / Noise
- Long-term monitoring
- Use Mask and Histogram



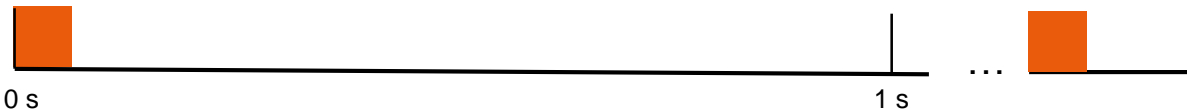
# HW-CDR TRIGGER FOR ADVANCED EYE ANALYSIS

- ▶ Options: RTP-K136/137
- ▶ HW-CDR up to 8/16 Gbps
  - Bit folding based on continuously running HW-CDR
- ▶ Powerful capabilities
  - HW-CDR as Math available
  - Powerful Filter & Qualify options
  - Saving of Data Eye
  - Automated eye measurements
  - Mask test w/ EyeStripe function
  - Mask test library for typical interface standards



## Signal-integrity characterization:

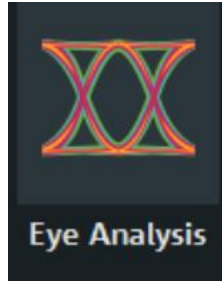
- Based on a long bit sequence
- Transmitter output and signal path characteristic
- Use Mask and Histogram



**FROM QUICK “AHA” TO THE DETAILS**

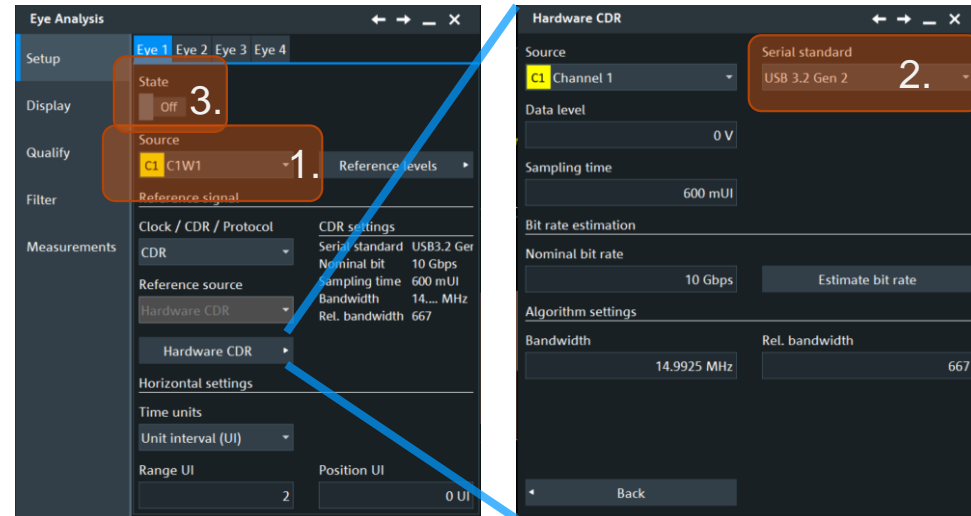
# ADVANCED EYE ANALYSIS

## EASY SETUP IN 3 STEPS



### Quick start with Eye Analysis

1. Select Source
2. Hardware CDR: Select Serial Standard
3. Set State: On

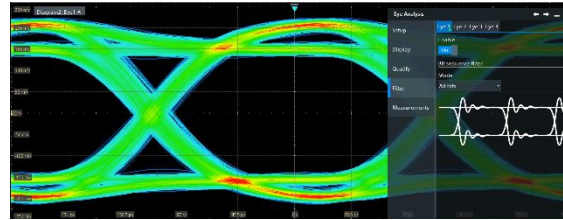


# ADVANCED EYE ANALYSIS

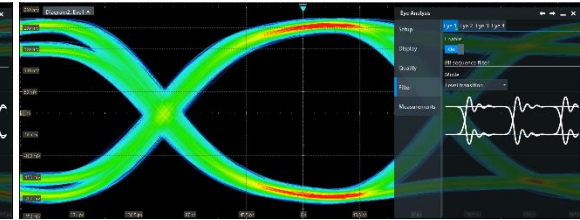
## TUNE YOUR SETUP

### Advanced settings:

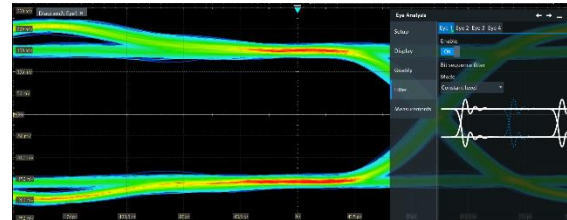
- ▶ Display:
  - color table, persistence,
  - „Eye stripe“
- ▶ Qualify:
  - Gate
  - Signal
- ▶ Filter:
  - All bits / level transition / constant level
  - Bit pattern



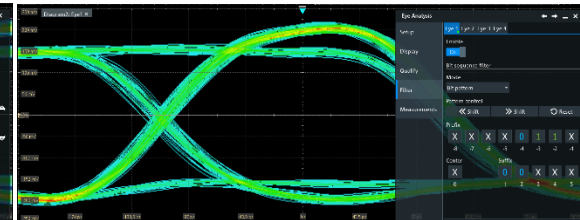
All bits



Level transition



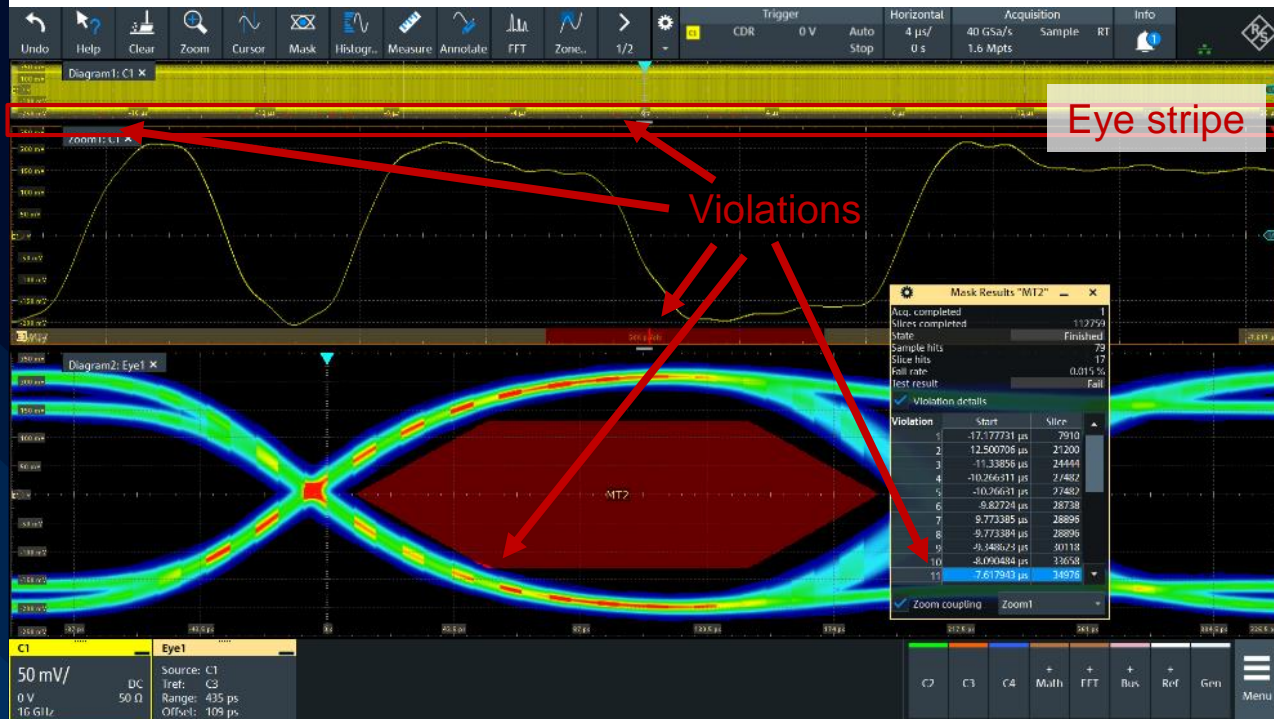
Constant level



Bit pattern

# EYE STRIPE

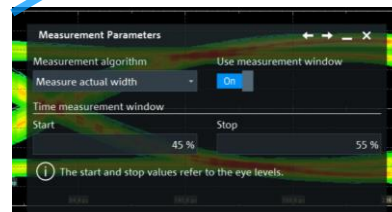
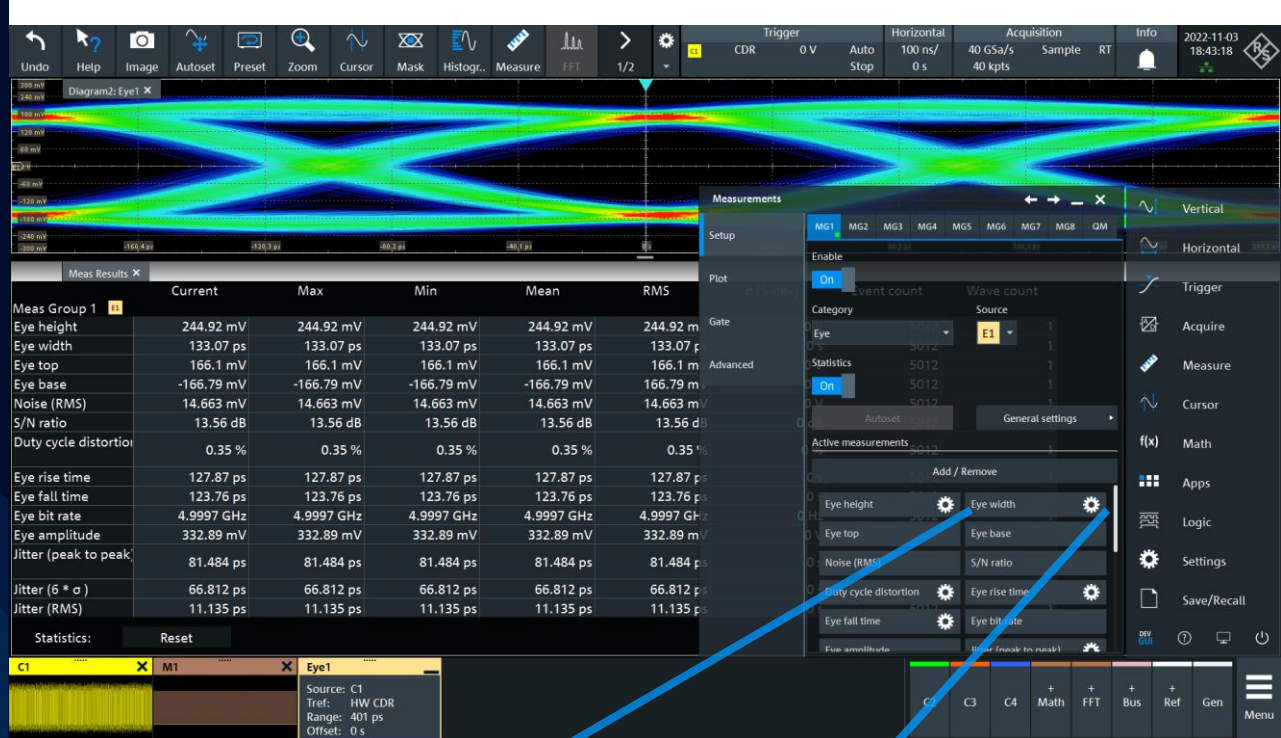
- ▶ Couples mask violations with position in waveform
- ▶ Easy navigation between violations
- ▶ Coupled zoom to investigate details
- ▶ Time-correlation to other signals possible





# AUTOMATED EYE MEASUREMENTS

- ▶ 18 automated measurements
- ▶ Configure detailed measurement parameters



**LIVE DEMONSTRATION**



# SUMMARY

# SUMMARY – ADVANCED EYE ANALYSIS GET YOUR RESULTS FASTER

- ▶ Traditional eye diagram approaches
  - a. “Live Eye” with edge trigger for long-term monitoring
  - b. Continued bit stream with SW-CDR processing for TX and signal path characterization
- ▶ New R&S approach: Hardware clock data recovery
  - Enables both, true “Live eye” and continued bit stream analysis with continuous running HW-CDR
  - Fastest approach to high statistical confidence
- ▶ In-depth analysis with „Advanced Eye“ tools



**THANK YOU.**

The image features a dark blue background. On the right side, there are several diagonal stripes of a lighter, medium blue color, creating a sense of movement and depth. The stripes are parallel and run from the top-left towards the bottom-right.