Smart eCockpit and In-Vehicle Safety Solution

Carl Chien / MPU CAS Manager

Successful examples with i.MX inside

Integration

Home Automation
& Building Control.

Eyeglasses for
visually impaired

Industrial and
Service Robotics
Industrial HMI and
Control

Transportation:
1. Inflight Entertainment,
2. Austin B-Cycles,
3. John Deere Tractor,
4. Hertz Neverlost

Educational Tablet

Surveillance
Camera

SONY, Amazon, Kobo eReaders

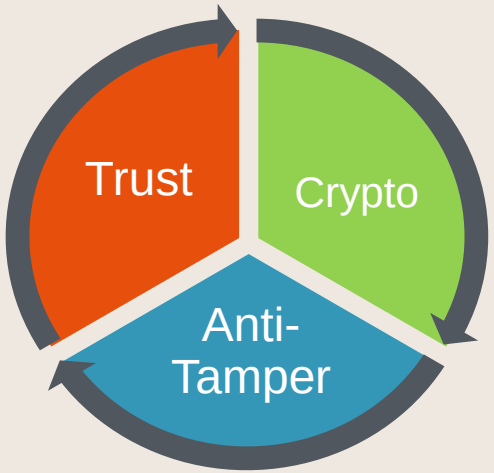
High end home
entertainment
HDD Audio
WiFi Speaker

Medical
Masimo, Philips,
Withings, etc.

Handheld devices:
Handheld Scanners,
Printers, POS and Mobile
Radios.

Why i.MX ?

Product Longevity



i.MX PROCESSOR VALUES

Trusted Supply

- Product longevity: Minimum 10 to 15 years
- Security and safety: Hardware acceleration, software
- Reliability: Zero-defect methodology, ULA, low SER FIT
- Quality: Automotive AEC-Q100, Industrial/Consumer JEDEC

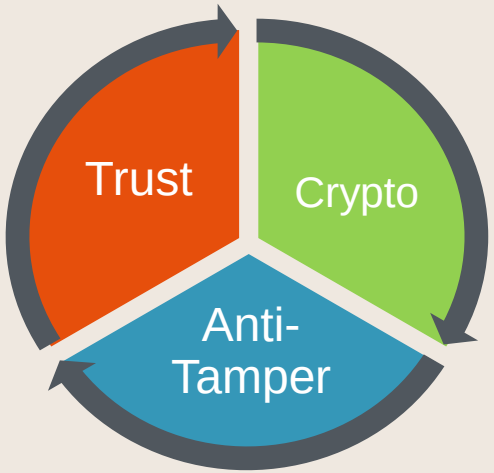
Scalability for Maximum Platform Reuse

- Pin compatibility and software portability
- Integration: CPU (single/dual/quad, asymmetric), GPU, IO
- Manufacturability: 0.65 to 0.8mm pitch, fewer PCB layers

Support and Enablement

- Software: Linux, Android, Windows-embedded, RTOS
- Industry-leading partners and support community
- System solutions: Voice, Video, Vision, Machine Learning, Sensors, Power Management, Connectivity

Product Longevity



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NXP Supply Longevity

Industrial/Automotive applications require product longevity

- Long product lifecycles
- Special product certification

NXP Processors

- NXP formally offers many devices for a minimum of 10 or 15 years from the time of launch
- Participating NXP products and program terms are listed at www.nxp.com/productlongevity

NXP Supply Longevity (Cont.)

				Longevity Years			
Category	Family/Series	Products	Launch Date	10 Years	15 Years	Extended	Remains in Longevity Program until
	i.MX 6 Series	Filter by...					
Processors	i.MX 6 Series	i.MX 6DualPlus	Feb 2016	✓	-	✓	Dec 2035
Processors	i.MX 6 Series	i.MX 6DualPlus (Industrial, Auto)	Feb 2016	-	✓	✓	Dec 2035
Processors	i.MX 6 Series	i.MX 6UltraLite	Sep 2015	✓	-	✓	Dec 2035
Processors	i.MX 6 Series	i.MX 6UltraLite (Industrial, Auto)	Sep 2015	-	✓	✓	Dec 2035
Processors	i.MX 6 Series	i.MX 6ULZ	Nov 2018	✓	-	✓	Oct 2031
Processors	i.MX 6 Series	i.MX 6QuadPlus	Feb 2016	✓	-	✓	Dec 2035
Processors	i.MX 6 Series	i.MX 6QuadPlus (Industrial, Auto)	Feb 2016	-	✓	✓	Dec 2035
Processors	i.MX 6 Series	i.MX 6SoloLite	Nov 2012	✓	-	-	Nov 2022
Processors	i.MX 6 Series	i.MX 6SoloX	Feb 2015	✓	-	✓	Dec 2035
Processors	i.MX 6 Series	i.MX 6SoloX (Industrial, Auto)	Feb 2015	-	✓	✓	Dec 2035

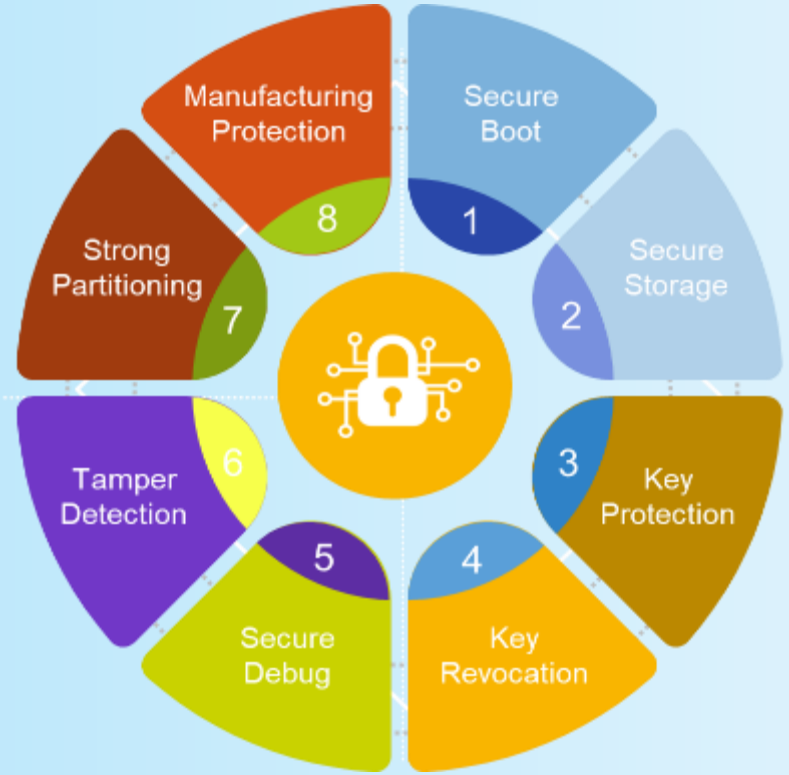
www.nxp.com/productlongevity

Security

Security

Covering every system vulnerability of the Product Life-Cycle

- **Design** – Hardware, IO, Storage: Trust Architecture
- **Manufacturing** – Key Generation, Provisioning, Updates: Secure Provisioning Tool
- **Software** – Operating System, Applications, Permissions: Trusted Linux
- **Connectivity** – Remote Access, Communications: Network Security Suite



i.MX SECURITY SCALABILITY

i.MX Family Security Features	6Quad, 6Dual, 6Solo	6SoloX	6UL	6ULL/Z	7Dual, 7Solo	7ULP	8ULP	8M Q/QL/D, Mini, Nano, Plus	8X Family 8QuadXPlus, 8DualXPlus	8 Family 8QuadMax, 8QuadPlus	91/93/95
Secure Enclave							✓ S400		✓ SECO	✓ SECO	✓ S400 (S500 – 95)
AES128/192/256, SHA1/224/256, DES/3DES	✓	✓	✓	AES 128	✓	✓	✓	✓	+ SHA 384/512	+ SHA 384/512	✓
Elliptic Curve (modulus up to 1024) RSA (up to 4096)			✓		✓		✓ S400	✓	✓ High performance	✓ High performance	✓ S400 (S500 – 95)
Hardware Crypto Accelerator	✓ CAAM	✓ CAAM	✓ CAAM	✓ DCP	✓ CAAM	✓ CAAM	✓ CAAM, S400	✓ CAAM	✓ CAAM & CAU	✓ CAAM & CAU	✓ 95 - V2X
Certifiable RNG	✓	✓	✓	✓	✓	✓	✓	✓	✓ CAVP	✓	✓
Run Time Integrity Protection (RTIC)			✓		✓		✓	✓	✓	✓	✓
Secure Execution (Trustzone TZ, TZ-M, SHE)	✓ TZ	✓ TZ	✓ TZ	✓ TZ	✓ TZ	✓ TZ	✓ TZ	✓ TZ	✓ TZ + SHE	✓ TZ + SHE	✓ TZ
High Assurance Boot (RSA/ECDSA)	✓ RSA	✓ RSA	✓ RSA	✓ RSA	✓ RSA	✓ RSA	✓ AHAB ECDSA	RSA (ECDSA on 8M Plus)	✓ AHAB	✓ AHAB	✓ AHAB ECDSA
Encrypted Boot	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓
Always ON domain	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓
Secure Storage (non-volatile)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Secure Key Storage	eFUSE	eFUSE	eFUSE	eFUSE	eFUSE	eFUSE	eFUSE	eFUSE	eFUSE	eFUSE	eFUSE
Tamper Detection Pins (Passive/Active)	✓	✓	✓ 10/5		✓ 8/4	✓ 1/0	✓ TBD		✓ Active	✓ Active	✓ TBD
Volt/Temp/Frequency Detection			✓		✓	✓			✓	✓	
Inline Encryption			BEE			OTFAD	IEE, OTFAD		IEE	IEE	IEE, OTFAD
Secure Debug	✓	✓	✓	✓	✓	✓	Domains	✓	Domains	Domains	Domains
Manufacturing Protection					✓		✓	✓	✓	✓	✓
Resource Domain Isolation (RDC,XRDC)		✓			✓	✓	✓	✓	✓	✓	✓
Content Protection	6Q 1.x only								DTCP	HDCP 1.x/2.x, DTCP	

NXP Edge Computing and Security Brand Platform

EDGEVerse™ Portfolio

Signature Software

eIQ™ Machine Learning

Immersiv3D™ Audio Framework

EdgeScale™ Device Mgmt

…

Embedded Processing

Apps Processors	Low Power Processors	Microcontrollers	Connectivity	Auto
i.MX Layerscape® …	i.MX 7ULP/8ULP …	LPC5500 K32 L3 MCX …	Bluetooth® LE Wi-Fi® …	S32 i.MX …

Turn-key Solutions

MCU-Based Solution for Alexa™ Voice Service

65 W+ Wireless Power for 5G

15 W Wireless Power for Auto

…

EDGELock™ Portfolio

EdgeLock SE	EdgeLock SA	EdgeLock	EdgeLock 2GO
Secure Element Products	Secure Authenticator Products	Embedded Security & Subsystems	IoT Service Platform

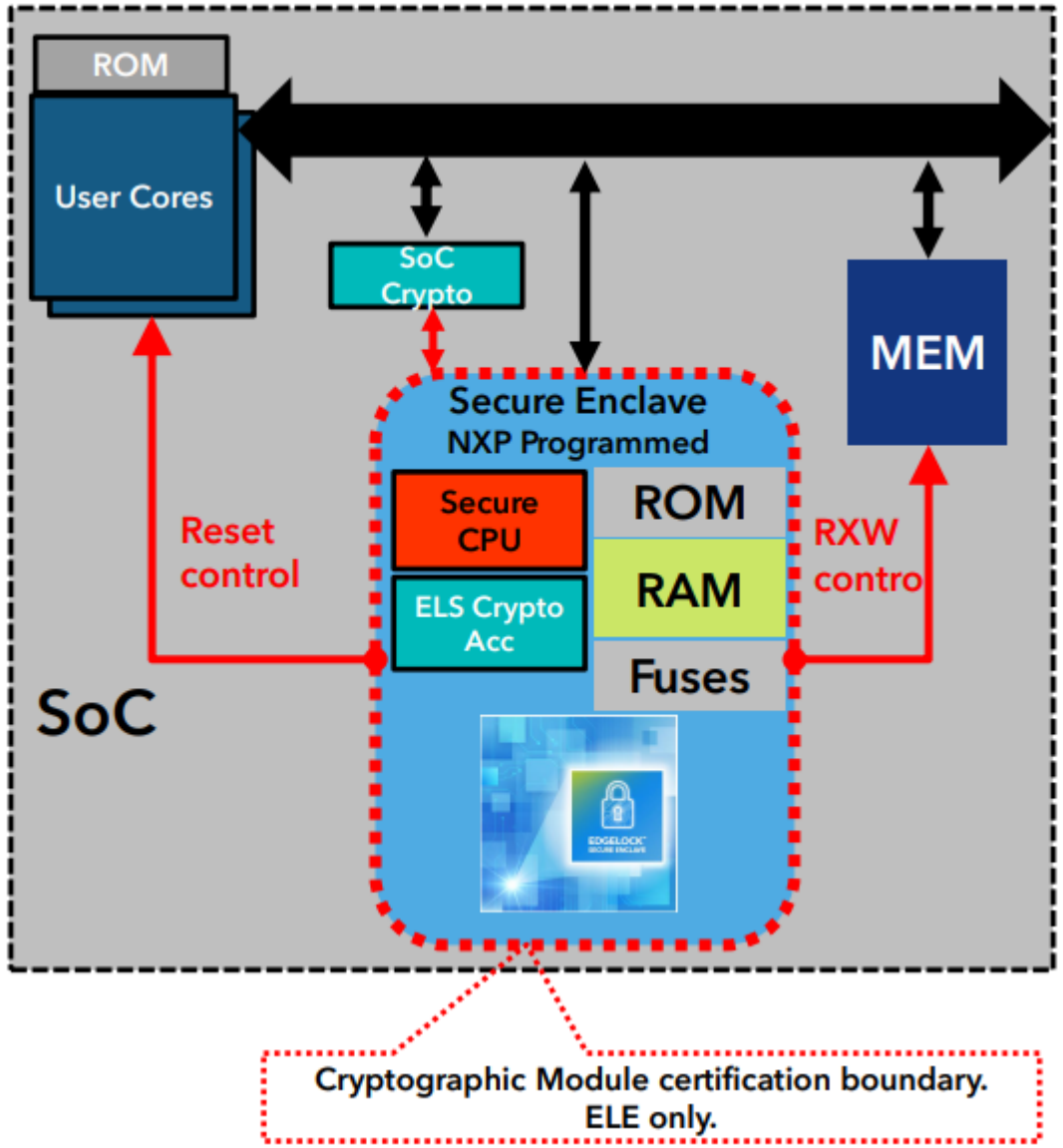
Security Certification

SoC/system level:

- SESIP– L2 (Equivalent to Arm PSA L2)
- OSCCA
- Supporting: IEC 62443, ISO/SAE 21434
- Amazon - AVS Security Requirements
  - *1.16. Device SHALL use a chipset that relies on hardware-based security capabilities and meets PSA certified Level 1 or similar.*

ELE as an integrated cryptographic module (HSM):

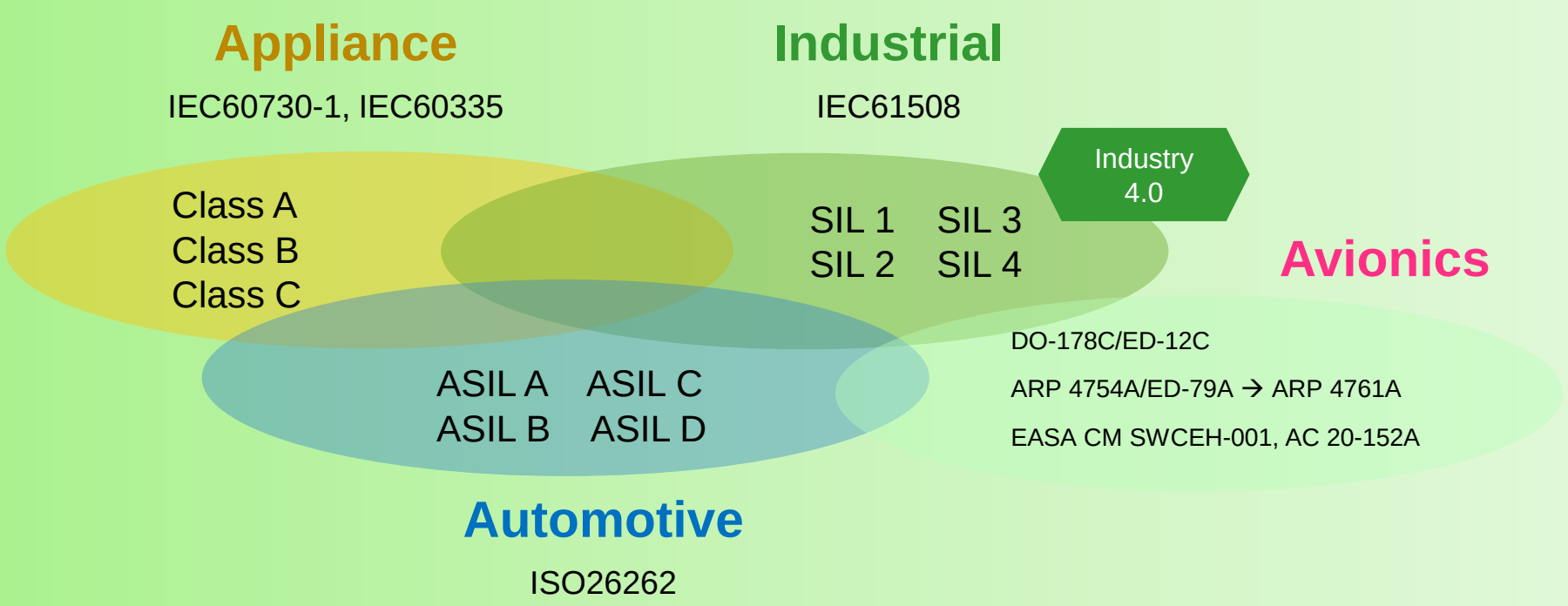
- Customer reusable, at the OEM product level.
- FIPS 140-3 L2: (On going for i.MX 93)



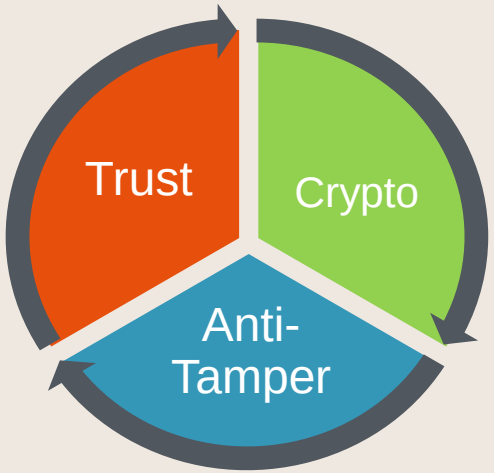
NXP Enables a Spectrum of Safety and Reliability

SAFE ASSURE™ by Freescale

Safety and Reliability



Product Longevity



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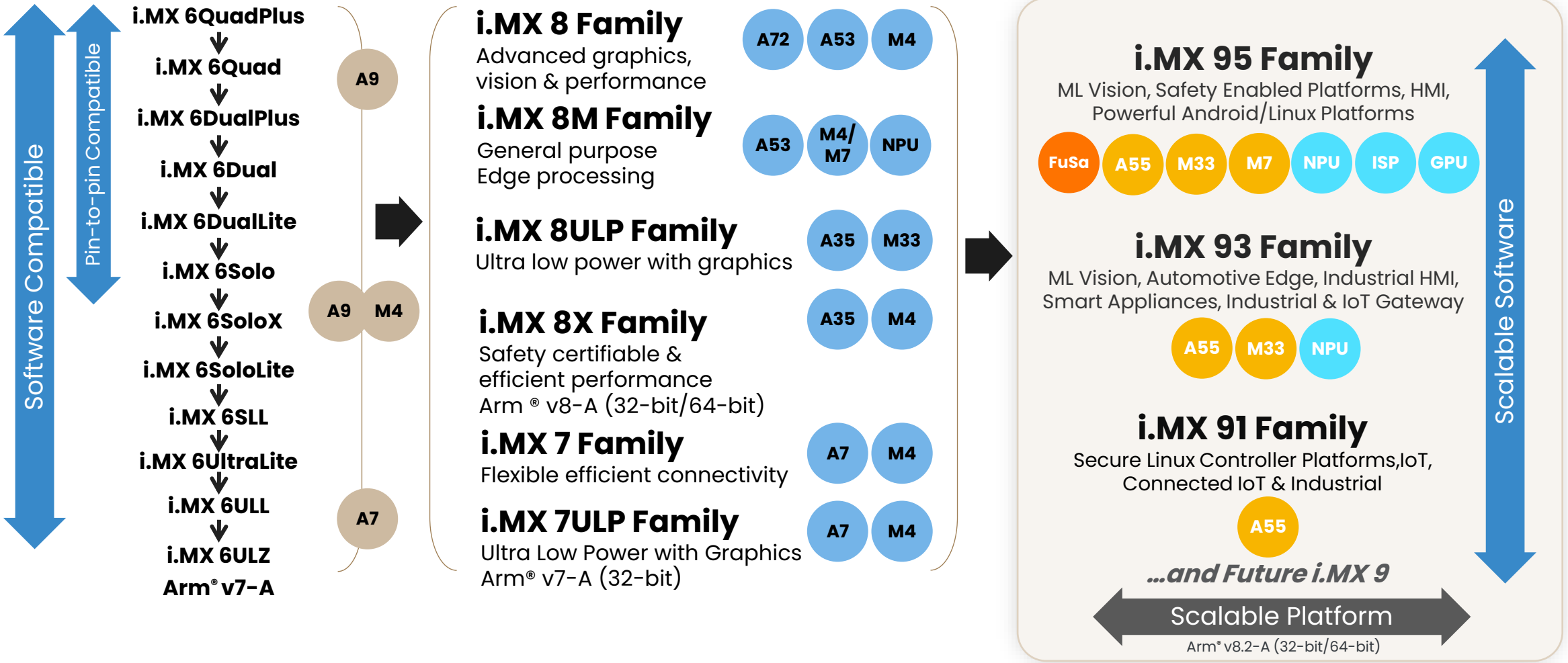
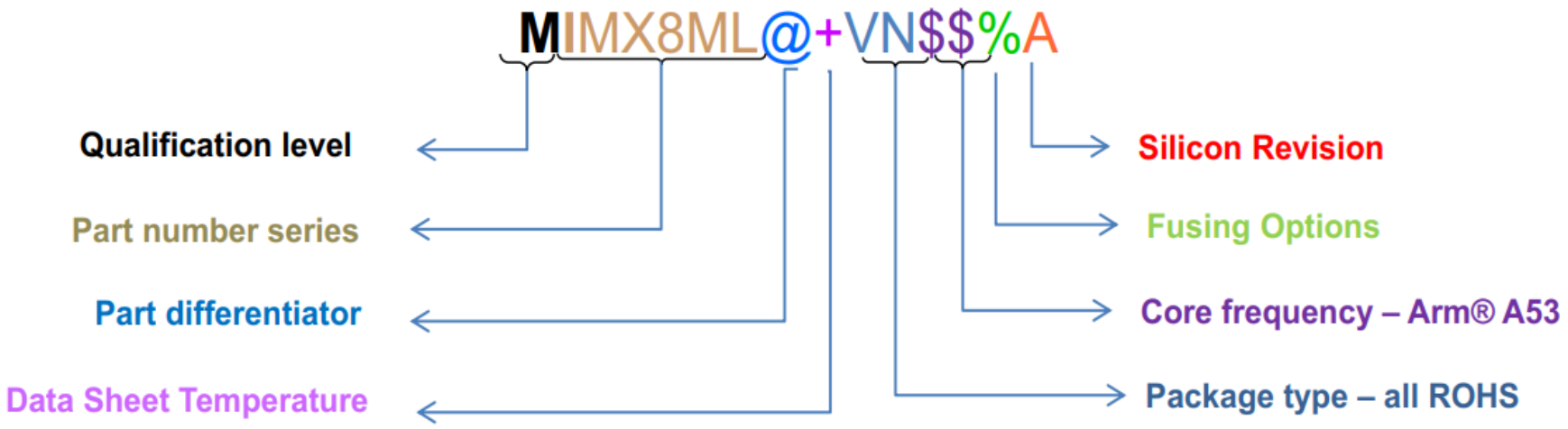
i.MX Applications Processors



Part number nomenclature



Qualification level	
Samples	P
Mass Production	M
Special	S

Part number Series	Description
IMX8ML	i.MX 8M Plus

Part differentiator	@
i.MX 8M Plus Quad 4x Arm® Cortex®-A53, VPU, NPU, ISP, HiFi 4	8
i.MX 8M Plus Quad 4x Arm® Cortex®-A53, VPU, ISP	6
i.MX 8M Plus QuadLite 4x Arm® Cortex®-A53	4
i.MX 8M Plus Dual 2x Arm® Cortex®-A53, VPU, NPU, ISP, HiFi 4	3

Temperature Tj	+
Consumer: 0 to +95°C	D
Industrial: -40 to 105°C	C

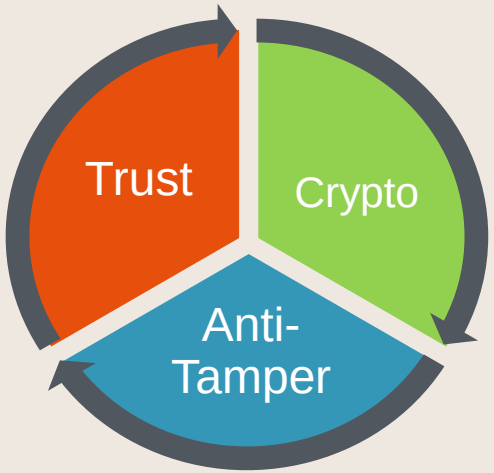
Package type	ROHS
FCBGA548 15 x 15 mm, 0.5 mm pitch	VN

A53 core frequency	$$
1.8 GHz	LZ
1.6 GHz	KZ

Fusing	%
-	A
Immersiv3D enabled w/Dolby Atmos	C
Immersiv3D enabled w/Dolby Atmos and DTS	D

Silicon Rev	A
Rev A1	B

Product Longevity



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Software Enablement

Strongest Operating Systems for NXP Processors

Supplier	Arm Cortex-A cores i.MX 6, 7, 8 & 9 series	Arm Cortex-M cores LPC & Kinetis MCUs; i.MX RT, 6SoloX, 7, 8 & 9 series
NXP Semiconductor	Linux Long Term Support (LTS) OS, supported in the Yocto Project; Android OS, Windows 10 IoT Enterprise	FreeRTOS (complementary); MQX RTOS (commercial); Zephyr (i.MX RT now, i.MX 8 future)
Mentor Embedded	Linux OS; Nucleus RTOS	Nucleus RTOS
QNX	Neutrino RTOS	-
Green Hills	INTEGRITY RTOS	u-VelOSity RTOS
Wind River	Linux OS; VxWorks RTOS	VxWorks RTOS
Microsoft (Express Logic)	WindowsCE; Win10 IoT; Azure RTOS (formerly ThreadX)	Azure RTOS (formerly ThreadX)
Canonical (LTS support)	Ubuntu and Ubuntu Core (commercial support available)	-
Timesys	Commercial Linux	-
DDCI, Sysgo…	DEOS RTOS, Pike OS…	-
Micrium (Silicon Labs)	uC/OS II / III RTOS, Micrium OS	uC/OS II / III RTOS, Micrium OS

eIQ ML SW Development Environment

Embedded Developers

Data Scientists

ML Experts

eIQ Toolkit

eIQ Marketplace

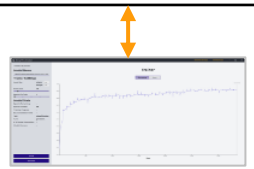
Value-Add Solutions and Services

eIQ Portal

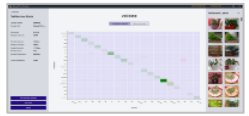
Bring Your Own Data Workflow

Data Curation

Model Selection



Model Training, Optimization, Quantization



Model Validation

Bring Your Own Model Workflow

PyTorch Caffe2 ONNX

PyTorch Caffe2 ONNX

eIQ inference

Applications running on EdgeVerse processors

ANOMALY DETECTION	VOICE RECOGNITION	FACE RECOGNITION	MULTI-OBJECT CLASSIFICATION	COMPLEX DIAGNOSIS

eIQ inference with…

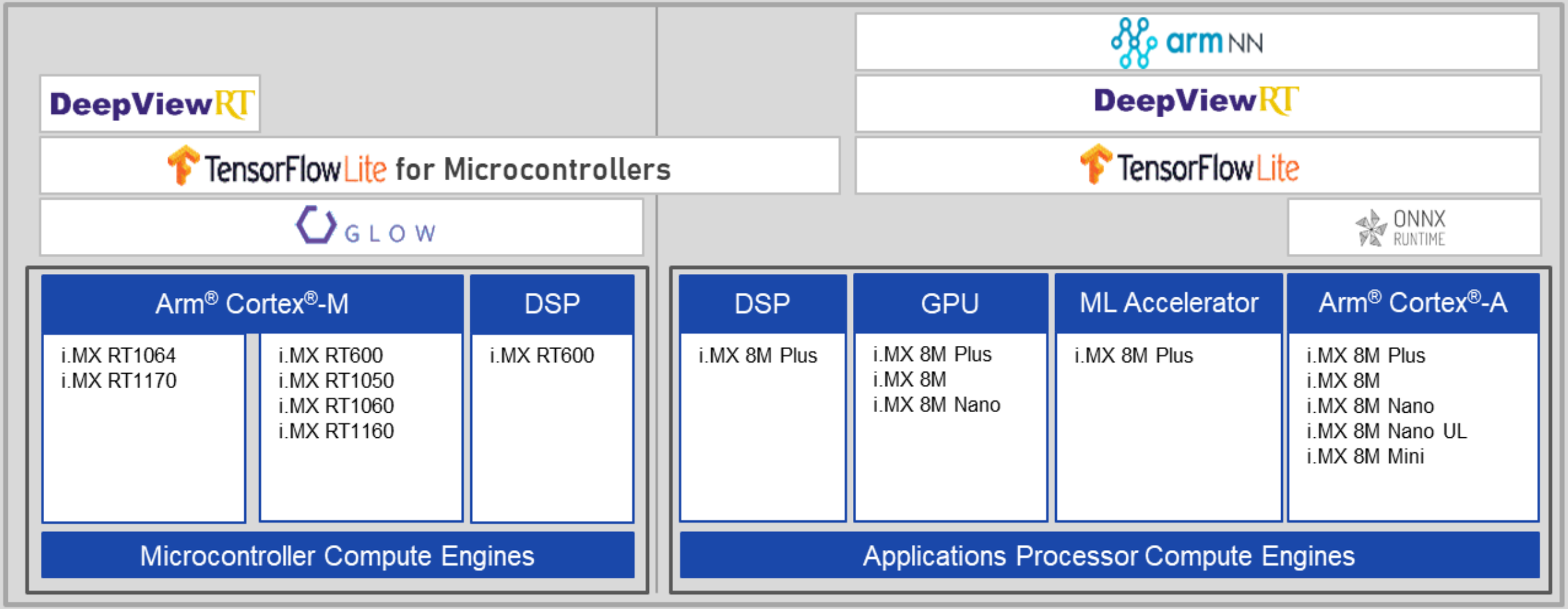
TFLite-Micro	Glow	DeepViewRT™	TFLite	Arm NN	ONNX Runtime	DeepViewRT™

Arm® Cortex®-M, DSP

Arm Cortex-A, GPU, DSP, NPU

NXP eIQ™ ML Software Development Environment

Inference Engines and Libraries for Neural Network Model Deployment

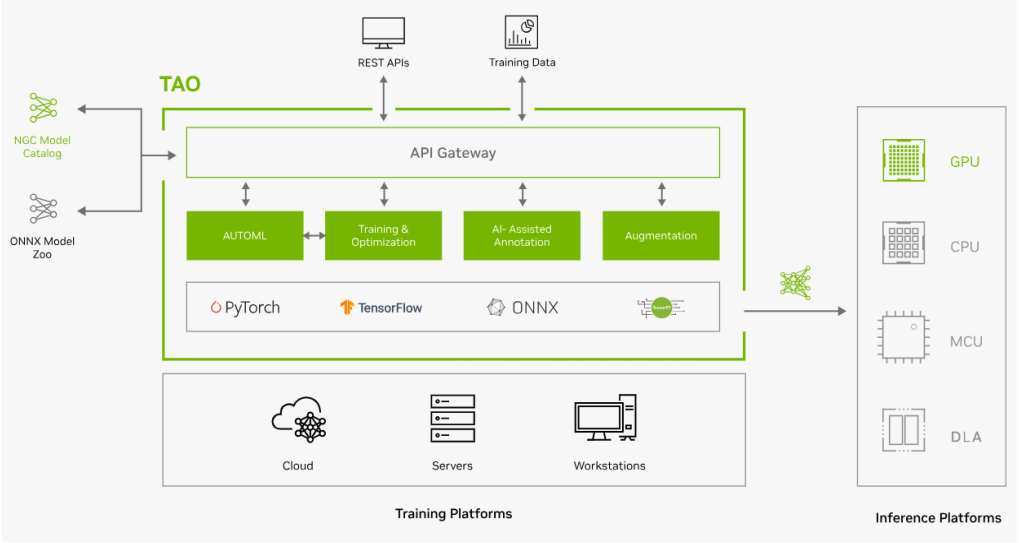


* Additional support for devices not listed can be available

NXP Collaborates with NVIDIA to Accelerate AI Deployment with Integration of TAO Toolkit with NXP Edge Devices

March 18, 2024 6:00 PM EDT (UTC−4) by NXP Semiconductors Press Release

- NXP is the first semiconductor vendor to integrate NVIDIA TAO Toolkit APIs directly with its AI enablement offering, the eIQ machine learning development environment
- Enables NVIDIA's trained AI models to be deployed on NXP's edge processing devices
- Accelerates AI development by making it easier to deploy trained AI models at the edge



[NXP Collaborates with NVIDIA to Accelerate AI Deployment with Integration of TAO Toolkit with NXP Edge Devices | NXP Semiconductors]

Hardware Enablement

i.MX 8M Plus Evaluation Kit

Base Kit: Compute Module + Base Board

Kit Contents
- i.MX 8M Plus CPU module
- Base board
- USB 3.0 to Type C cable.
- USB A to micro B cable
- USB Type C power supply.

Compute Module: Overview
- NXP i.MX 8M Plus
- Murata Wi-Fi Type 1MW (CYW43455) 802.11 a/b/g/n/ac 1x1
- PMIC NXP PCA9450CHN
- 6GB LPDDR4;16 GB eMMC5.1
- 64MB QSPI Flash
- Target: 8-layer PCB
- Target Size: 2”x2”

OS Support
- Linux, Android and FreeRTOS BSPs from NXP
- Others: 3rd parties

Place holder Picture

Part Numbers:
IMX8MPLUSLPD4-EVK

Base Board: Overview
- MiniSAS Display Connectors
  - 1x MIPI-DSI
  - 1x LVDS
- MiniSAS Camera connectors
  - 2x mini-SAS MIPI-CSI
- 1x HDMI
- Audio DAC
- Microphone/headphone jacks (TBD)
- 1x micro SD card slot
- 2x 10/100/1000 Ethernet port (1x w/ TSN)
- USB 3.0 Type C for power
- 1x USB 3.0 Type A
- 1x USB 3.0 Type C
- Connectivity expansion:
  - M.2 connector (PCIe)
- General purpose expansion connector (RPI-like): UART, PDM, SPI, SAI
- 2x CAN-FD
- 10-pin JTAG
- Micro USB for console
- Target Size 8” x 6”

Optional Add-ons

xxxx MIPI CSI Board miniSAS based **MINISASTOCSIxxxx**

OLED MIPI DSI Board miniSAS based **MX8-DSI-OLED1**

MIPI-DSI to HDMI miniSAS based **IMX-MIPI-HDMI**

Audio Board **MCIMX8M-AUD** ***future**

EVKs accessory

4-Cam Board
miniSAS Based
MX8-8X-MIPI4CAM

OV10635 MIPI Camera
MCIMXCAMERA1MP

MIPI to HDMI
miniSAS Convertor
IMX-MIPI-HDMI

LVDS to HDMI
miniSAS Convertor
IMX-LVDS-HDMI

OV5640 MIPI CSI board
miniSAS based
MINISASTOCSI

BroadReach 100 Mbps PHY
IMX-RMII-BRPHY

Std 1Gbps PHY
IMXAI2ETH-ATH

BroadReach Switch (100Mb/s)
IMXAI2SWCH-NXP

MIPI-DSI OLED
MX8-DSI-OLED1

i.MX 8M Audio Board
MCIMX8M-AUDIO

Wi-Fi/Bluetooth module
Dual-band 2 × 2 802.11ac with MU-MIMO +
Bluetooth 4.2
Murata 1CQ (QCA6174A)

Automotive

i.MX Automotive Target Applications

Cluster & Infotainment

- Low/mid eCockpit
- Standalone infotainment
- Standalone cluster

Telematics & Connectivity

- Low to high Telematics
- Smart Antenna systems
- Connectivity Domain Controllers

Display & HMI

- DMS / OMS
- Standalone touch / displays

DMS (Driver Monitoring System) + OMS (Occupant Monitoring System)

ICMS (In-Cabin Monitoring System)

EU Regulation for ICMS

EU Regulation on Driver Drowsiness and Attention Warning Systems Published

According to an analysis of road traffic accident statistics carried out on behalf of the European Commission, driver fatigue is a contributory factor in 10-25% of all road traffic accidents which occur in the European Union. For this reason, the fitment of Driver Drowsiness and Attention Warning (DDAW) systems was one of the new safety features identified by the European Commission for inclusion in their updated General Safety Regulation. EU Regulation 2019/2144 on "the type approval requirements of motor vehicles and their trailers, and systems, components and separate technical units intended for such vehicles, as regards their general safety and the protection of vehicle occupants and vulnerable road users", more commonly referred to as General Safety Regulation 2 or GSR 2, requires the mandatory fitment of Driver Drowsiness and Attention Warning (DDAW) systems to all new types of M and N category vehicle (i.e. all passenger carrying and goods carrying motor vehicles) from July 6, 2022, and to all new vehicles falling into those categories from July 7, 2024.

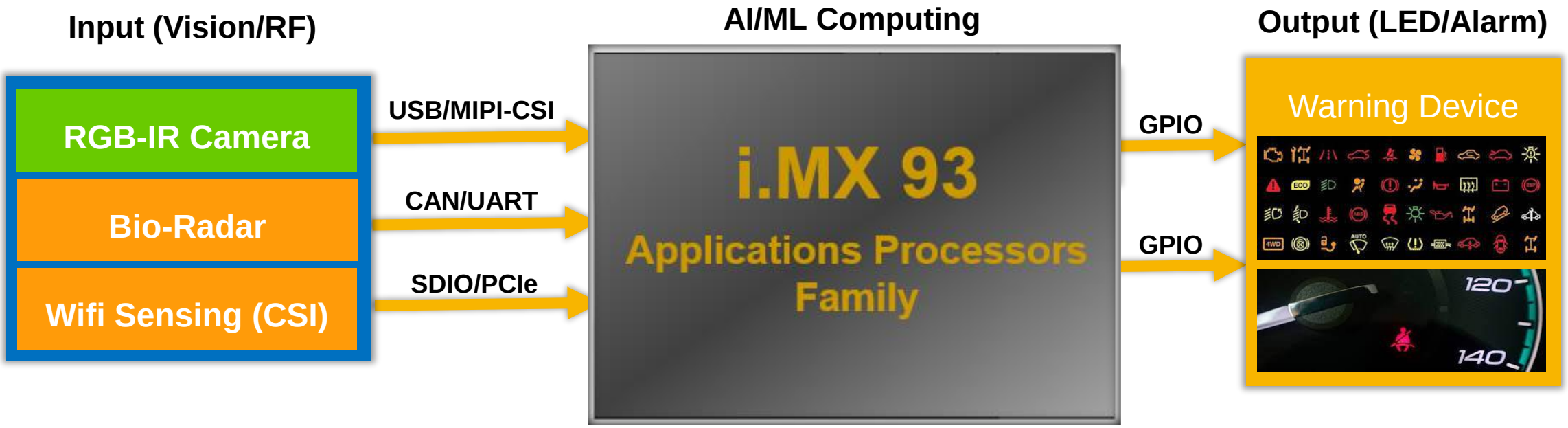
InterRegs Spotlight: EU Regulation on Driver Drowsiness and Attention Warning Systems Published

FOR SAFER CARS
EURO NCAP

★★★★★

5 star safety: Overall excellent performance in crash protection and well equipped with comprehensive and robust crash avoidance technology

In-Cabin Monitoring System (ICMS)



Use case: Doze, Yawn, Smoke, Phone, Seatbelt…

i.MX 93 Family: market positioning

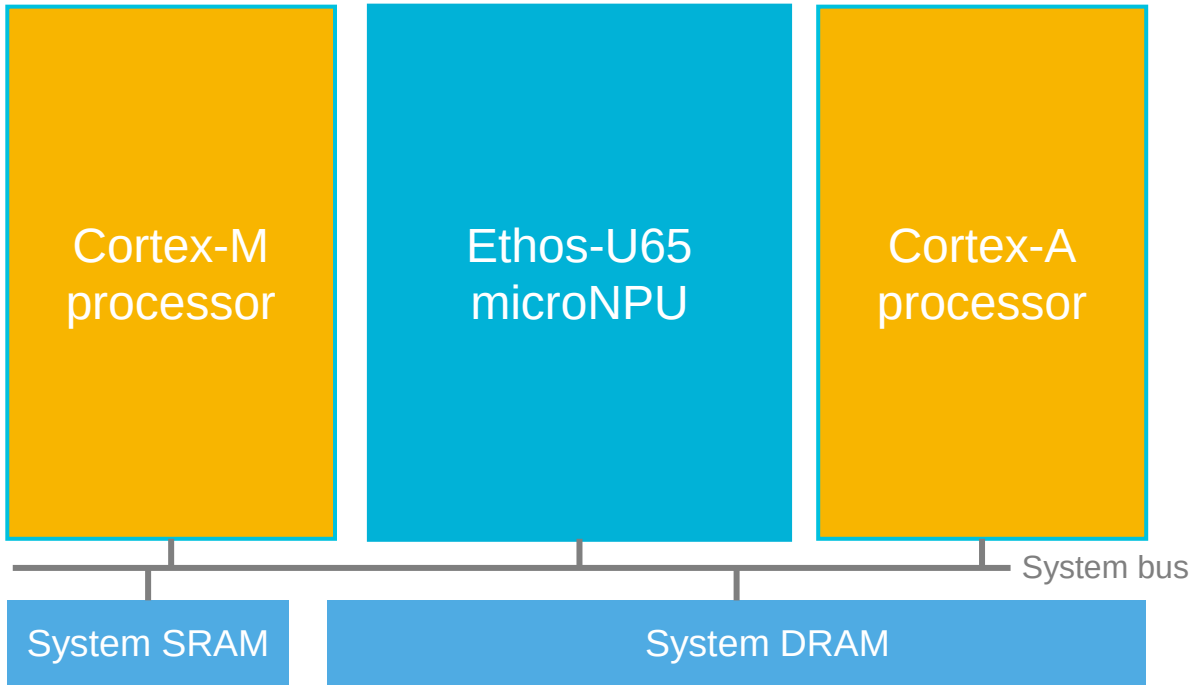
"Intelligent and secure edge processor family for entry-level SoC" with key features including

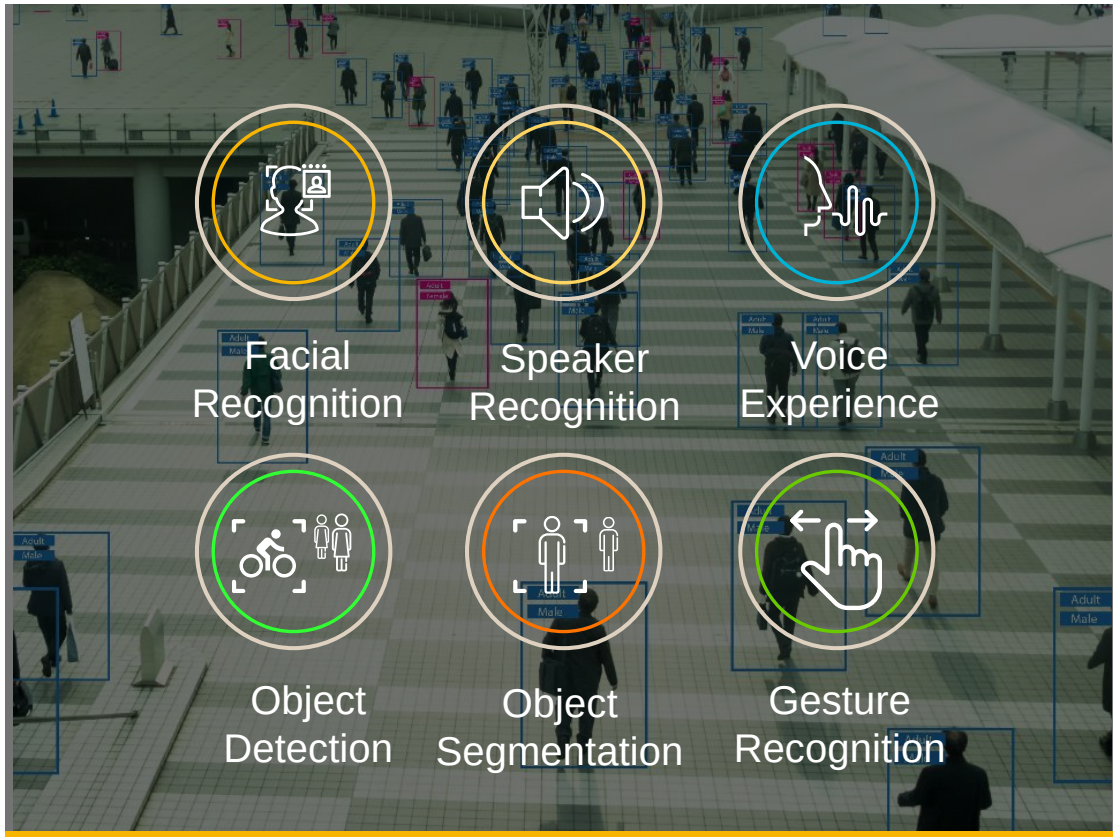
- EdgeLock® Secure Enclave subsystem to provide necessary security functions, dedicated NPU for efficient processing for ML applications in next-gen IoT market products
- Heterogenous processing of A55 + M33 cores (can boot from either core) with energy flex architecture for entry/mid-tier IoT applications that require high performance and low power
- Great Vision pipeline including MIPI-CSI interface along with 2x A55 and NPU to achieve cost-efficient vision applications across industrial, consumer IoT and auto markets
- Rich set of interfaces including 2x 1GbE, multiple audio channels, multiple display interfaces for a broad range of applications such as HMI, factory automation, audio soundbars

i.MX 93 Applications Processor Features

Product	i.MX931x/932x	i.MX933x/935x	i.MX930x
Main CPU	1x/2x A55 1.7GHz Arm® v8.2-A	1x/2x A55 1.7GHz Arm v8.2-A	1x/2x A55 900MHz Arm v8.2-A
	64kB L2 + 256kB L3 cache (ECC)		
MCU	1x M33, 250MHz Arm v8-M		1x M33, 133MHz Arm v8-M
	16kB+16kB cache (ECC), 256kB TCM/OCRAM (ECC)		
DDR	3.2GT/s x16 LPDDR4X/LPDDR4 Inline ECC	3.7GT/s x16 LPDDR4X/LP4 Inline ECC	1.8 GT/s x16 LPDDR4X/LP4 Inline ECC
GPU	PXP Engine: Blending/Composition, Rotation, Resize, Color Space Conversion		
Security	EdgeLock® Secure Enclave		
AI/ML	Efficiency NPU		No NPU
SRAM	Up to 640kB (ECC)		
Camera	8-bit parallel YUV/RGB	1080p60 MIPI CSI (2-lane), 8-bit parallel YUV/RGB	
Display I/F	24 bit per pixel parallel RGB	1080p60 MIPI DSI (4-lane) or 720p60 LVDS (4-lane) or 24 bit per pixel parallel RGB	1080p60 MIPI DSI (4-lane) or 24 bit per pixel parallel RGB
Connectivity	SDIO, USB2	SDIO, USB2	SDIO, USB2
Audio	SPDIF Tx/Rx, 8 channel PDM mic input, MQS output (sigma-delta modulator)		
	3x I2S TDM (32-bit @ 768KHz)	7x I2S TDM (32-bit @ 768KHz),	
Expansion I/O	8x UART/USART/Profibus, 8x I2C, 8x SPI, 2x I3C, 2x 32-pin FlexIO		
	1x USB 2.0, 1x 2-ch 12-bit ADC	2x USB 2.0, 1x 4-ch, 12-bit ADC	
Network/Storage	1x GbE, 2x CAN-FD, 3x SD/eMMC, Octal SPI	2x GbE (1x TSN), 2x CAN-FD, 3x SD/eMMC, Octal SPI FLASH	
Package	9x9mm, 0.5mm de-pop, 138 I/Os	11x11mm, 0.5mm de-pop, 198 I/Os 14x14mm, 0.65mm de-pop for auto, 198 I/Os	11x11mm, 0.5mm de-pop, 198 I/Os

Expanding edge ML with Arm® Ethos™-U65





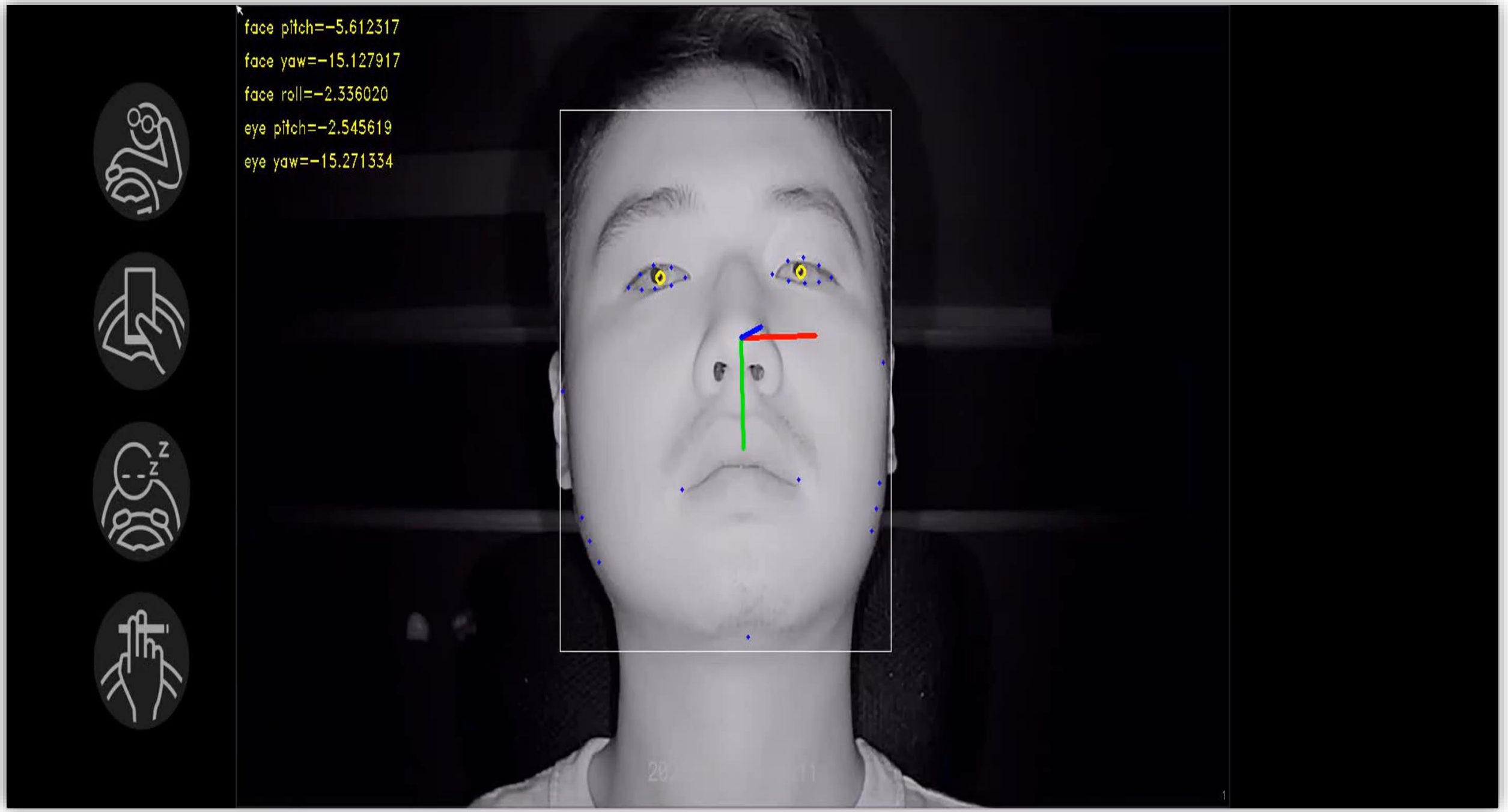
- Efficient (power, performance and area) hardware accelerator for entry-level ML applications
- Higher pipelining resulting higher utilization of NPU (>70%)
- Ethos-U65 provides ~10X better performance (inference/sec) than Cortex A55 for most models
- Comprehensive software and tools with NXP's eIQ® ML Software Development Environment

POWER & PERFORMANCE EFFICIENT NPU FOR ENTRY-LEVEL ML APPLICATIONS

i.MX93 VS i.MX8M PLUS NPU

Performance (inferences/sec)	i.MX8M Plus (2.3 TOPS) (NPU with 256KB SRAM)	i.MX93 (0.5 TOPS) (NPU with 384KB SRAM)
MobileNet-v1	368	218
MobileNet-v2	332	243
Inception v3	30	30
ResNet50-v1	60	20
SSD-MobileNet_v2	137	119
Geometric Mean	125	82
Performance relative to i.MX 8M Plus (geomean of benchmarks)	**1.00**	**0.66**

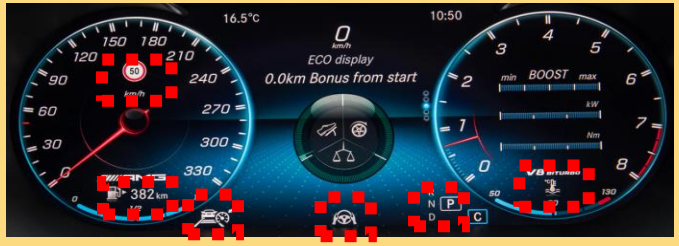
- DDR peak NPU bandwidth for i.MX8M Plus is 8 GB/s and for i.MX93 is 3.75 GB/s)
- Accuracy within 0.5% of FP32 reference


face pitch=-5.612317
face yaw=-15.127917
face roll=-2.336020
eye pitch=-2.545619
eye yaw=-15.271334

i.MX automotive target applications

Cluster & Infotainment

- Low/mid eCockpit
- Standalone infotainment
- Standalone cluster

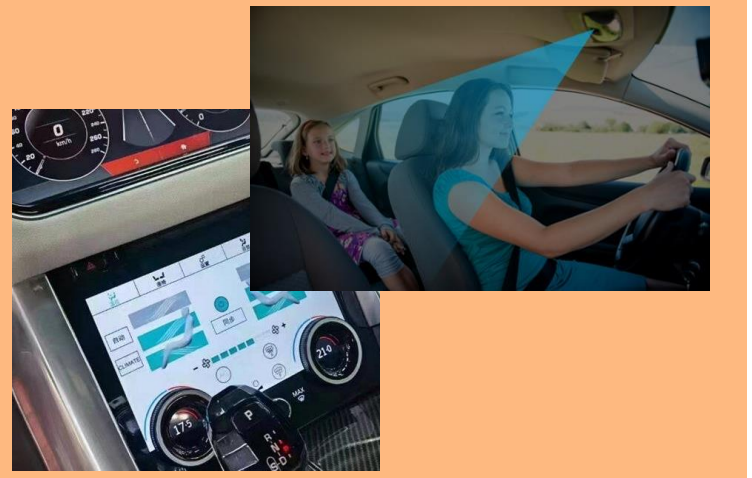


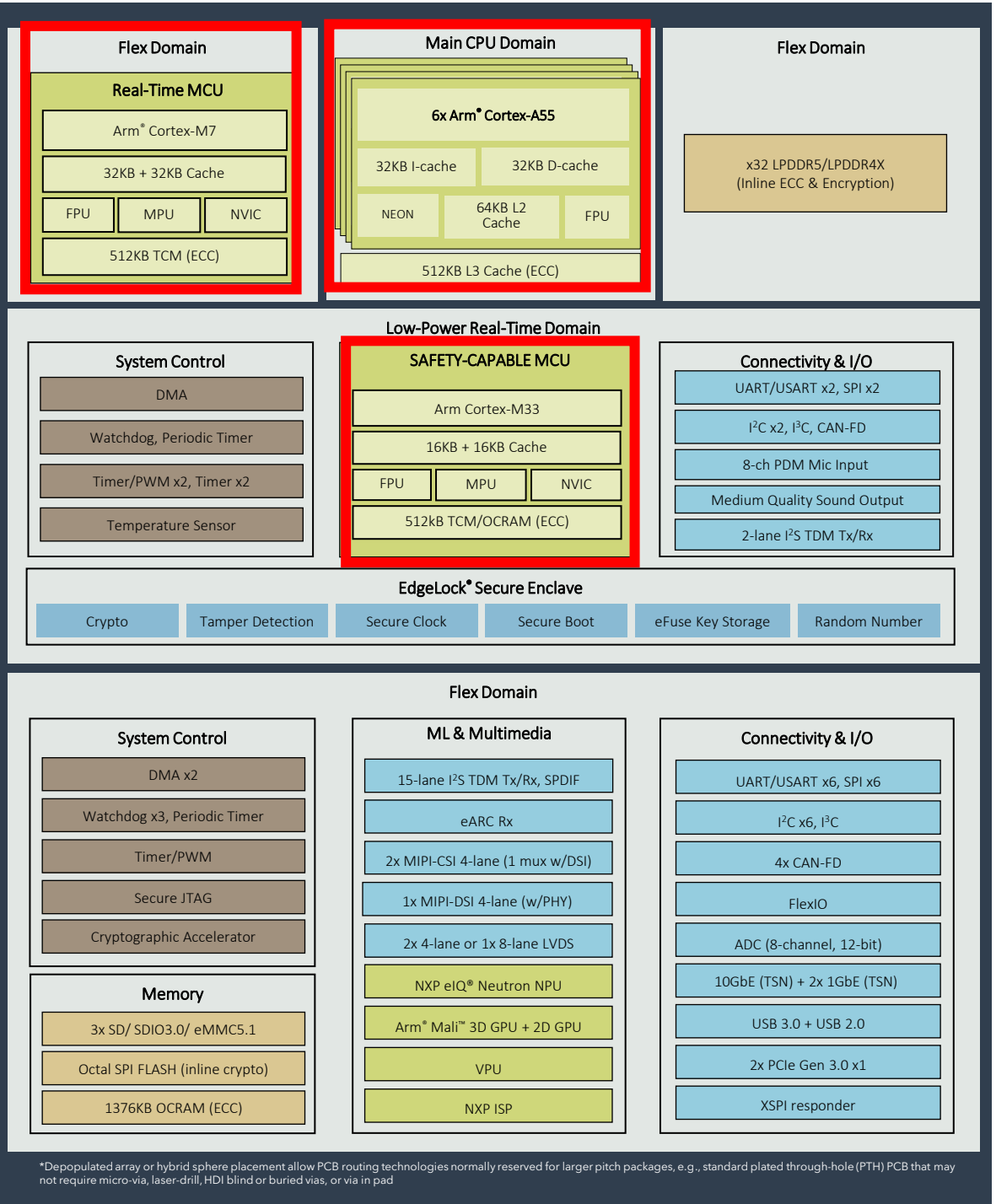
Telematics & Connectivity

- Low to high Telematics
- Smart Antenna systems
- Connectivity Domain Controllers

Display & HMI

- DMS / OMS
- Standalone touch / displays
- MCU expansion (off-chip memory)





*Depopulated array or hybrid sphere placement allow PCB routing technologies normally reserved for larger pitch packages, e.g., standard plated through-hole (PTH) PCB that may not require micro-via, laser-drill, HDI blind or buried vias, or via in pad

i.MX95 application processor family

- **Application Domain**: **6x Arm Cortex-A55**@Up to 2.0 GHz (Arm v8.2 64-bit capable)
- **Real-Time Domains**:
  - **1x Cortex-M7** @ 800 MHz, 32KB + 32KB Cache (ECC) w/512KB TCM SRAM (ECC)
  - **1x Arm Cortex-M33** @ 333 MHz, 16KB + 16KB cache (ECC) w/ 512KB TCM SRAM (ECC)

Energy Flex Architecture

- Multiple power islands can be clock-gated or power-gated when not used
- Logic runs full speed at 0.8V or 50% speed at 0.75V
- SRAM retention mode (0.65V)

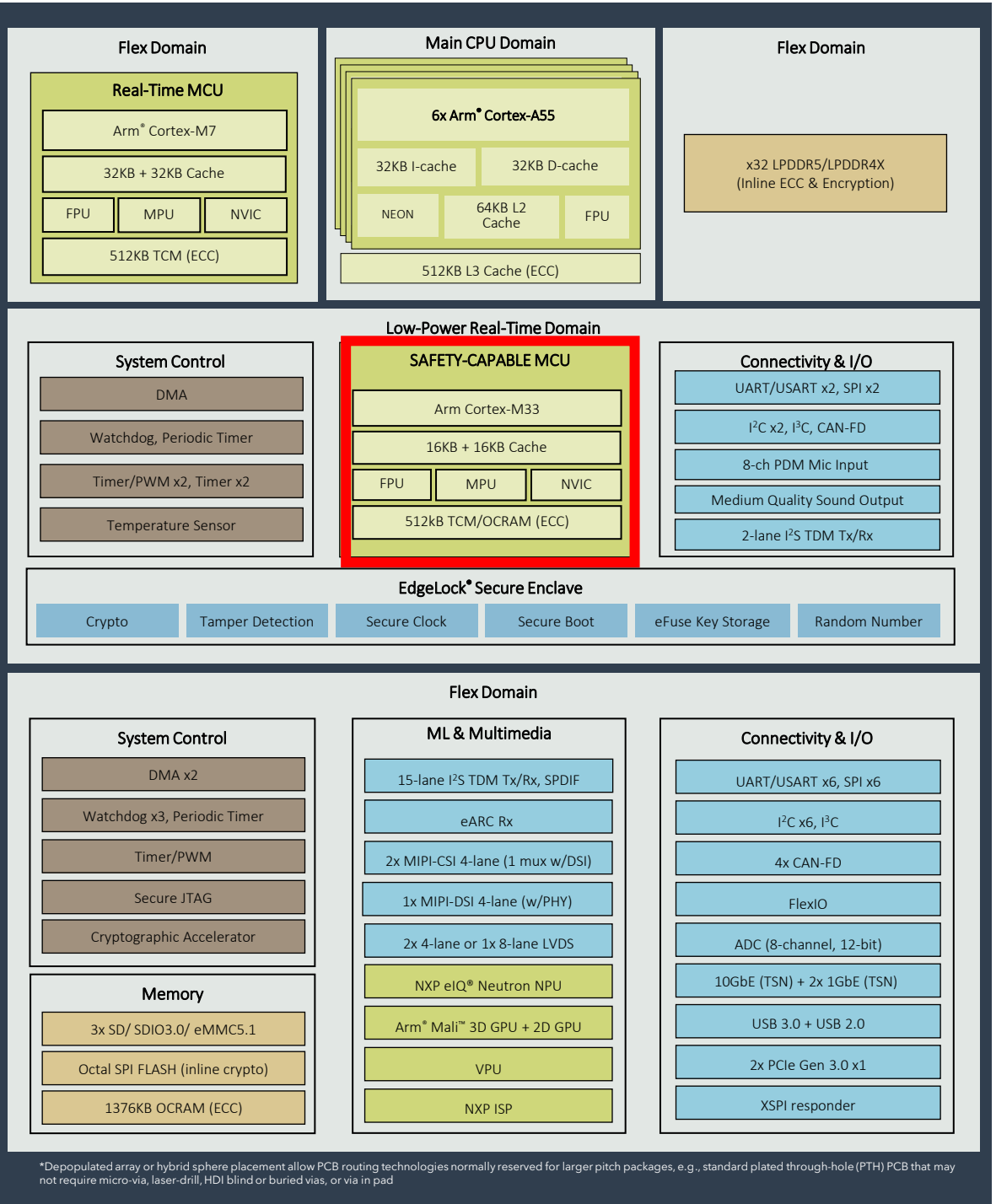
Cortex-A55 cores support:

- A55 sleep mode – stop executing code
- Each A55 has independent frequency control
- Each A55 can be independently power-gated
- DVFS on entire A55 complex (0.75V – 0.9V)

Customer can choose to power GPIO at 1.8V or 3.3V

Support for multiple low power modes including suspend to DRAM

Extensive tools for optimizing power in the real world, including power-instrumented EVKs, real-time power monitoring via graphical and text interfaces



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i.MX95 application processor family

Safety: NXP SafeAssure for ISO 26262 ASIL-B & IEC 61508 SIL-2 compliant platforms

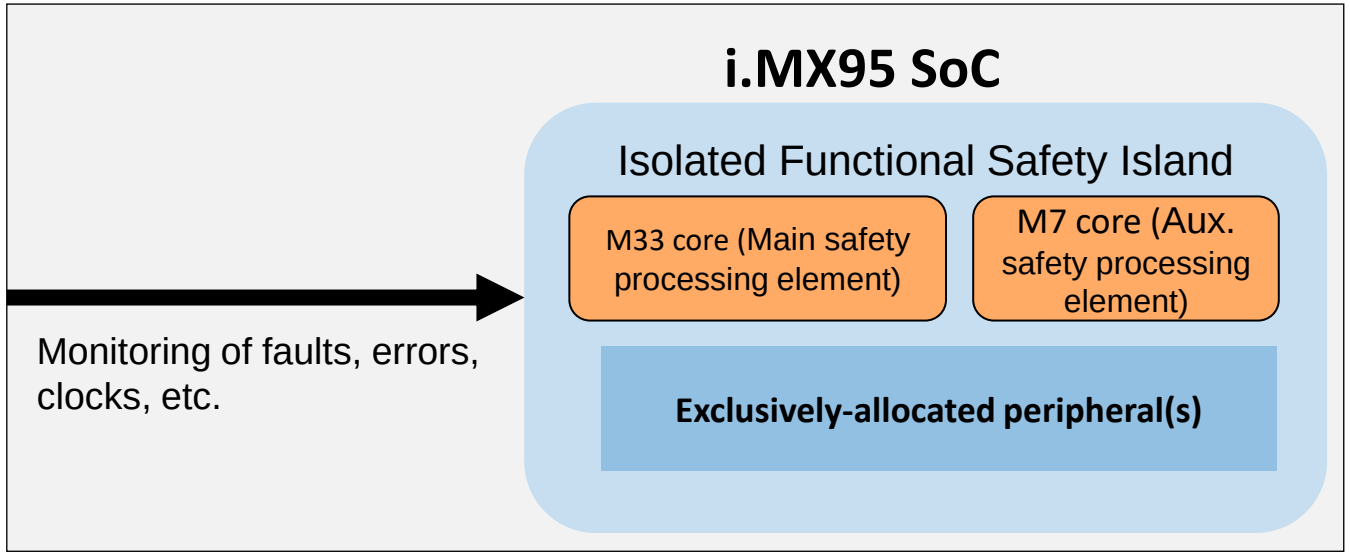
SAFE ASSURE™

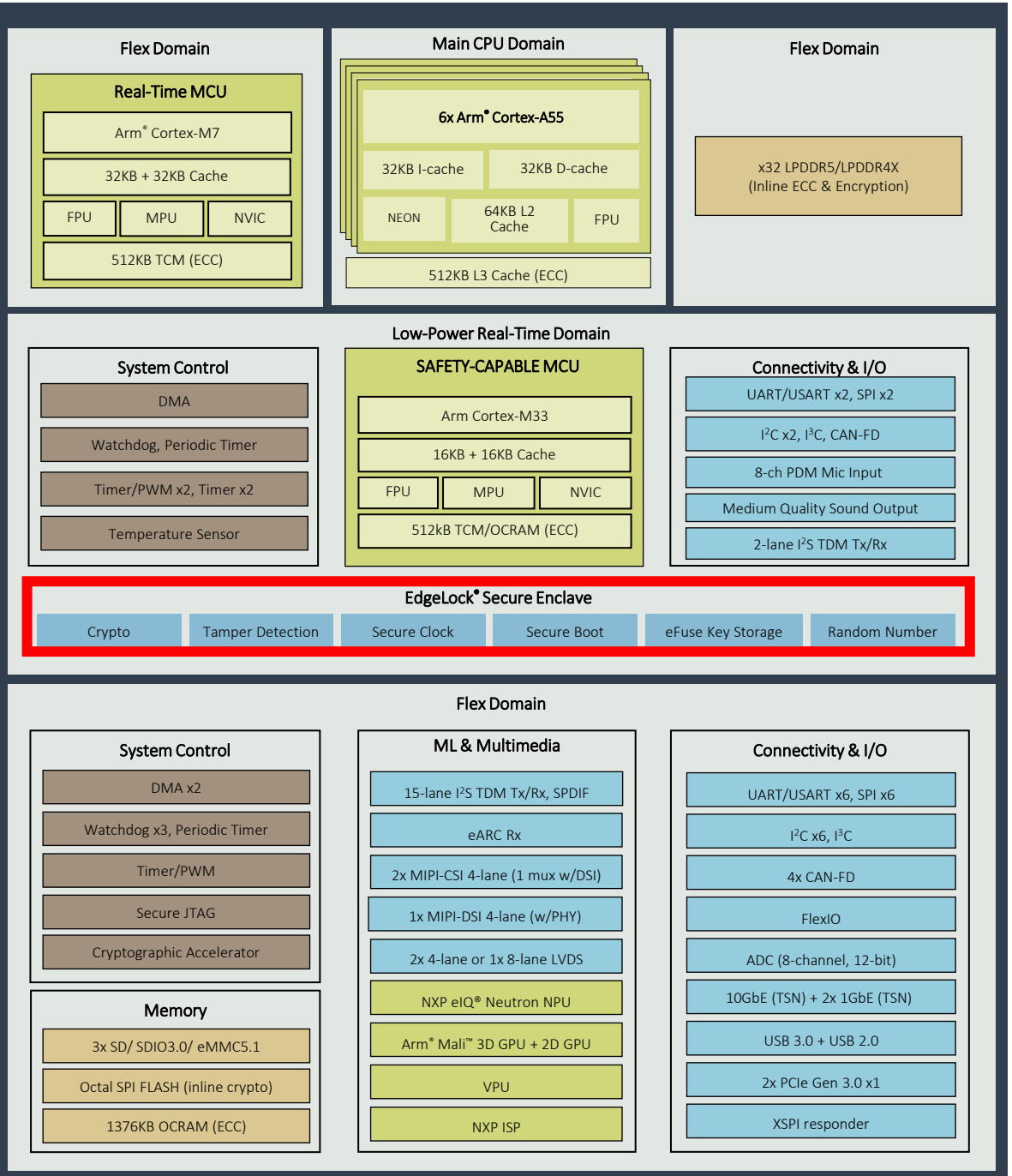
Goals of Functional Safety solution:

- Enable customers to implement safety monitoring SW
- Provide sufficient diagnostics to avoid undetected miscomputation
- Prevent non-safety components from interfering with the safety components

Automotive Use-cases

- Targeting ASIL-B
- Monitor regions of interest on Automotive display for failure condition, (optional) failover rendering of regions of interest by safety island
- Provide failover operation of vehicle audio (chimes, etc) and rear-view camera





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i.MX95 application processor family

- **Security**: **Edgelock Secure Enclave + V2X Cryptographic Accelerator**

EDGELOCK Secure Enclave

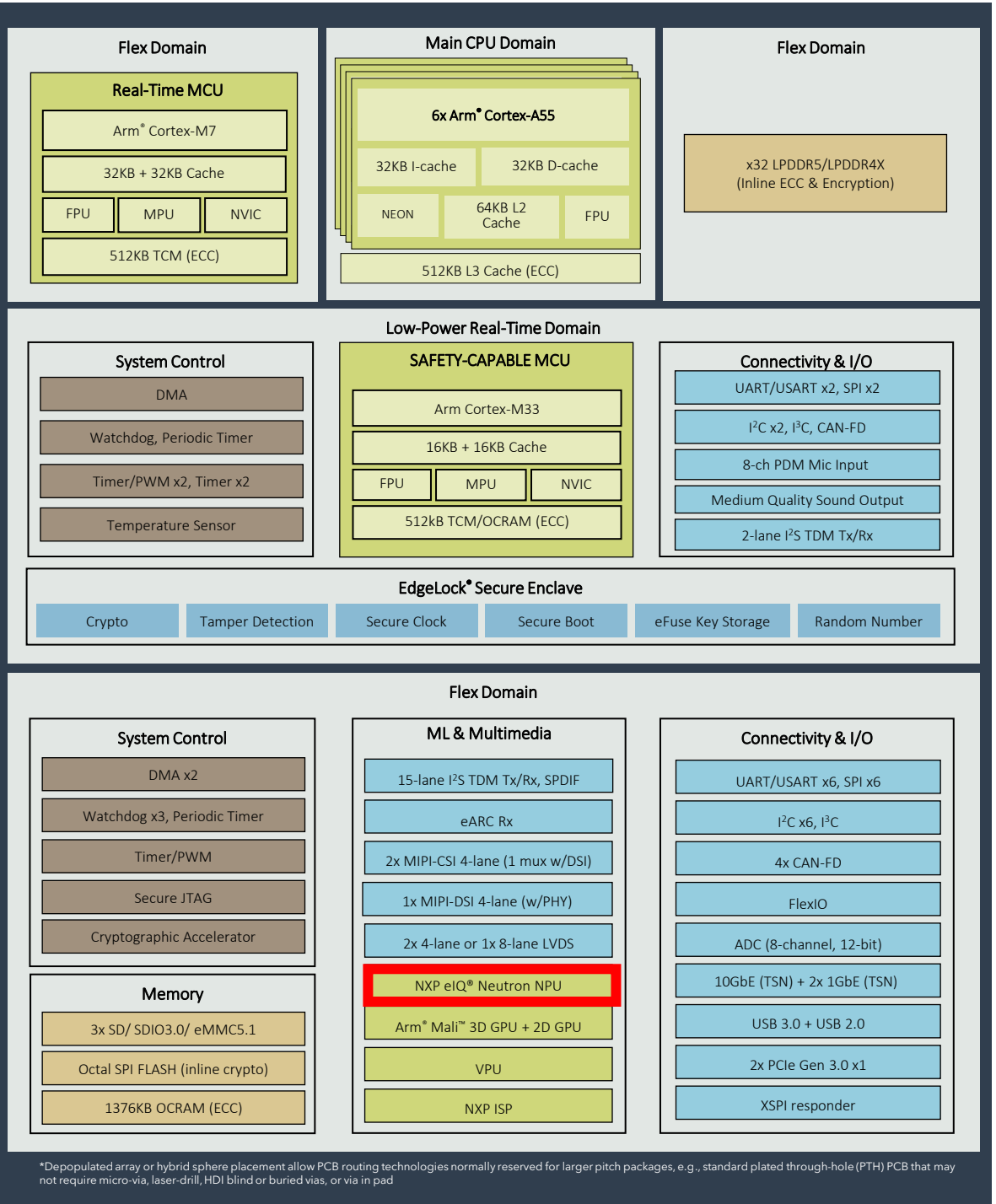
- Physically isolated security island – primary HSM
- Hardware root-of-trust
- Manages secrets for the SoC
- Provides crypto services
- Distributes keys to other masters via trusted buses

EDGELOCK® ASSURANCE by NXP

V2X Cryptographic Accelerator

- Accelerates ECDSA sign/verify to >3000 Ops/sec
- Provides fast SHA-2 performance for authenticated boot
- SHE / EVITA compliance (no internal NVM)
- Digital Rights Management (DRM) acceleration (when not used for V2X)

V2X VEHICLE-TO-EVERYTHING



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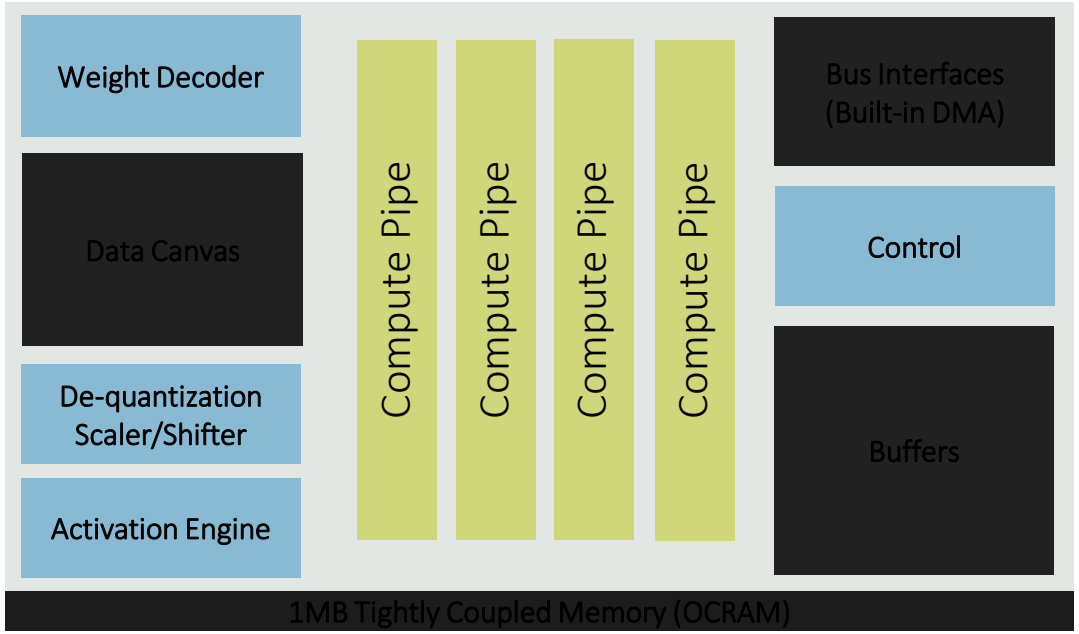
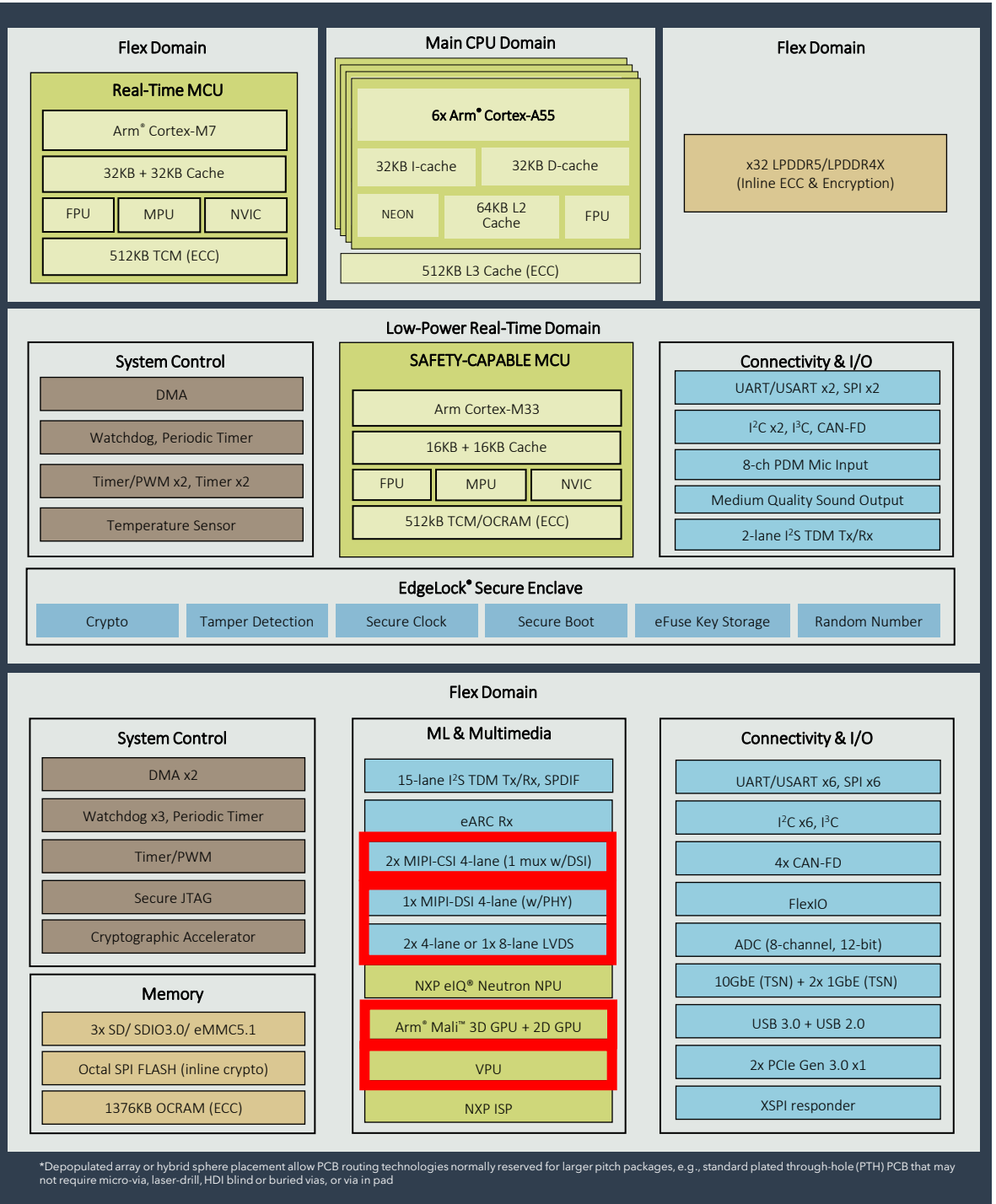
i.MX95 application processor family

- **Machine Learning**: **NXP eIQ® Neutron NPU**

Single Architecture With Great Scalability

- Optimized for performance and power efficiency
- ML solution development support with eIQ® ML SW Development Environment
- H/W scales from performance efficient 32 Ops/cycle to 2k Ops/cycle
- S/W support is unified over multiple generations and device portfolio





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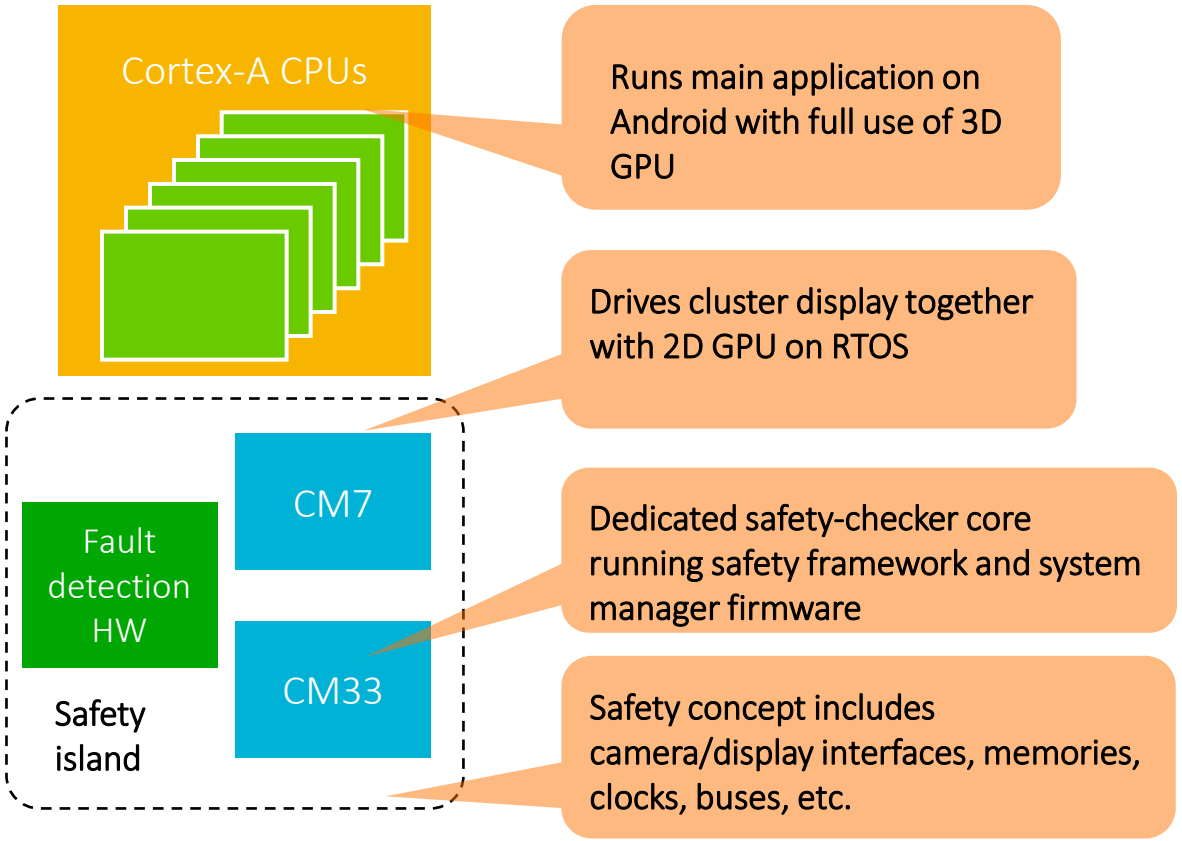
i.MX95 application processor family

- **3D Graphics**: **Arm Mali G310 GPU** (OpenGL® ES 3.2, Vulkan ® 1.2, OpenCL 3.0)
- **Display Controllers** (up to 3 simultaneous displays):
  - 1x 333Mpixel/s MIPI-DSI (4-lane, 2.5 Gbps/lane) supporting 4K30 or 3840x1440P60 display resolution
  - Up to 1080P60 LVDS Tx (2x 4-lane or 1x 8-lane)
- **Camera & Image Signal Processing**: **NXP ISP with RGB-IR support**
  - Up to 500 Mpixel/s throughput MIPI-CSI (2x 4-lane, 2.5 Gbps/lane) with PHY (1 mux with DSI)
  - Up to 1x4K60, 2x4K30, 4x1080P60 or 8x1080P30 cameras with MIPI virtual channels
- **Video Processing**:
  - 4K60 H.265/H.264 decode or encode (4K30 H.265/H.264 simultaneous encode & decode)
  - up to 32 streams

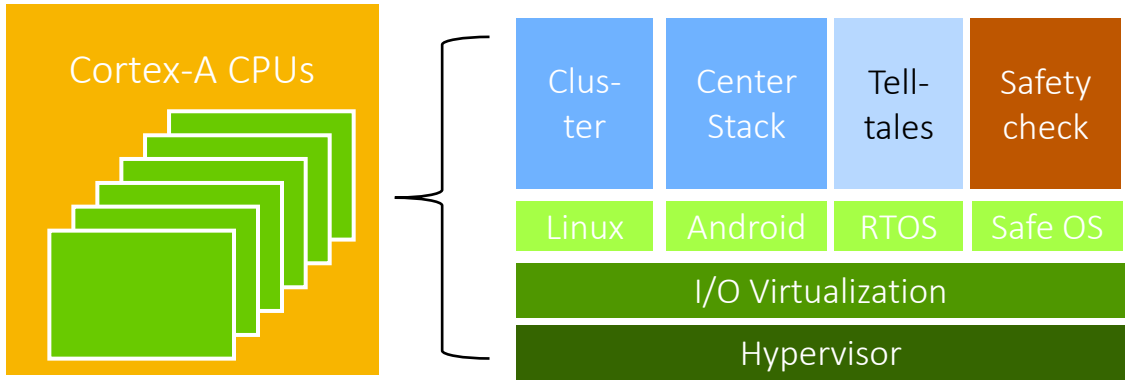
i.MX 95 enables e-cockpit solution without hypervisor

- Reduced load & far less complex software on Cortex-A CPUs and GPU
- Cluster boots up fast on real-time core and is isolated from Android O/S
- NXP ASIL-B software offering: “SafeAssure Framework” – in production today on i.MX 8

NXP i.MX 9 hypervisor-less solution



Competition smartphone-derived solution

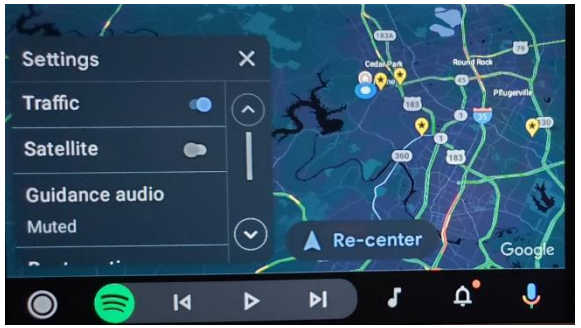


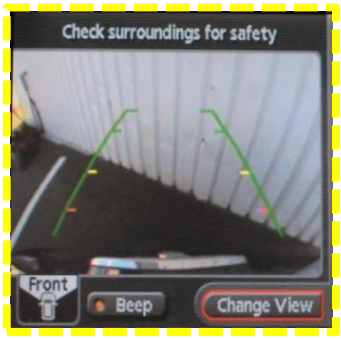
- Complex software architecture
- Cost of hypervisor $$$
- Hypervisor impact on CPU & GPU performance
- No hardware fault detection
- Requires external ASIL-B MCU

e-Cockpit without hypervisor on i.MX95

Real-time & ASIL-B cluster elements rendered by Cortex-M7 / RTOS & 2D-engine

Center stack / 3D elements rendered by Cortex-A55 / Android & 3D GPU

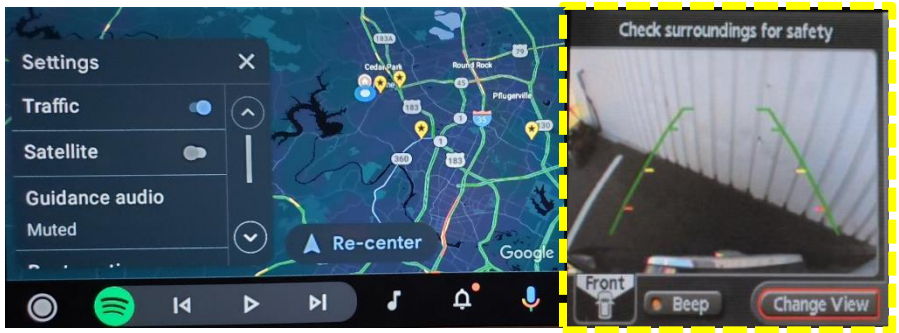




Blended by display controller (pipeline #1)

Blended by display controller (pipeline #2)

Instrument Cluster Display



Center Stack Display

i.MX95 objectives for low-mid eCockpit solution

Reduce system cost

Integrated real-time MCU

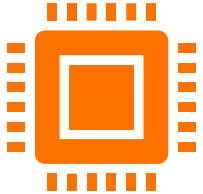
Comprehensive connectivity

Support adjacent use-cases e.g. parking assistant

Enable state-of-the-art Functional Safety solutions

Integrated ASIL-B FuSa island

SafeAssure software framework



Optimize performance and efficiency

Latest-generation multimedia cores

Scalable product families

Low-power modes for EV use-cases

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