HIGH-SPEED CABLES FOR PCIe 5.0 / 6.0 AND IEEE802.3ck: SIGNAL INTEGRITY CHALLENGES, PERFORMANCE PARAMETERS AND TEST AUTOMATION

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ROHDE&SCHWARZ

Make ideas real

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HIGH-SPEED CABLES FOR PCIe 5.0 / 6.0 AND IEEE802.3ck

SIGNAL INTEGRITY CHALLENGES, PERFORMANCE PARAMETERS AND TEST ASPECTS

DATA CENTER ECOSYSTEM: EVOLUTION OF KEY TECHNOLOGIES

PCIe: Processing, Storage

PCIe Spec.	Raw BW (per lane)	Modulation NRZ / PAM	Symbol Rate (per lane)
…			
PCIe 4.0: for 16.0 GT/s	16.0 Gbps	NRZ	16.0 GBd
PCIe 5.0 for 32.0 GT/s	32.0 Gbps	NRZ	32.0 GBd
PCIe 6.0 for 64 GT/s	64.0 Gbps	PAM4	32.0 GBd
PCIe 7.0 for 128 GT/s	…	…	…

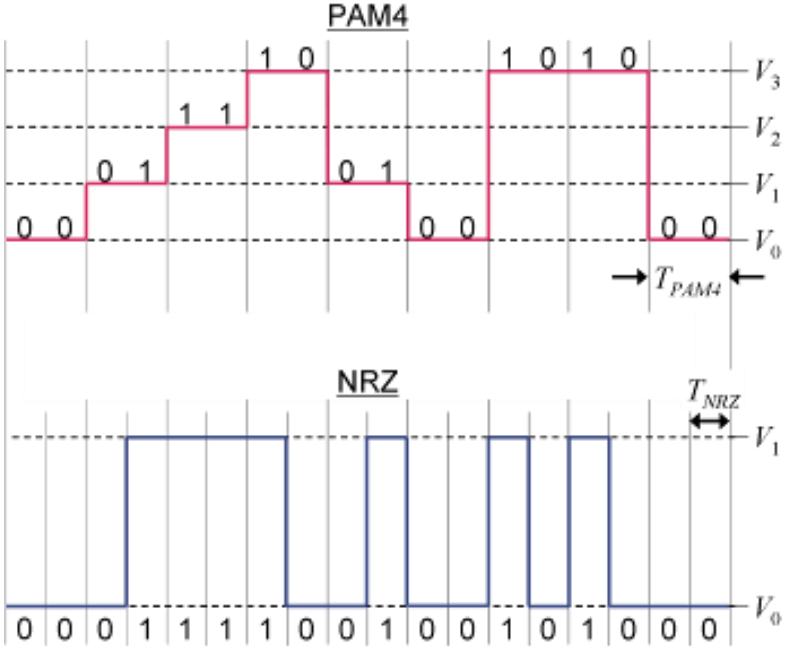
used cable formats: x1, x2, x4, x8, x16

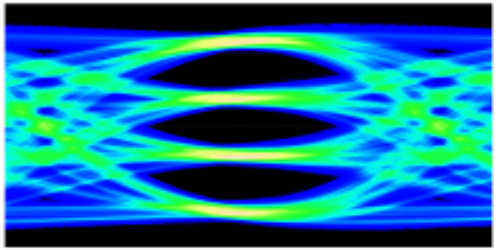
IEEE 802.3: Datacom

IEEE Spec.	Raw BW (per lane)	Modulation NRZ / PAM	Symbol Rate (per lane)
…	…		
802.3bj/by	25.78125 Gb/s	NRZ	25.78125 GBd
802.3cd	53.125 Gb/s	PAM4	26.5625 GBd
802.3ck	106.25 Gb/s	PAM4	53.125 GBd
802.3dj	…	…	…

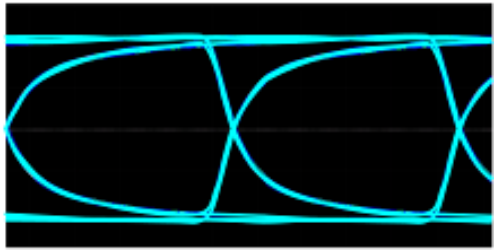
used cable formats: CR1, CR2, CR4, CR8, CR16

GENERAL SIGNAL INTEGRITY CHALLENGES: CROSSTALK IN SYSTEMS WITH PAM 4





$$BW_{PAM4} = ½\ BW_{NRZ}$$

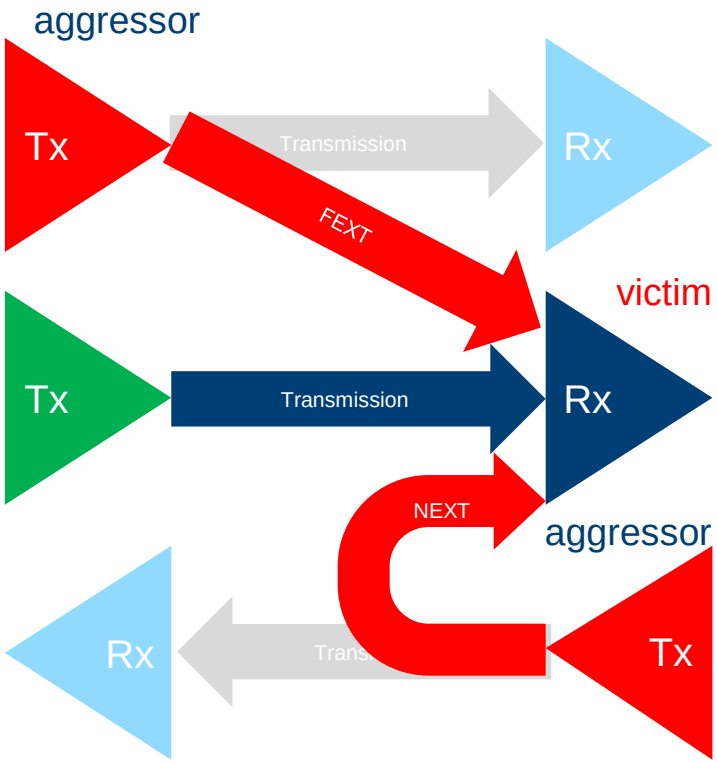


eye height for PAM4 is 1/3 of eye height for NRZ: 20 log (1/3) = -9.5 dB

→ higher sensitivity to noise and crosstalk

GENERAL SIGNAL INTEGRITY CHALLENGES: CROSSTALK

- crosstalk:
  - near end crosstalk: NEXT
  - far end crosstalk: FEXT
- multiple aggressors: power sum
  - power sum NEXT: PSNEXT or multi-disturber NEXT: MDNEXT
  - power sum FEXT: PSFEXT or multi-disturber FEXT: MDFEXT



TEST PARAMETERS IN PCIE 5.0 / 6.0
EXAMPLE: PCIe 5.0 / 6.0 INTERNAL AND EXTERNAL CABLES

Parameters according to PCIe Specification:

- Differential Insertion Loss (Sdd21): mask check against IL limit mask
- Differential Return Loss (Sdd11 and Sdd22): mask check against RL limit mask
  iRL metric: method of waiver, if RL violates limit mask
- NEXT and PSNEXT (power sum of individual NEXT aggressors): mask check against PSNEXT limit mask
  $ccICN_{NEXT}$ metric: method of waiver, if PSNEXT violates limit mask
- FEXT and PSFEXT (power sum of individual FEXT aggressors): mask check against PSFEXT limit mask
  $ccICN_{FEXT}$ metric: method of waiver, if PSFEXT violates limit mask
- Intra-Pair Skew EIPS (Effective Intra-Pair Skew): limit check
- Inter-Pair Skew (Lane-to-Lane Skew): limit check

Beyond Specification:

- Differential Trace Impedance Profile
- …

TEST PARAMETERS IN IEEE 802.3ck
EXAMPLE: 802.3ck COPPER CABLE ASSEMBLIES (CR)

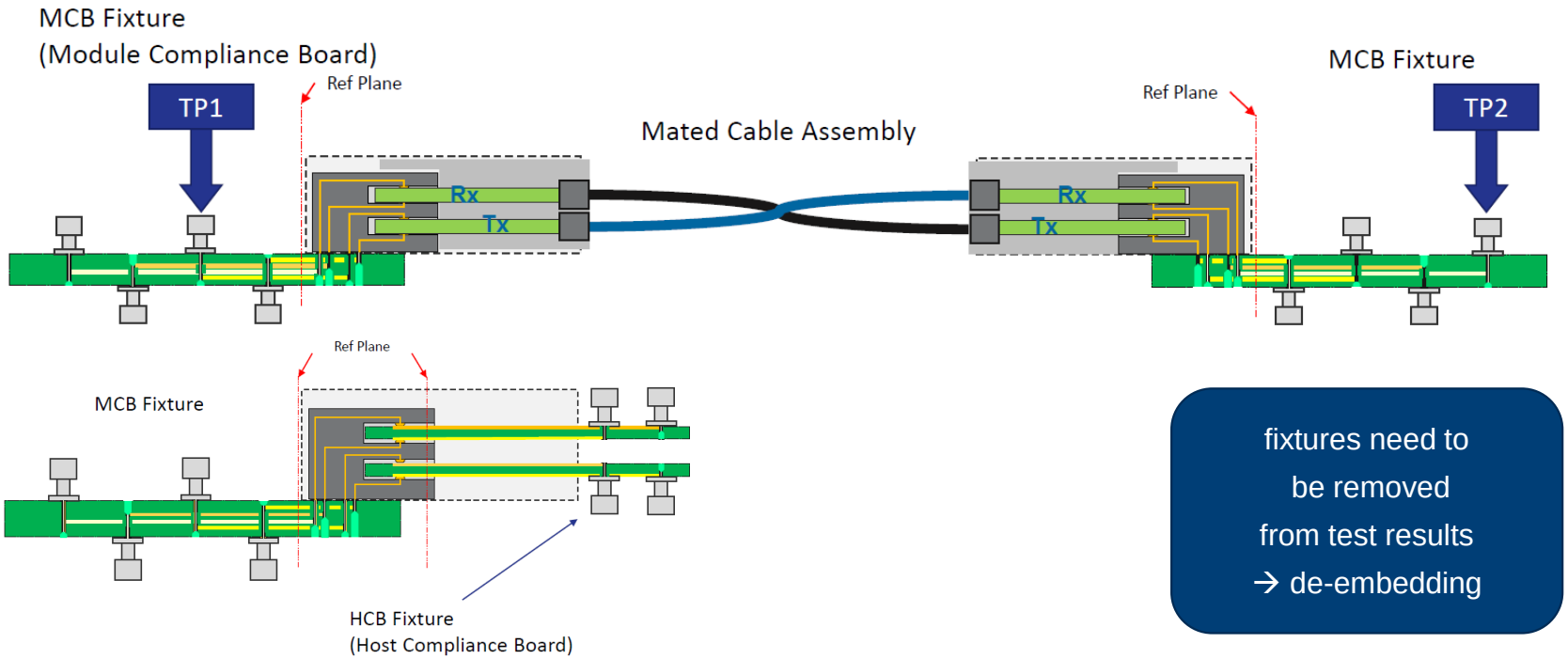
Parameters according to IEEE Specification:

- Differential Insertion Loss (Sdd21): mask check against ILdd limit mask
- Differential-Mode to Common-Mode Return Loss (Scd11 and Scd22): mask check against RLcd limit mask
- Differential-Mode to Common-Mode Insertion Loss (Scd21) minus Differential Insertion Loss (Sdd21): mask check against ILcd-ILdd limit mask
- Common-Mode to Common-Mode Return Loss (Scc11 and Scc22): mask check against RLcc limit mask
- Metrices:
  - Channel Operating Margin (COM)
  - for cable assemblies with COM < 4dB:
    Effective Return Loss (ERL)

Beyond Specification:

- Differential Trace Impedance Profile
- …

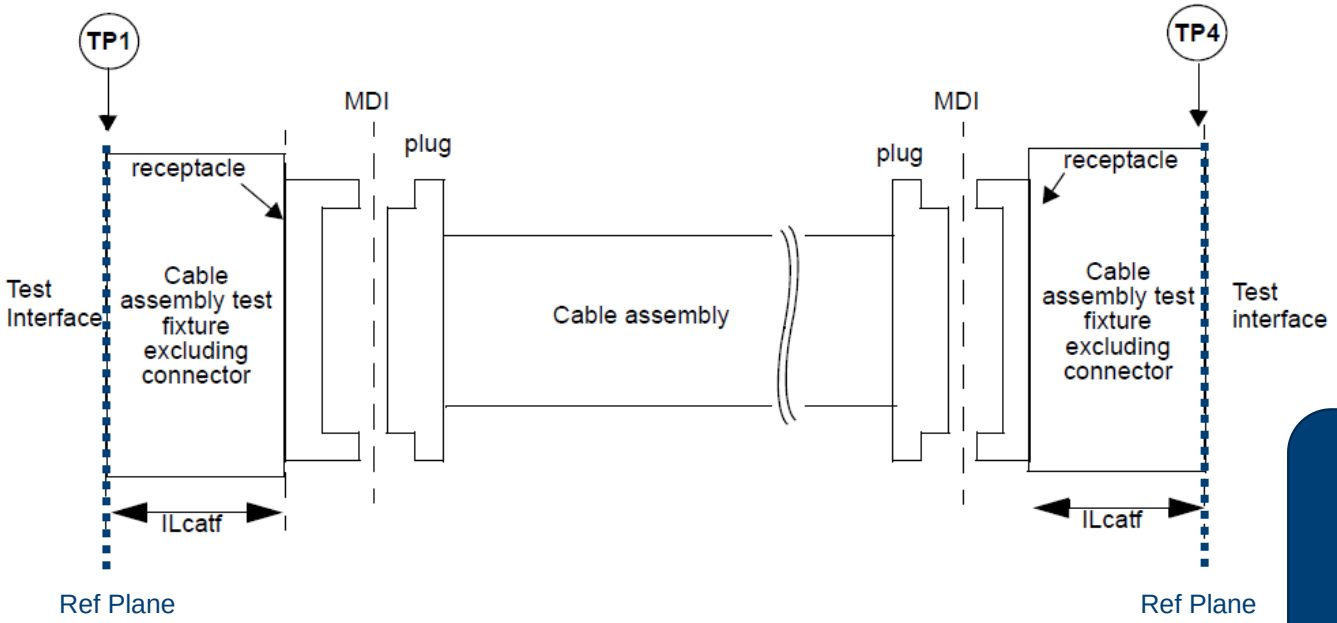
REFERENCE PLANE DEFINITION IN PCIe
EXAMPLE: PCIe 5.0 / 6.0 INTERNAL AND EXTERNAL CABLES



fixtures need to
be removed
from test results
→ de-embedding

Source: PCI-SIG Electrical Work Group (EWG): PCIe 5.0/6.0 External Cable Specification (in progress)

REFERENCE PLANE DEFINITION IN IEEE 802.3
EXAMPLE: 802.3ck COPPER CABLE ASSEMBLIES (CR)

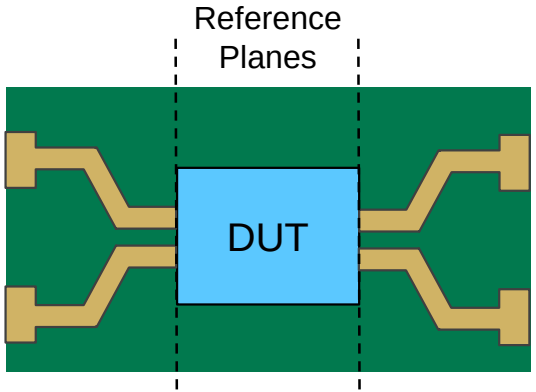


fixture are included
in test results
→ no de-embedding

Source: IEEE Std 802.3bj-2014

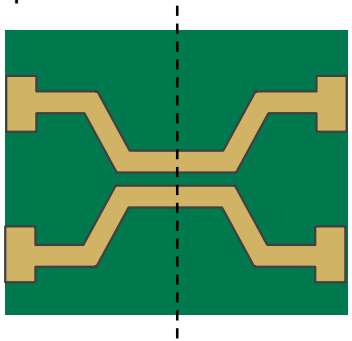
TEST FIXTURE CHARACTERIZATION AND DE-EMBEDDING HOW IT WORKS

Total Structure
Fixture – DUT – Fixture



with

2x-Thru Coupon
Replica of Lead-in / Lead-out



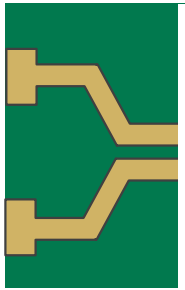
Traditional 2x-Thru de-embedding:
fixture models were only derived from 2x-Thru Coupon (replicas)

But:
replicas typically have different impedance profiles than actual lead-ins / lead-outs!

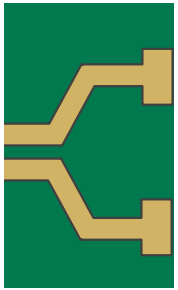
Therefore:
use modern de-embedding with impedance correction to avoid phantom limbs

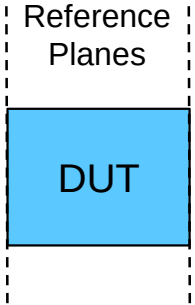
Tool

Fixture 1 Model:
Lead-in traces



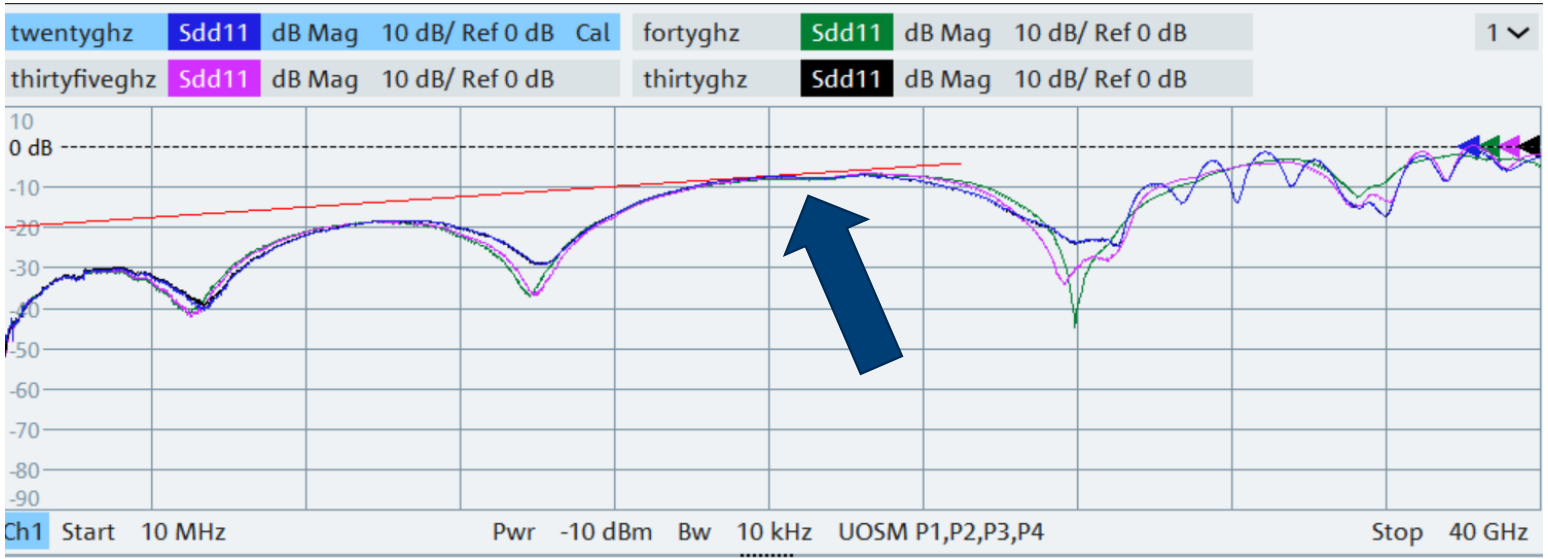
Fixture 2 Model:
Lead-out traces





TEST FIXTURE CHARACTERIZATION AND DE-EMBEDDING EXAMPLE: PCIE 5.0 CEM CONNECTOR FIXTURE

For best results: characterize fixture lead-ins / lead-outs up to 40 GHz



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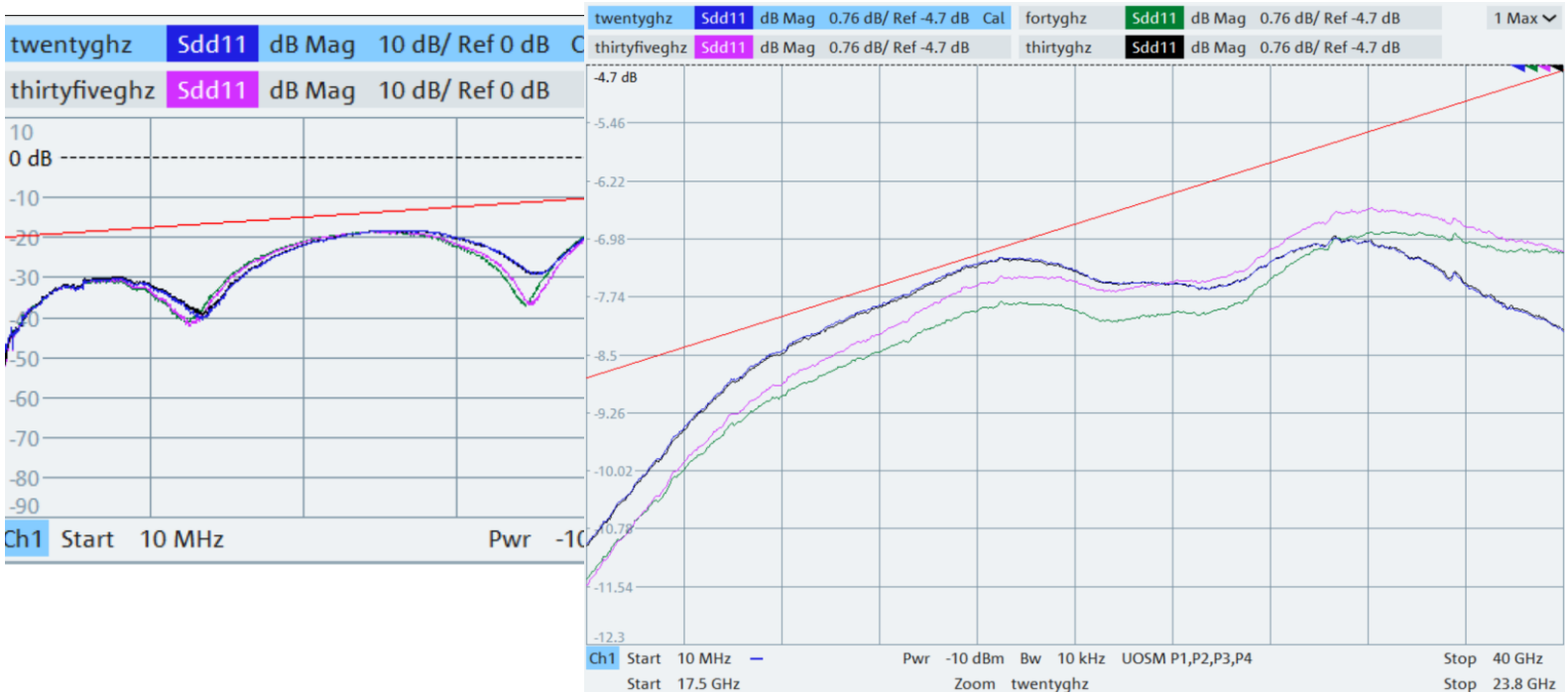
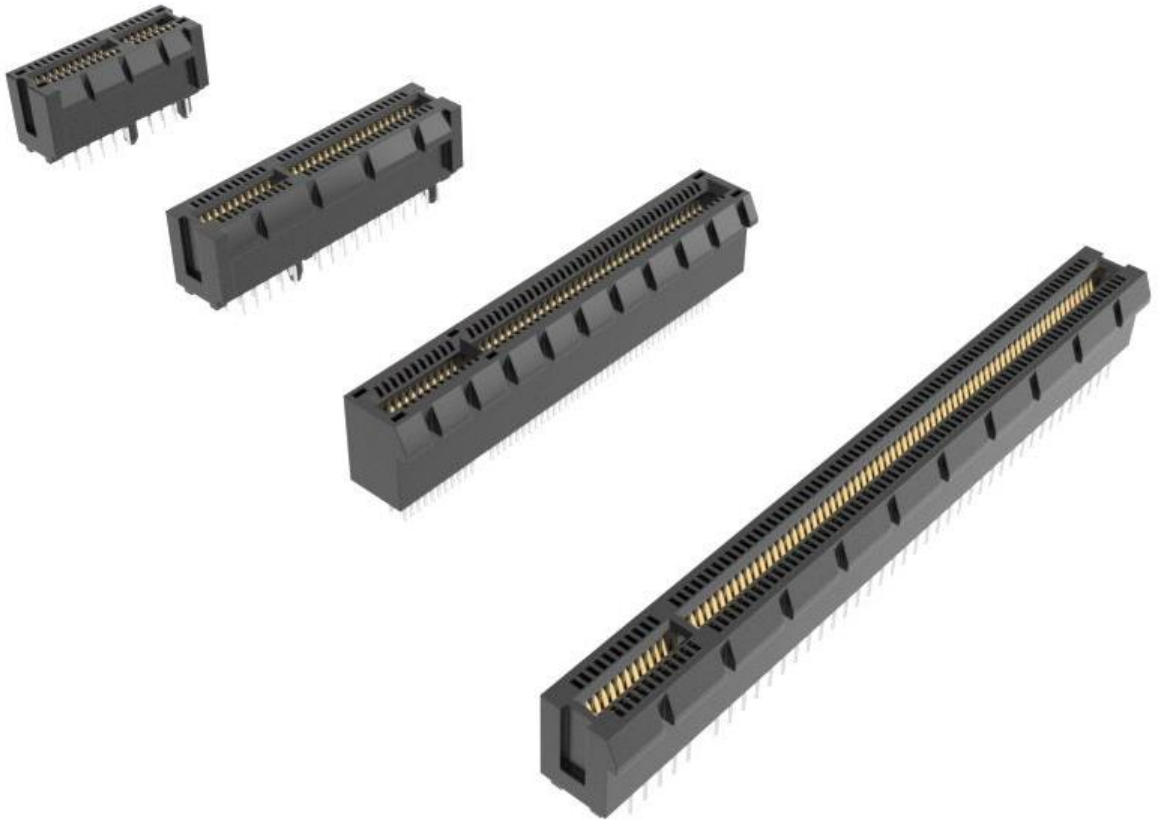


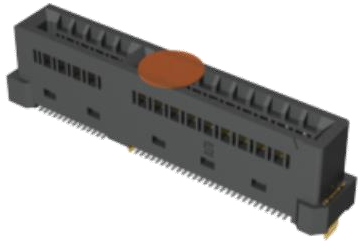
HIGH-SPEED CABLES FOR PCIe 5.0 / 6.0 AND IEEE802.3ck

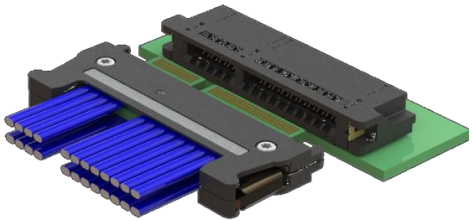
REQUIREMENTS AND IMPLEMENTATIONS



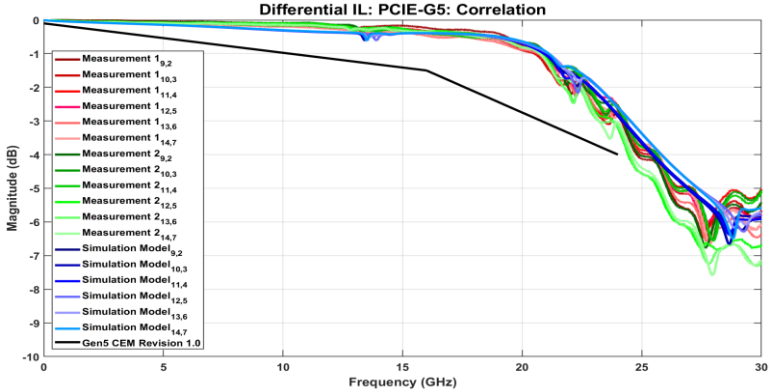
PCIE CONNECTOR AND CABLE PERFORMANCE: MAIN REQUIREMENTS

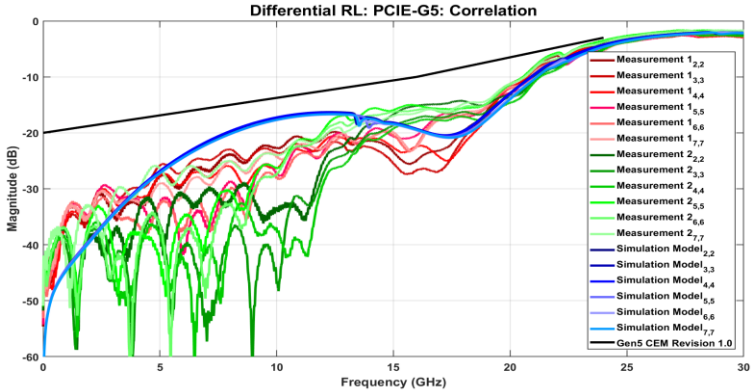
- PCIe 5.0 and 6.0 CEM Connector
  - FD IL, RL and Crosstalk limits
  - Excursions for crosstalk introduced with PCIe 5.0: ccICN (expected to be continued in PCIe 6.0)
  - Excursions for return loss expected to be introduced with PCIe 6.0: iRL (not released)
- PCIe 5.0 and 6.0 Cable Standard around SFF-TA-1016 (internal cables) and SFF-TA-1032 (external cables) is expected but not released
  - Separate requirements for mated cable assemblies and mated cable connectors
  - FD IL, RL and Crosstalk limits
  - Excursions for crosstalk (ccICN) and return loss (iRL)
  - Intra-Pair Skew

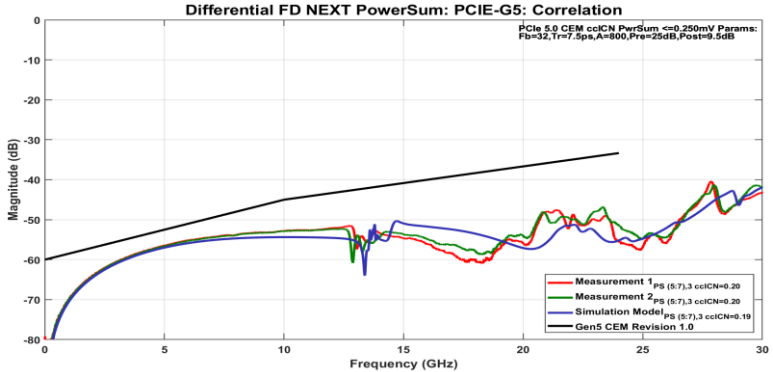




PCIe 5.0 FREQUENCY DOMAIN REQUIREMENTS: EXAMPLES







PCIe CEM 5.0 frequency limits and example measurements

TEST PARAMETERS IN PCIe 5.0 / 6.0
EXAMPLE: PCIe 5.0 / 6.0 INTERNAL AND EXTERNAL CABLES

Why excursions: introduction of iRL and ccICN

- connectors and cables may slightly exceed a frequency domain specification limit line
- slight excursions do not necessarily cause system failures as proven by simulation
- introduction of excursion metrices:
  - for return loss: iRL (integrated Return Loss)
    expected (unreleased specifications)
  - for crosstalk: ccICN (component contribution to Integrated Crosstalk Noise)
    expected (unreleased specifications)
    already introduced for PCIe 5.0 CEM (released)

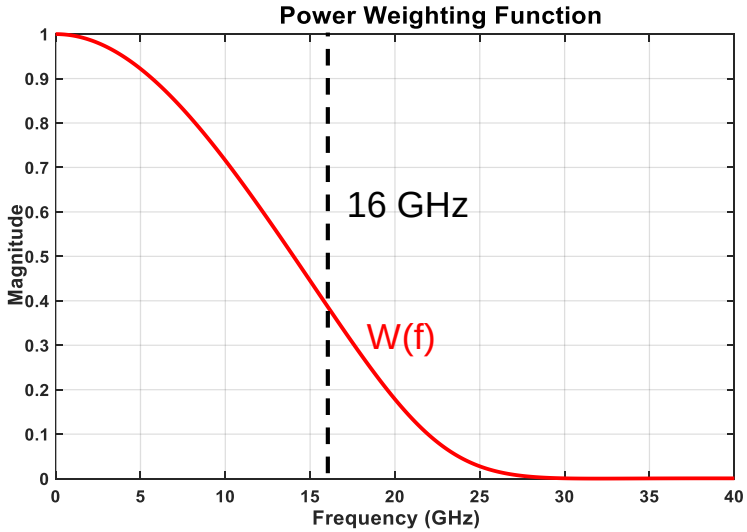
what excursions are more critical, what are less critical?
→ weighting according to power spectrum of PCIe signal

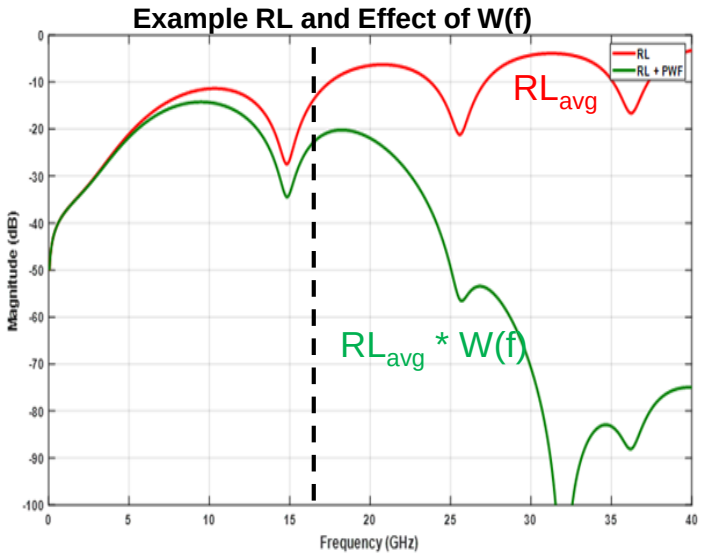
TEST PARAMETERS IN PCIe 5.0 / 6.0
EXAMPLE: PCIe 5.0 / 6.0 INTERNAL AND EXTERNAL CABLES

iRL (integrated Return Loss)

- Integration of averaged return loss after a power weighting filter W(f)
- W(f) represents transferred power for 16 GHz Nyquist signaling

$$iRL = dB\left(\sqrt{\frac{1}{N}\sum_{i=1}^{N} W(f_i)\, RL_{avg}^2(f_i)}\right)$$





$$W(f_i) = sinc^2(f_i/f_b)\left(\frac{1}{(1+(f_i/f_t)^4)}\right)\left(\frac{1}{(1+(f_i/f_r)^8)}\right)$$

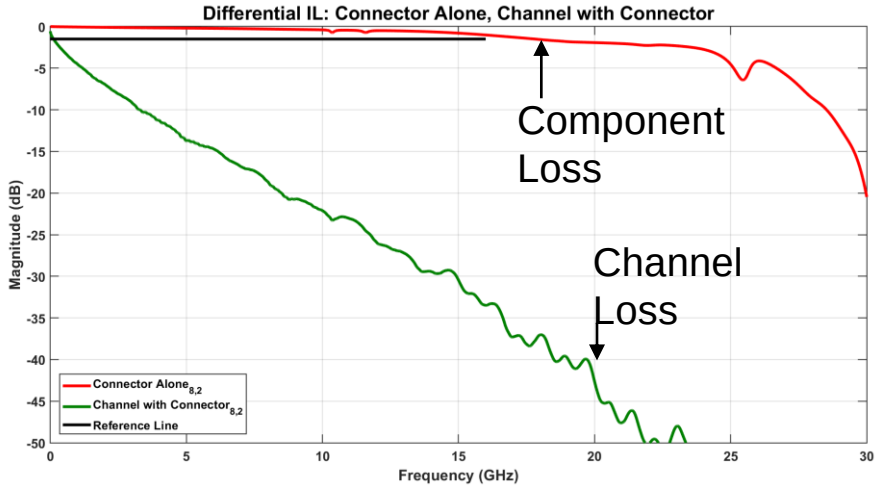
$$RL_{avg}(f_i) = (|RL_{11}(f_i)| + |RL_{22}(f_i)|)/2$$

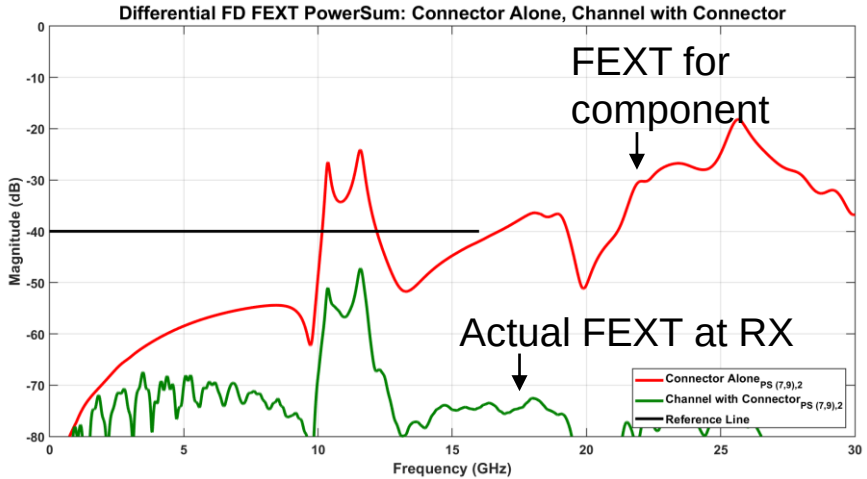
TEST PARAMETERS IN PCIe 5.0 / 6.0
EXAMPLE: PCIe 5.0 / 6.0 INTERNAL AND EXTERNAL CABLES

ccICN (component contribution to Integrated Crosstalk Noise)

- Similar to IRL, but also filters response by reference channel loss
  - FEXT and NEXT have different loss coefficients
  - FEXT is attenuated by end to end channel loss.
  - NEXT is much shorter (less attenuated)

$$\sigma_{ICN} = \sqrt{2 \cdot \Delta f \cdot \sum_{f_{min}}^{f_{max}} \frac{A^2}{f_b} \cdot PWF(f) \cdot 10^{\left(\frac{PwrSumXt}{10}\right)} \cdot 10^{\left(\frac{-2*Kxa*\frac{f}{f_b}}{10}\right)}}$$

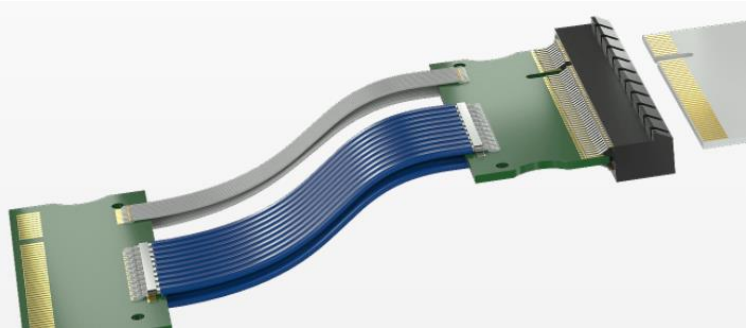




NON-STANDARD CONNECTORS AND CABLES

- SI requirements for CEM, SFF-TA-1016 and SFF-TA-1032 form factors may not apply to other form factors, such as:

CEM Extender Cables expect to have worse performance than e.g. the smaller SFF-TA-1016

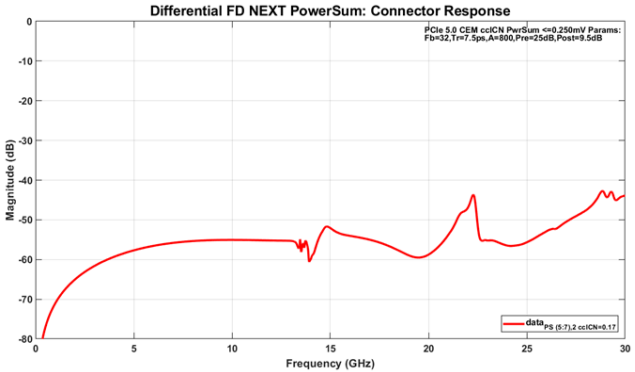


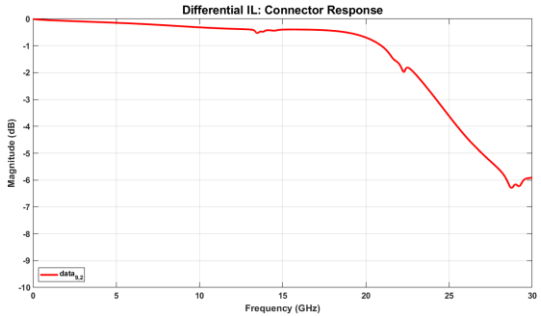
Array Connectors\Cables are more dense and can expect more crosstalk than SFF-TA-1016

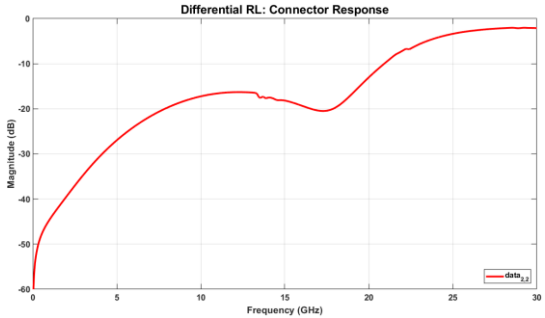
So, what can we do?

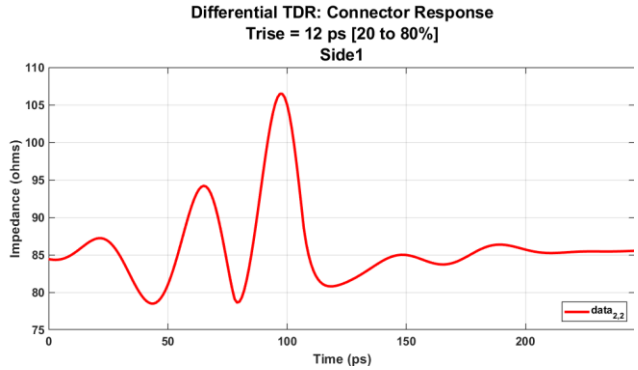
STEP 1: FREQUENCY DOMAIN CONSIDERATION

- Other form factors are taller:
  having more loss and lower resonances,
  with more pins and noise
- Anecdotal recommendations:
  - “Rule of Thumb”









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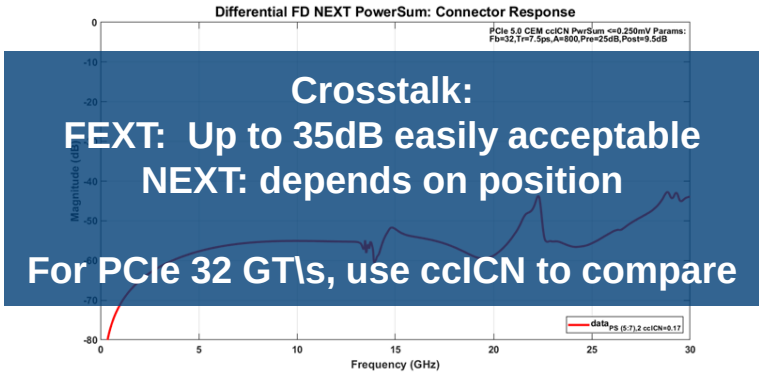
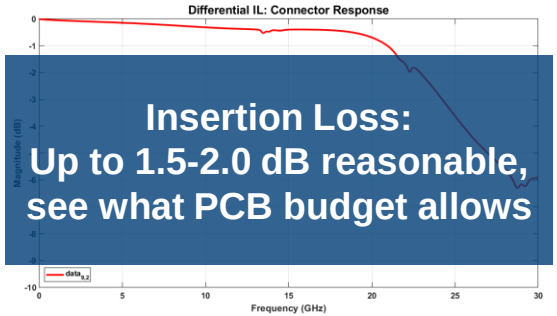
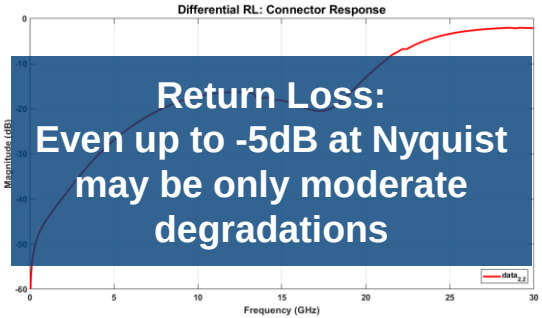


Crosstalk:
FEXT: Up to 35dB easily acceptable
NEXT: depends on position

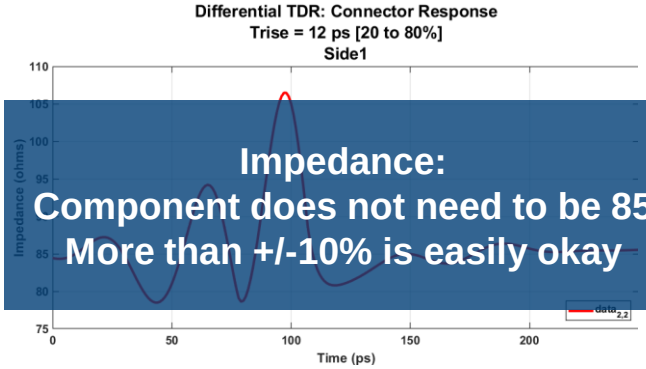
For PCIe 32 GT\s, use ccICN to compare



Insertion Loss:
Up to 1.5-2.0 dB reasonable, see what PCB budget allows



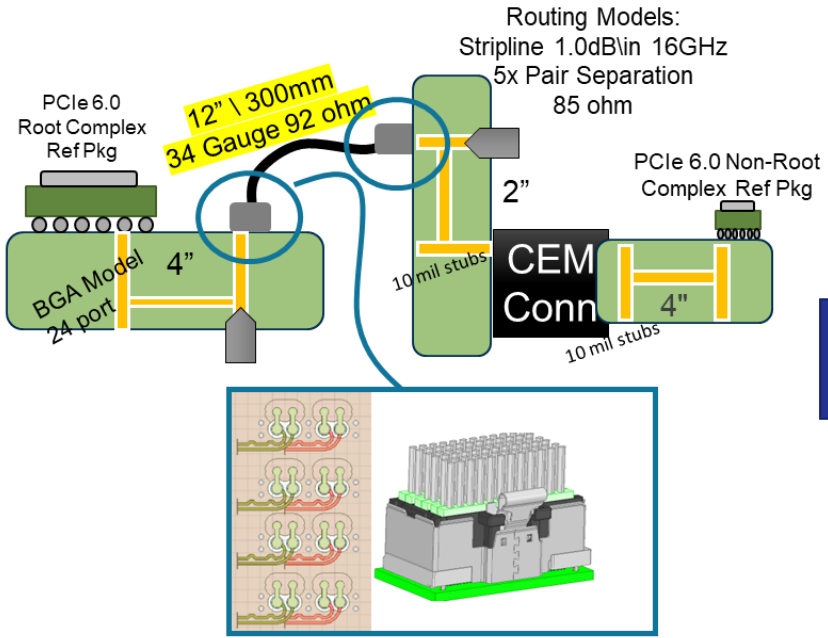
Return Loss:
Even up to -5dB at Nyquist may be only moderate degradations

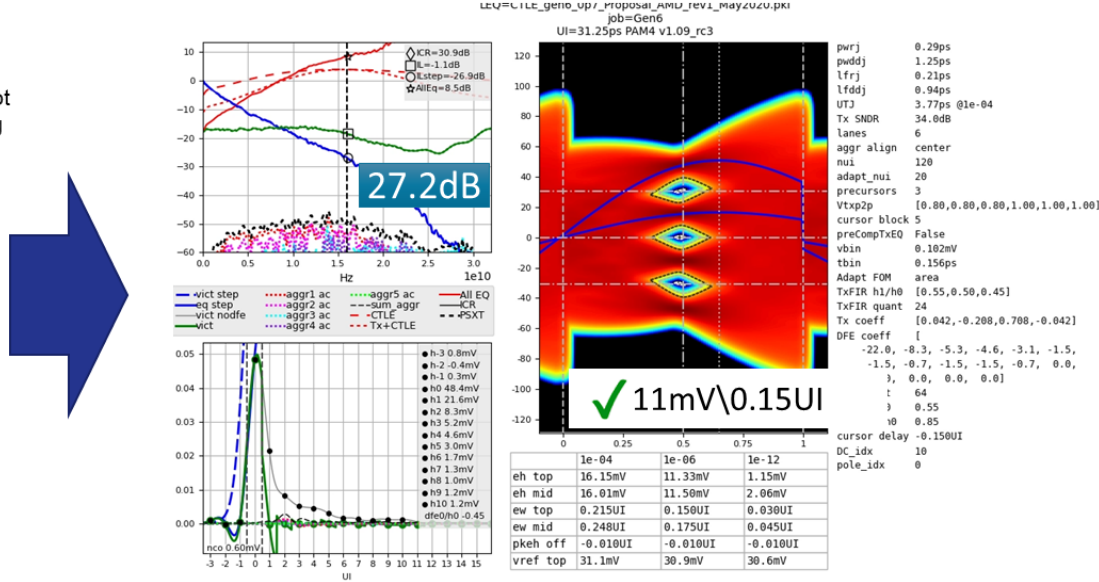


Impedance:
Component does not need to be 85
More than +/-10% is easily okay

STEP 2: CHANNEL SIMULATION
EXAMPLE PCIe 6.0 CABLED TOPOLOGY

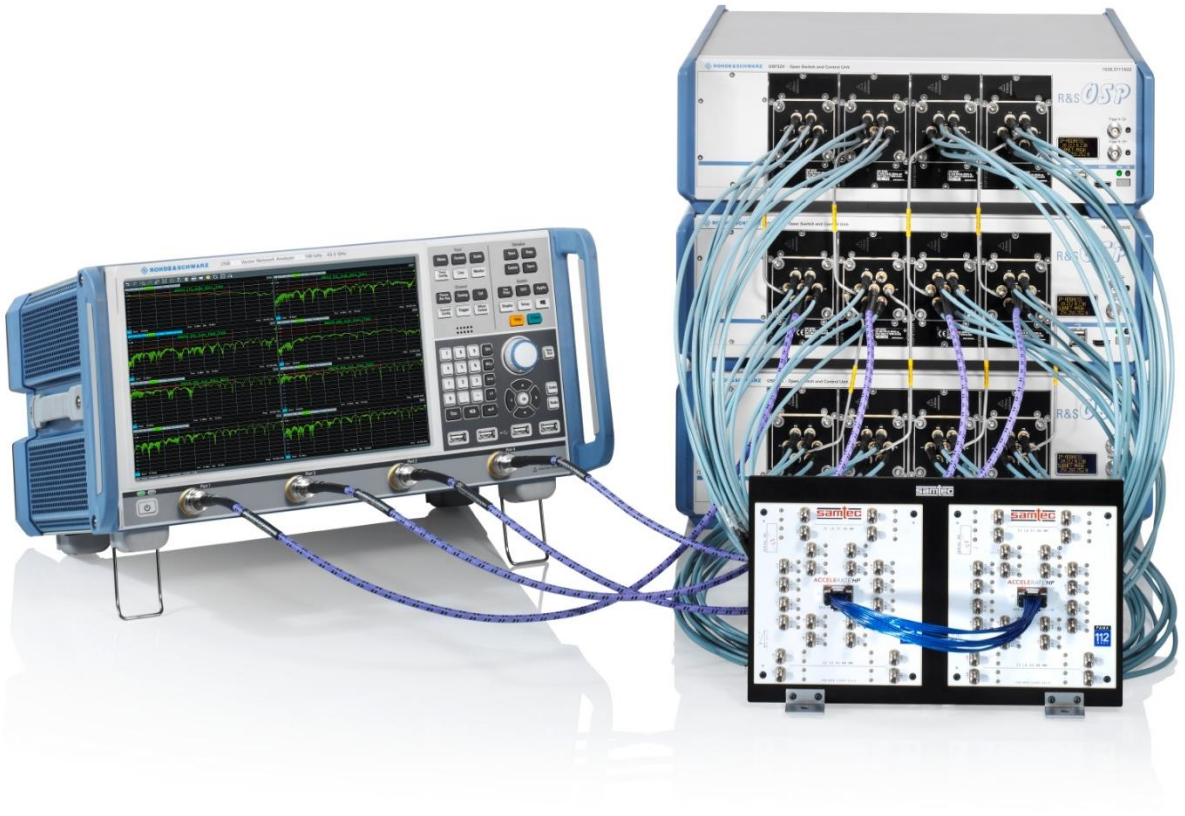
- Why simulation?
  - Non-Interoperable captive systems, impedances other than 85, specific application models





HIGH-SPEED CABLES FOR PCIe 5.0 / 6.0 AND IEEE802.3ck

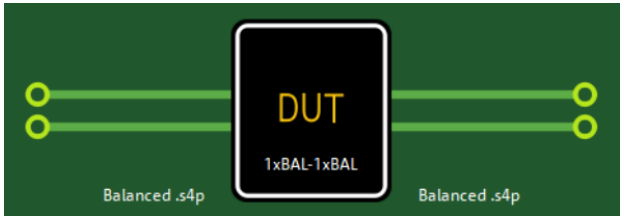
TEST SOLUTIONS: FIXTURE REMOVAL, TEST AUTOMATION



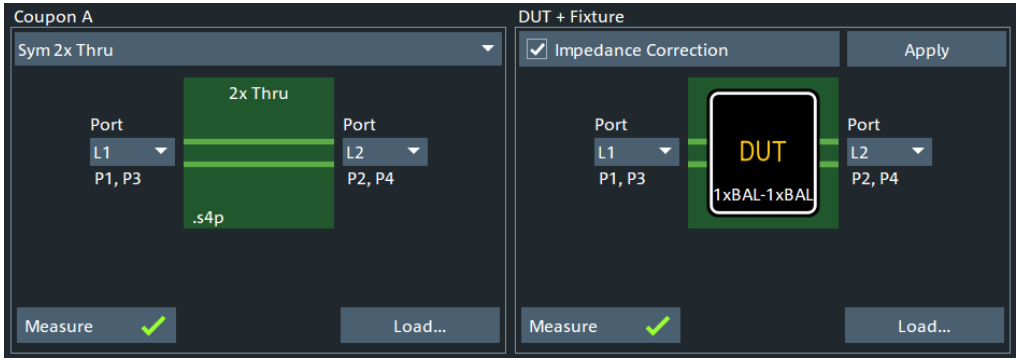
TEST FIXTURE CHARACTERIZATION

R&S DE-EMBEDDING ASSISTANT

Step 1: Topology
- DUT
- Lead-in
- Lead-out



Step 2: Measure/Load
- Coupon(s)
- Total structure



Step 3: Result
- Apply

- Industry accepted modeling algorithms
  - K210 EZD: Eazy De-embedding
  - K220 ISD: In-Situ De-embedding
  - K230 SFD: Smart Fixture De-embedding

Method	Offset	TRL	Fixture Model De-embed
Correction (kit)	Easy	Complex	Easy
Speed	Fast	Slow	Fast
Accuracy	Poor	Moderate	Best

TEST OF SAMTEC SI-FLY FLYOVER EVALUATION KIT

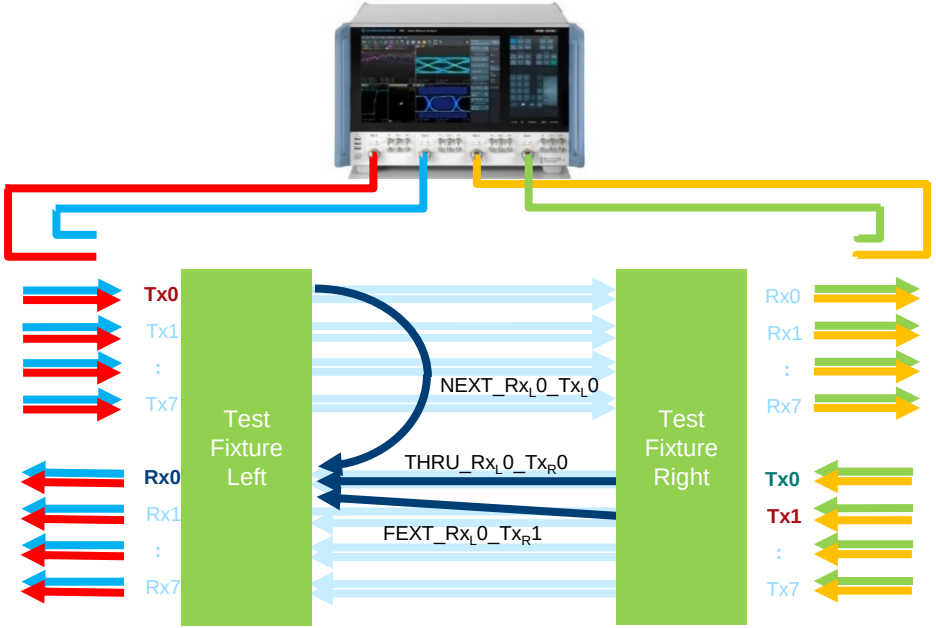
RETURN LOSS, INSERTION LOSS, AND TDR COMPARISON

VERIFICATION OF PCIE 5.0, 6.0 CABLES AND CONNECTORS WITH VECTOR NETWORK ANALYZER

- **Required measurements:**
  - Insertion loss Sdd21
  - Return loss Sdd11 and Sdd22
  - Near-end crosstalk (NEXT)
  - Far-end crosstalk (FEXT)

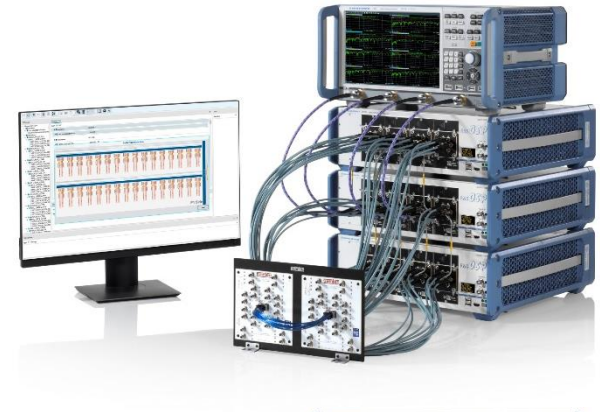
- **Testing with 4 port VNA**
  - multiple 4-port measurements

- **Postprocessing:**
  - Integrated return loss iRL
  - Power sum MDNEXT and $ccICN_{NEXT}$
  - Power sum MDFEXT and $ccICN_{FEXT}$
  - Intra-pair skew: EIPS
  - Inter-pair skew (lane-to-lane)



Example PCIe x8 cable

HIGH SPEED INTERFACE TESTING SOLUTION



32-port (4 lanes)

64-port (8 lanes)

ZNrun Option	ZNrun-K410	ZNrun-K411	ZNrun-K440
DUT example	SFP28 QSFP28 SFP56 QSFP56	SFP112 QSFP112 QSFP-DD112 OSFP	GenZ MCIO Riser CEM CDFP
Technology	IEEE802.3bj/by/cd	IEEE802.3ck	PCIe 5.0/6.0
Recommended VNA Frequency	26.5 GHz	50 GHz	43.5 GHz
Fixture de-embedding	Optional	Optional	Mandatory
SI test items	ERL COM	ERL COM	iRL ccICN EIPS

AUTOMATED VERIFICATION WITH VNA AND MULTIPORT SWITCH MATRIX

Setup | Calibrate | Measure

- Solution: R&S ZNrun cable test client, VNA, and OSP
  - Predefined topology for multi-lane setup
  - Test plan of PCIe and IEEE802.3
  - Flexible de-embedding
  - Test cases selection
  - Efficient calibration
  - Report generation
  - Data export
  - Automation interfaces

DE-/EMBEDDING

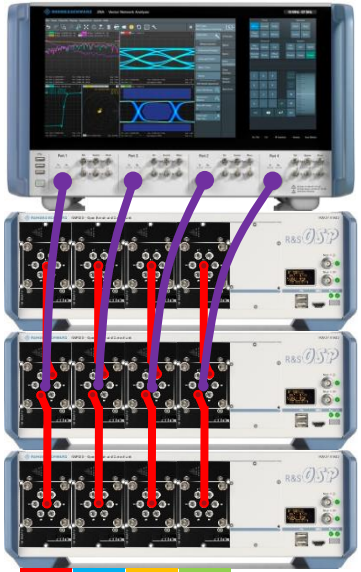
Port	Usage	Touchstone File	Interchange Mode
Fixture left	Deembedding		Standard
Fixture right	Deembedding		Standard

Test Case Selection

RX Lane	Test Case	Execute	TX Lanes
0	THRU / SKEW / TDR		0
	NEXT		0,1,2
	FEXT		1,2
1	THRU / SKEW / TDR		1
	NEXT		0,1,2
	FEXT		0,2
2	THRU / SKEW / TDR		2
	NEXT		0,1,2
	FEXT		0,1
	Calculate psNEXT (L)		
	Calculate psNEXT (R)		
	Calculate psFEXT (L)		

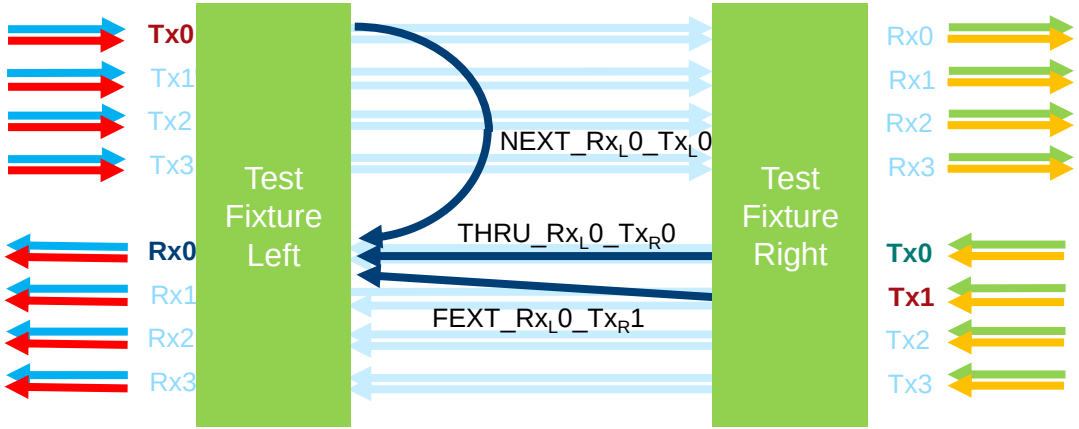
VERIFICATION OF PCIE 5.0 / 6.0 CABLES AND CONNECTORS: GENERAL CONSIDERATIONS

Measurements:
automation with switch matrix:
example for PCIe x8



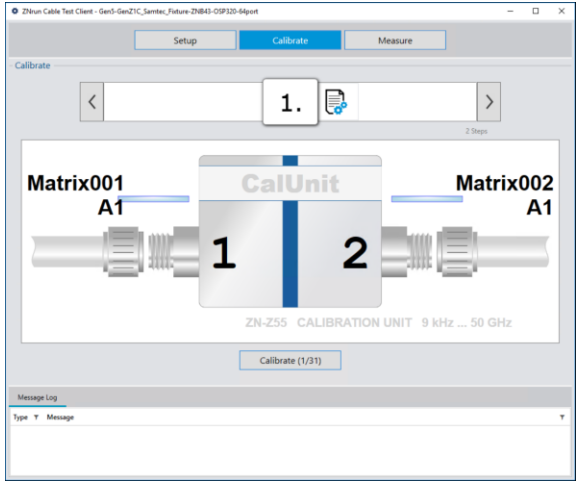
total = 64 ports

	PCIe x4	PCIe x8	PCIe x16
number of lanes (Tx + Rx)	4 Tx + 4 Rx	8 Tx + 8 Rx	16 Tx + 16 Rx
number of ports for full testing (all lanes and all crosstalk combinations)	32	64	128
number of 4-port measurements for full testing (all lanes and all crosstalk combinations)	8 x THRU 4 x 4 = 16 x NEXT_L 4 x 4 = 16 x NEXT_R 3 x 4 = 12 x FEXT_L 3 x 4 = 12 x FEXT_R total: 64 4-port meas.	16 x THRU 8 x 8 = 64 x NEXT_L 8 x 8 = 64 x NEXT_R 7 x 8 = 56 x FEXT_L 7 x 8 = 56 x FEXT_R total: 256 4-port meas.	32 x THRU 16 x 16 = 256 x NEXT_L 16 x 16 = 256 x NEXT_R 15 x 16 = 240 x FEXT_L 15 x 16 = 240 x FEXT_R total: 1024 4-port meas.

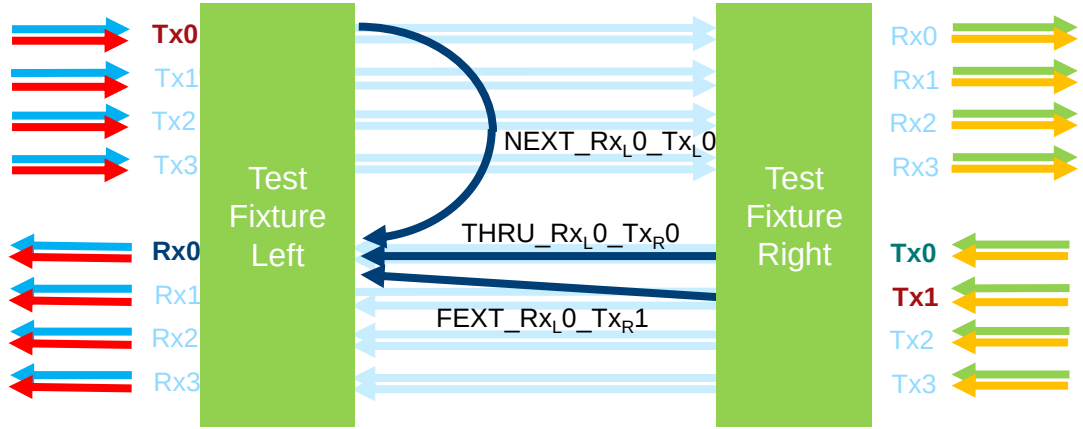


VERIFICATION OF PCIE 5.0 / 6.0 CABLES AND CONNECTORS: GENERAL CONSIDERATIONS

Calibration:
automation of calibration
example for PCIe x4 w. R&S ZNrun

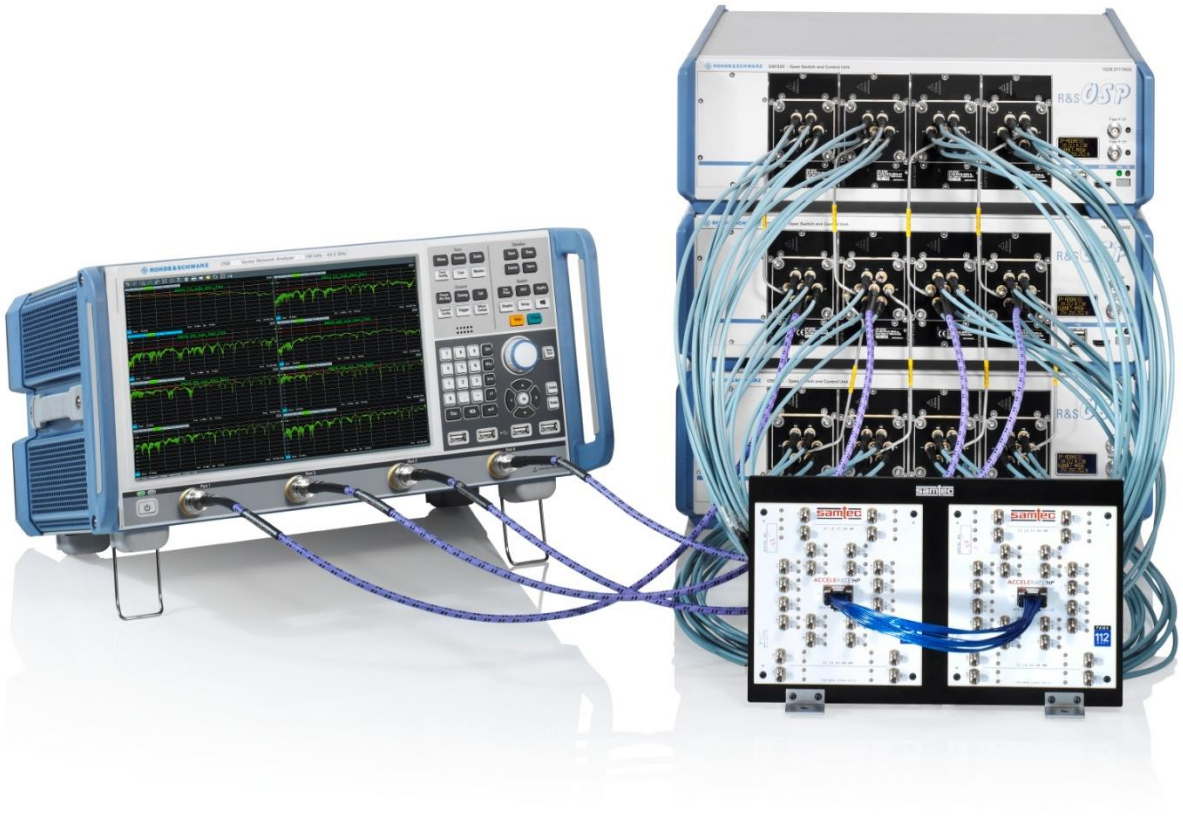


	PCIe x4	PCIe x8	PCIe x16
number of lanes (Tx + Rx)	4 Tx + 4 Rx	8 Tx + 8 Rx	16 Tx + 16 Rx
number of ports for full testing (all lanes and all crosstalk combinations)	32	64	128
number of 4-port measurements for full testing (all lanes and all crosstalk combinations)	64 4-port groups:	256 4-port groups:	1024 4-port groups:
standard calibration (3 connections per 4-port)	64 x 3 = 192	256 x 3 = 768	1024 x 3 = 3072
optimized calibration	**31**	**63**	**127**



HIGH-SPEED CABLES FOR PCIe 5.0 / 6.0 AND IEEE802.3ck

PRACTICAL DEMO



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Thank you!

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