

Aerospace and Defense Testing

DECEPTIVE JAMMER AND DRFM TESTING

VERSION 2.0

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ROHDE & SCHWARZ

Make ideas real



All Information was derived from publicly available sources

Us DoD Classification:

Distribution A - Approved for public release: Distribution is unlimited



Webinar Link: Deceptive Jammer / DRFM testing, Version 1.0



AGENDA

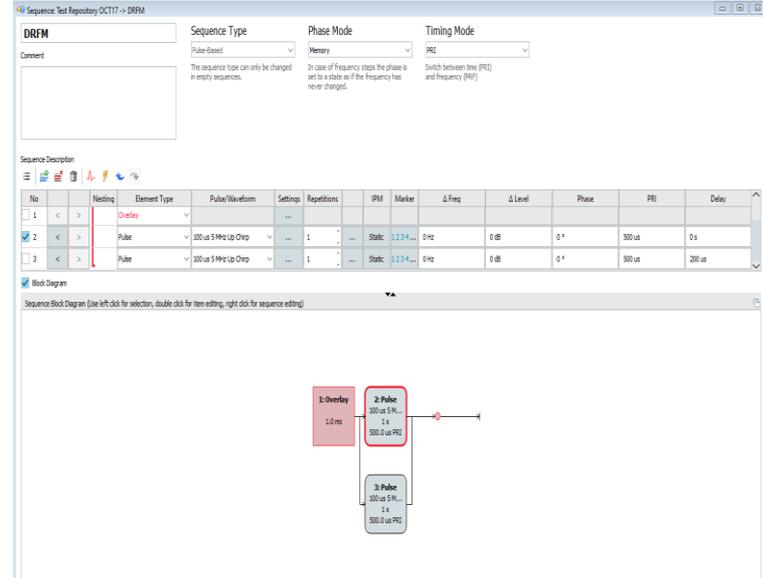
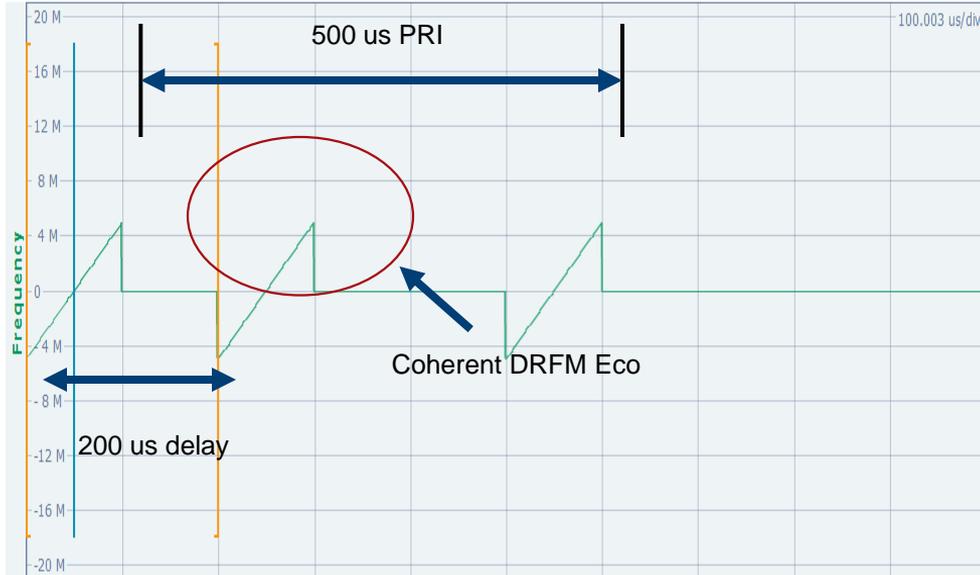
- ▶ DRFM Overview
- ▶ DRFM Test Requirements
 - System Level
 - RF/IF Subsystems
 - Digital Subsystems
- ▶ Conclusion
- ▶ Appendix A – Fair use statement



DRFM HISTORY

Earliest references to Digital RF Memory appear in an AOC article in 1975 by Sheldon C. Spector, entitled "A Coherent Microwave Memory Using Digital Storage: The Loopless Memory Loop".

Principles of DRFM



DRFM OVERVIEW

- ▶ DRFM Jammers are an essential technology for Electronic Attack
- ▶ Key figure of merit is RF latency (RF in to RF out)
 - Usually in the ns range
- ▶ Wideband (>2 GHz) technology and low SWAP characteristics
- ▶ DRFM is often deployed as a towed decoy
- ▶ Leonardo BriteCloud™ is an attritable DRFM launched from a chaff/flare dispenser
- ▶ Flexible techniques generator capable of:
 - Coherent range and velocity Pull-Off/In
 - False Doppler and range targets
 - Coherent noise
 - CW jamming
 - Inverse gain techniques

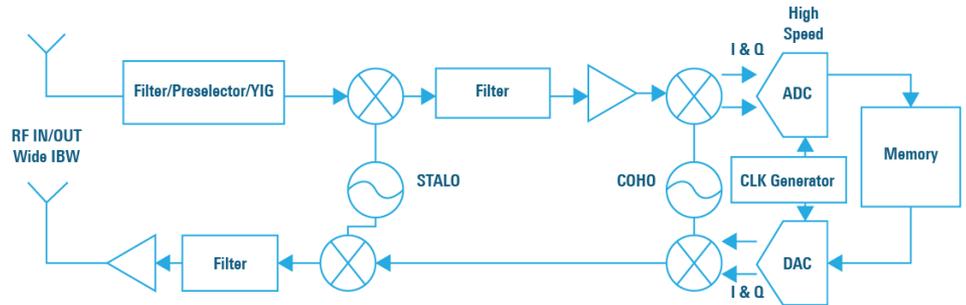


LEONARDO

DRFM TECHNOLOGY

BASIC DRFM BLOCK DIAGRAM

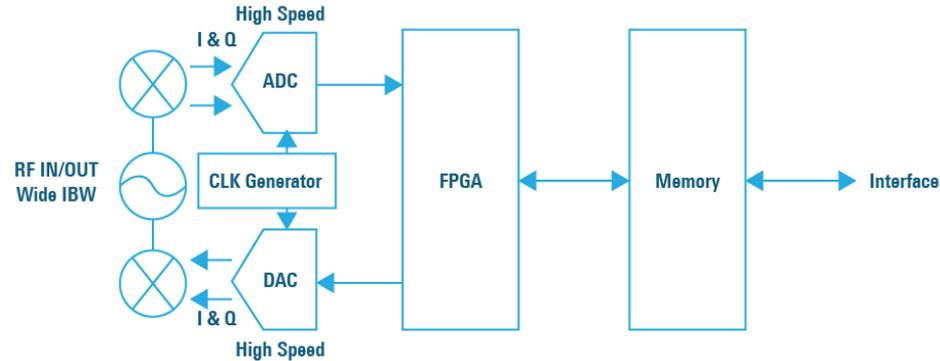
- ▶ DRFM digitizes incoming radar signal, classifies the emitters, delays the signal and then retransmits that radar signal
- ▶ Coherency ensures victim radar cannot distinguish DRFM transmission from legitimate returns
- ▶ Storage allows for
 - False targets behind the intended target - Reactive Jamming
 - False targets ahead of the intended target - Predictive Jamming
- ▶ Variations in frequency and amplitude of the transmitted signal can be used to create Doppler and range errors and manipulate velocity and range gating on the victim radar



DRFM TECHNOLOGY

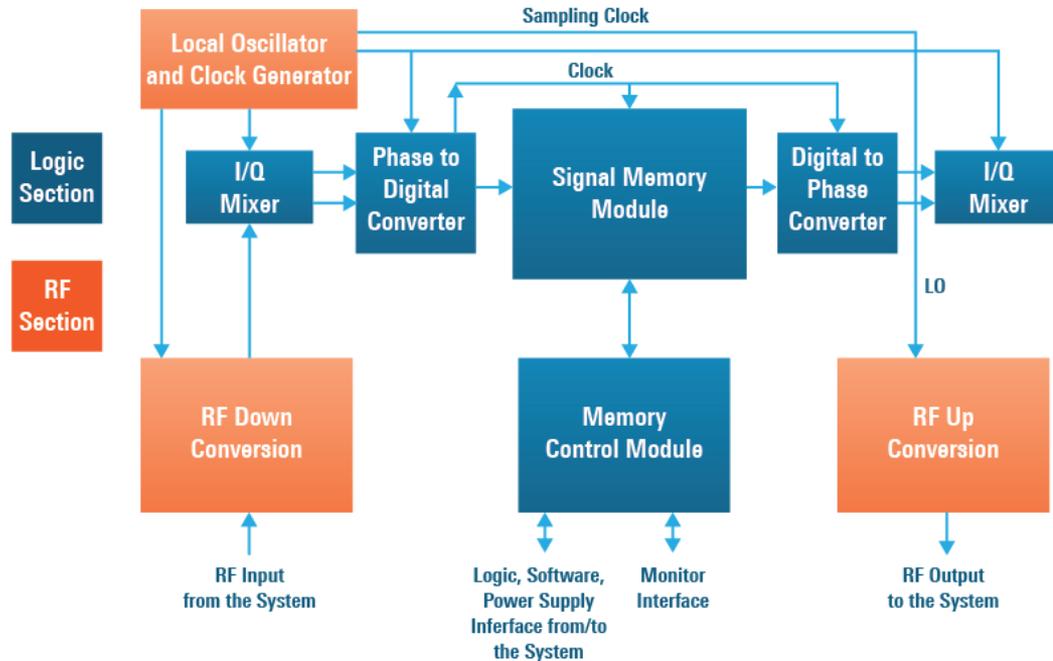
MODERN DRFM JAMMERS

- ▶ Modern DRFM Jammers make extensive use of:
 - FPGAs
 - High Speed, low latency ADCs and DACs for wideband operation
 - Wideband RF Front Ends
 - Digital Instantaneous Frequency Measurement - DIFM
 - Phase correction
- ▶ Receiver Architectures
 - IFM - instantaneous frequency measurement
 - CVR (crystal video receiver)
 - Digital Channelized Rx
 - ...



DRFM TECHNOLOGY

MODERN DRFM JAMMERS – EXAMPLE HENSOLDT



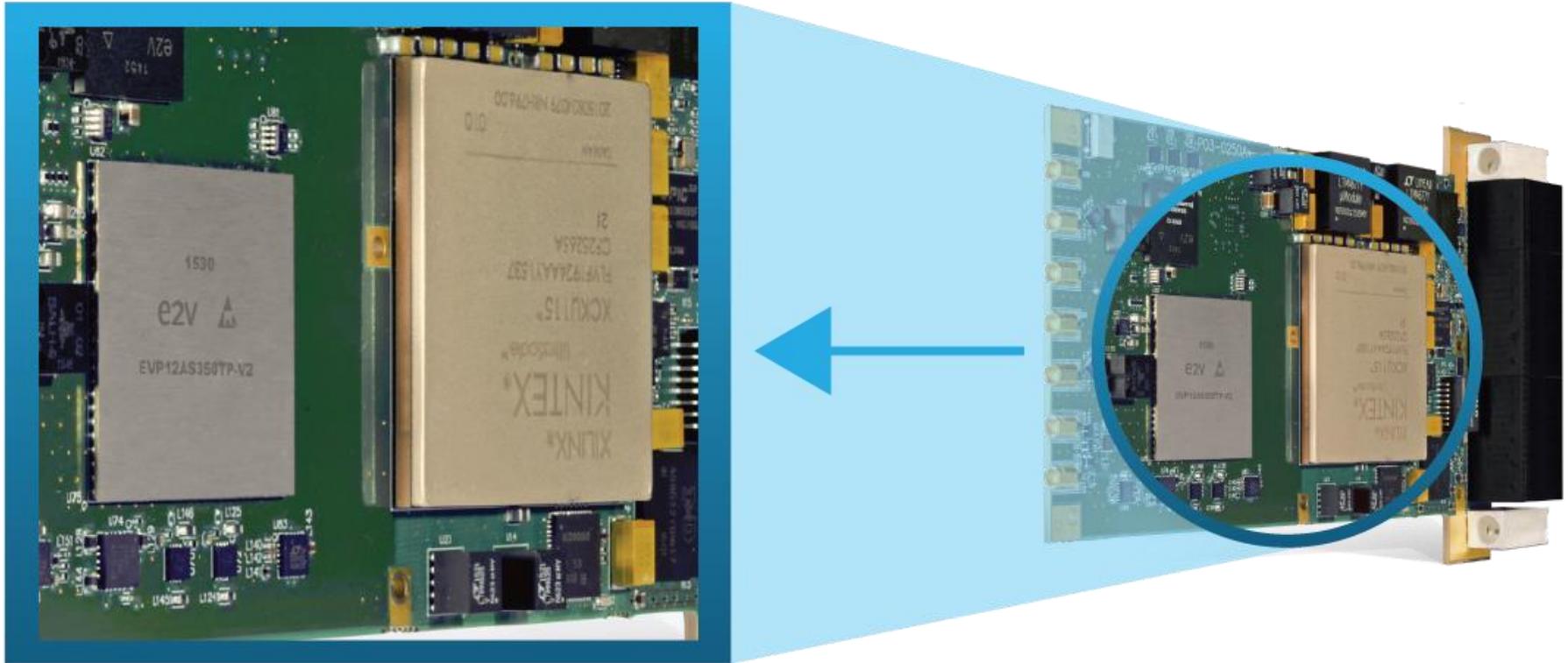
Standard ECM Functions

- Coherent range and velocity Pull-Off/In
- Velocity gate Pull-Off/In
- Fixed false Doppler and range targets
- Random false Doppler and range targets
- Phase modulation
- Multi-frequency false targets
- Narrow and wideband coherent noise
- Narrow and wideband non-coherent noise
- Swept spot noise
- Multi-frequency noise
- CW jamming
- Frequency offset jamming, coherent and non-coherent
- Inverse amplitude techniques (with amplitude quantisation)
- Target scintillation
- Due to the programmability, other „custom-made“ ECM functions can be installed. A combination of ECM techniques is possible.

Characteristics and Performances

- Extremely wide band, single board DRFM
- Freely configurable integrated techniques generator
- Multi-threat capability
- Coherent and non-coherent ECM techniques
- Extremely fast digital signal detection
- Instantaneous bandwidth: up to 2,3 GHz
- Quantisation: up to 10 Bit amplitude
- Frequency accuracy: extremely accurate
- Volume: 3 litres
- Power consumption: 50 Watt

DRFM TECHNOLOGY



Source – Apisys, AV133 DRFM Module, <https://www.aes-eu.com/datasheets/apisys/AV133-datasheet.pdf>

DRFM MODULE SPECIFICATIONS

Specifications

Analog Input/Output

- Coupling: AC
- Input bandwidth: > 5.5 GHz
- Input Full scale : 8.5 dBm
- Output bandwidth: > 6 GHz
- Output Full scale : -3.5 dBm (NRZ)
- Impedance: 50 Ohm
- Connectors: SMPM

Analog-Digital Conversion

- One channel, $F_s \leq 5.4$ GHz
- Resolution: 12 bit
- Analog Performances @1 GHz, -1dBFS
 - SNR: 53 dBFS
 - SFDR: 56 dBc
 - ENOB: 8.5 bit

Digital-Analog Conversion

- One channel, $F_s \leq 5.4$ GHz
- Resolution: 12 bit
- Analog Performances @1 GHz, 0dBFS
 - SFDR: 59 dBc, NRTZ mode
- Analog Performances @3 GHz, 0dBFS
 - SFDR: 55 dBc, NRTZ mode

Clock

- Internal:
 - 1 GHz to 6 GHz low jitter clock
- External Input Clock:
 - Frequency: 2 GHz to 5.4 GHz
 - Input level: 10dBm recommended
 - Connector : SMPM 50 Ohm and VPX P2
- External reference:
 - Frequency: 10 MHz to 100 MHz
 - Connector: SMPM, 50 Ohm and VPX P2

Trigger

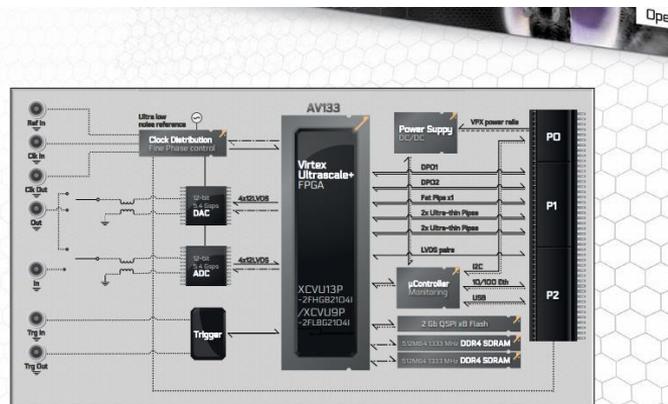
- External: 0 to 2 Vp
- Connectors: SMPM, 50 Ohm:

FPGA

- FPGA: Xilinx Virtex Ultrascale+
 - XCVCU13P-2FHGB2104I
 - XCVCU9P-2FLBG2104I

Memory

- Two banks 512G64 DDR4 SDRAM, 1333 MHz clock



- Support up to two banks 1G64 DDR4 SDRAM
- One 2 Gbit QSPI FLASH memory

VPX interface

- P1:
 - Data plane: two fat pipes
 - Expansion plane: one fat pipe
 - Control plane: 2 ultra-thin pipes
 - 2 user-defined ultra-thin pipes
- P2:
 - USB2.0 and 10/100 Ethernet
 - 18 LVDS differential pairs, configurable as 36 LVCMOS

Software support

- Software Drivers:
 - Windows 10 64 bits
 - Linux 64 bits
- Application example: Windows and Linux

Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx VIVADO 2019.2

Ruggedization

- As per VITA 47:
 - Air cooled : EAC4 and EAC6
 - Conduction cooled : ECC3 and ECC4

Power dissipation

- +12V: 9.7 A max (116W)
- +5V: 2.4 A max (12W)
- +3.3V: 2.0 A max (6.5W)
- +3.3VAUX: 0.6 A max (2.0W)

Weight

- Air cooled : 550g
- Conduction cooled : 650g

DRFM TEST REQUIREMENTS

R&S NRPxx



Test Systems
DF, Phase Coherent
Signals

R&S FSW



R&S FSWP

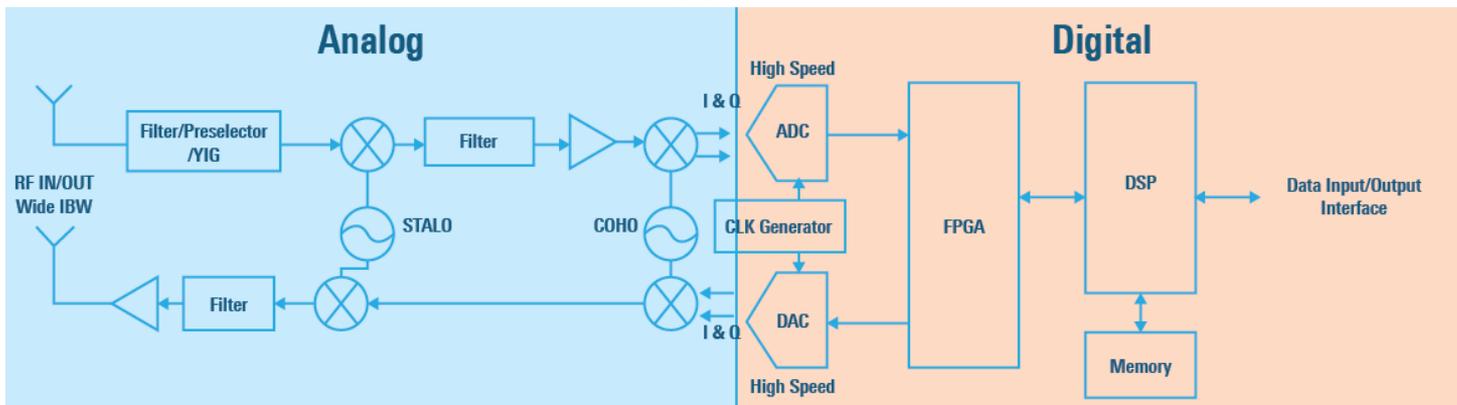


R&S ZNA / ZNB / ZNBT



R&S Pulse Sequencer

R&S Pulse Sequencer



R&S SMA100B



R&S CMA180



R&S SMW



R&S SGx



R&S RTP

DRFM TEST – KEY MEASUREMENTS

▶ System Level

- DF Accuracy/Repeatability
- Deception Techniques
- Phase / Pulse Stability
- Latency
- Spectral Purity
- GNSS Tests
- EMC/EMI
- Coexistence

▶ RF/IF Subsystems

- Spurious measurements
- Dynamic Range
- Compression Point
- Gain/Phase/Frequency Response
- Noise Figure
- Input/Output Impedance
- Image Rejection
- Receiver Sensitivity
- IP3
- Quadrature Error
- LO Phase Noise
- LO Leakage
- LO Long Term Stability
- Antenna Radiation Pattern

▶ Digital Subsystems

- Power/Signal Integrity
- LO/Clock Jitter
- Latency
- Timing
- EQ Flatness
- EMI debugging
- FPGA Tests
- DSP Tests
- ADC/DAC Tests
- SFDR
- EnoB
- Speed
- Quantization Error

DRFM TEST REQUIREMENTS

SYSTEM LEVEL

► System Level Tests

- DF Accuracy/Repeatability
- Deception Techniques
- Phase / Pulse Stability
- Latency
- Spectral Purity
- GNSS Tests
- EMC/EMI
- Coexistence
- Latency



R&S Pulse Sequencer



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Source – US DoD



Source – Apisys



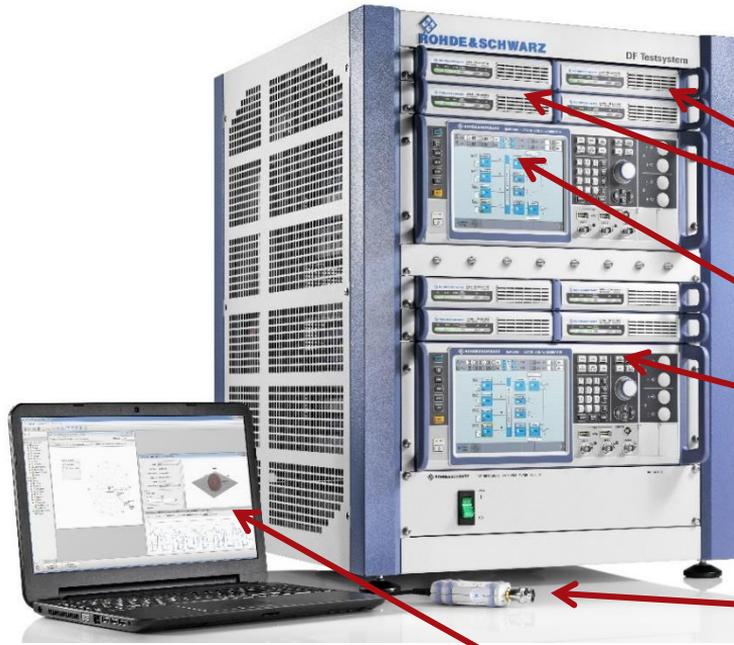
Source – USAF – R.Brooks (Public Domain)



DRFM TEST REQUIREMENTS

SYSTEM LEVEL TESTS – AOA SIMULATION

Angle-of-Arrival estimation and other DF applications require signals that are aligned in time and phase at the reference plane



R&S®SGS100A and R&S®SGU100A for additional RF channels

8 independent RF outputs up to 20 GHz with 160 MHz bandwidth

R&S®SMW200A with 4 separate, independent basebands
Option SMW-B90 Phase Coherence required

R&S®NRP-Z81 power sensor

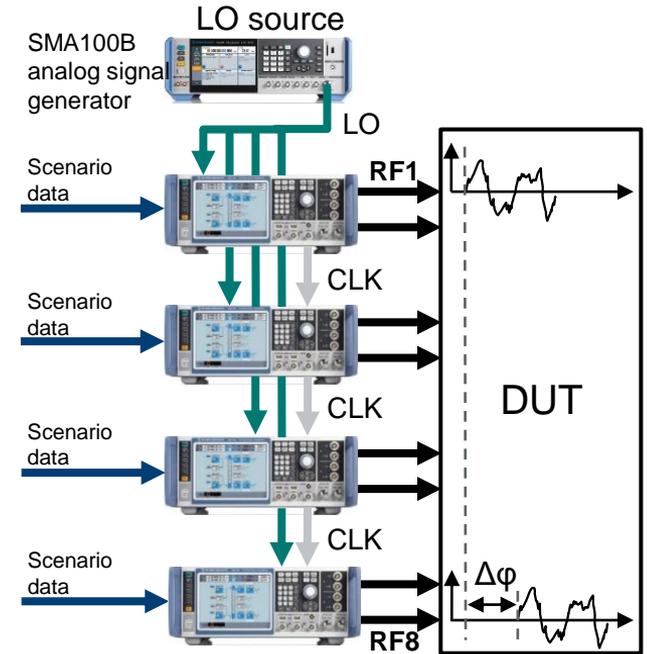
R&S®Pulse Sequencer software for scenario definition and full remote control of system

DRFM TEST REQUIREMENTS

SYSTEM LEVEL TESTS – AOA SIMULATION

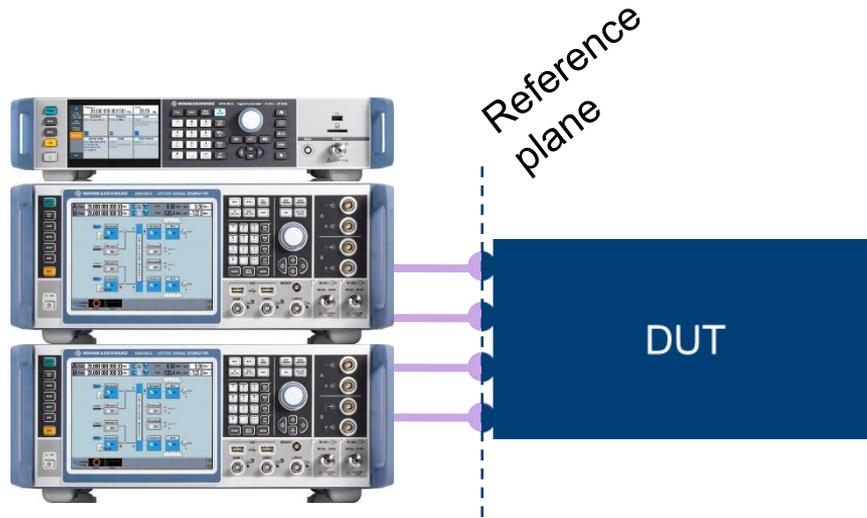
- ▶ EME Scenario (Blue Arrows)
 - R&S Pulse Sequencer S/w provides EME scenario
 - Scenario is streamed via LAN from scenario computer
- ▶ Key H/W requirements
 - Repeatable & stable Amplitude, Phase and time alignment at the RF ports
- ▶ Hardware details
 - Common LO provided by SMA100B - ultra low phase noise, stable analog signal generator (Green arrows) to all SMW200A
 - SMW200A baseband generators are all phase coherent (Black arrows)

Eight phase-coherent RF port system

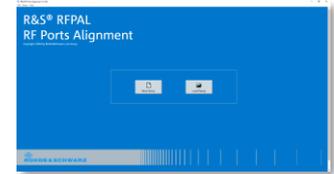


DRFM TEST REQUIREMENTS

SYSTEM LEVEL TESTS – AOA CALIBRATION



- ▶ Option K545
- ▶ PC with RFPAL Software
- ▶ VNA - ZNA, ZNB, ZNBT



DRFM TEST REQUIREMENTS

SYSTEM LEVEL TESTS – DECEPTION TECHNIQUES ANALYSIS

- ▶ Simulation of the dense emitter environment (up to 256 emitters in a 8GHz BW; interleaving / de-interleaving)
- ▶ Generation of realistic radar signals incl radar mode switching
- ▶ Analysis of the deception technique
- ▶ Comparison to original radar signal
- ▶ Streaming of up to 6 million PDWs per second with PDW interleaving

PDW Streaming



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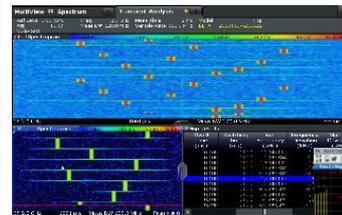
R&S SMW

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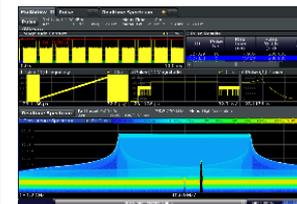
Source – US DoD

R&S FSW



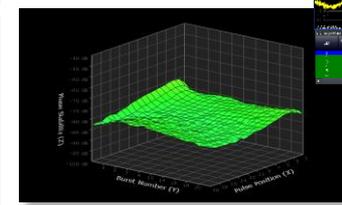
R&S FSW-K60H

R&S FSW-K6



R&S FSW-B800R

R&S FSW-K60C



R&S FSWP-K6P

DRFM TEST REQUIREMENTS

SYSTEM LEVEL TEST - RADAR/EW SCENARIO GENERATION & PULSE GENERATION

- ▶ Pulsed radar signals
 - Ultralong signal playtimes producing hundreds of thousands of pulses combined with frequency and level agility can be achieved with minimum memory requirements
- ▶ Powerful radar signal simulator scenarios
 - Antenna diagrams, scans and interferers with the antenna configuration of receivers
 - AoA of radar transmitters with propagation loss model to provide RF power levels as they occur in real-world scenarios
 - Import of pulse descriptor word (PDW) lists
 - Replaying customer-specific PDW
 - PDW import wizard to simplify definition of existing PDW formats
- ▶ Flexibility
 - Define both radar signals and interferers with complex modulation in one tool
- ▶ Quick results
 - Predefined items that can quickly be combined to create challenging radar test cases
 - User friendliness 3D previews and graphical live
- ▶ Powerful hardware platform
 - The Pulse Sequencer software is designed to take full advantage of the R&S®SMW200A vector signal generator. It offers a maximum RF frequency of 40 GHz and 2 GHz agile bandwidth.
 - Single channel to multichannel phase coherent application support

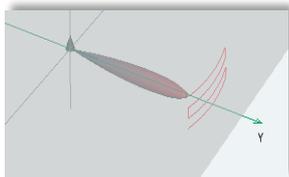


DRFM TEST REQUIREMENTS

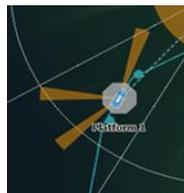
SYSTEM LEVEL TEST - PULSE SEQUENCER SCALABILITY



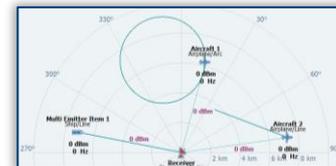
K300: Pulse Sequencer
Define unique Pulses and Sequences



K301 Extended PS
Create localized Emitters



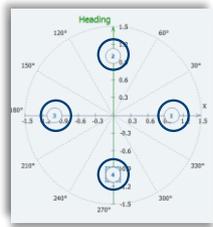
K302 Radar Platforms
Simulate platforms with multiple emitters



K304: Moving Emitters
Simulate Moving Emitters and Receivers



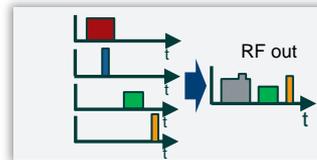
K306: Multiple Emitters
Create dense, multi-emitter environment w/o adding hardware



K308 Direction Finding
Create the Signals to test your DF receiver



K309: Import 2D Maps
Improve visualization of complex scenarios

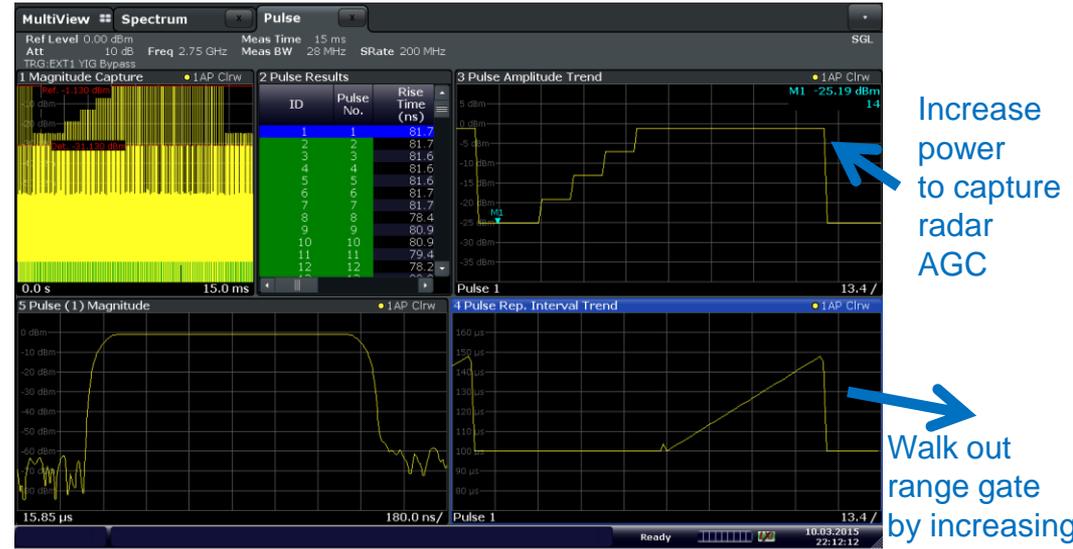


K315: Pulse on Pulse
No Pulse dropping – Just like real life

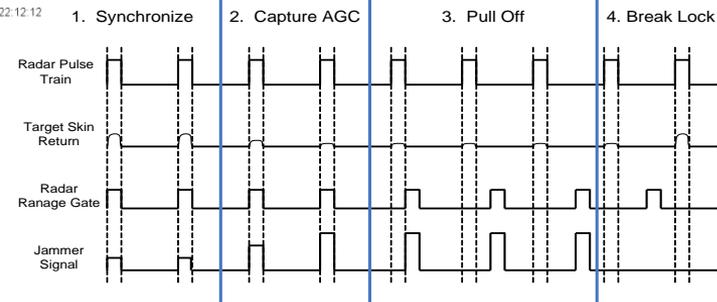
DRFM TEST REQUIREMENTS

SYSTEM LEVEL TESTS - DECEPTION TECHNIQUES ANALYSIS – EXAMPLE RGPO

- ▶ Synchronize with radar PRI (with high stagger levels or jitter this might take more pulses)
- ▶ Increase power of the false target to capture the radars automatic gain control (AGC) and make receiver insensitive
- ▶ Noise Cover Pulse (CP) to further aggravate processing of the real target echo
- ▶ Increasing delay for the false target pulse thus “pulling” radars range gate
- ▶ Dropping the target (may include a “hook” signal) to break lock and forcing the radar to go back to acquisition



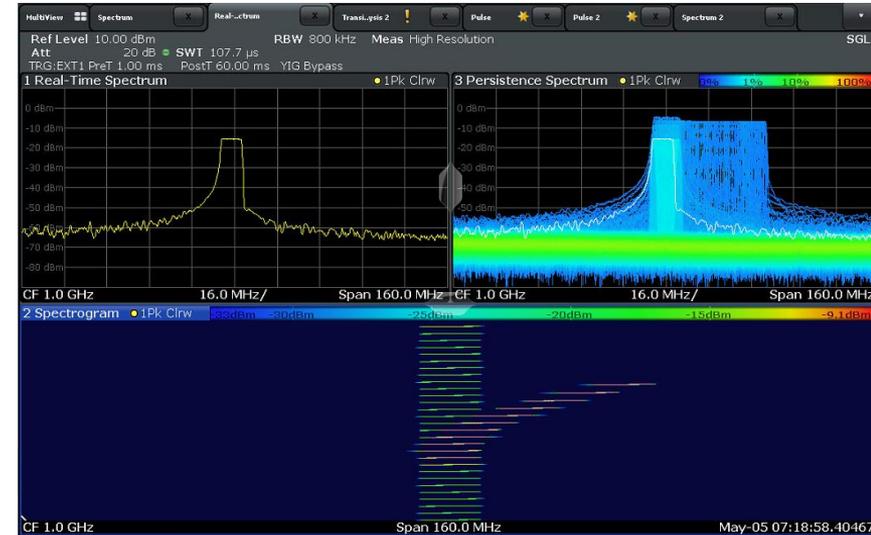
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DRFM TEST REQUIREMENTS

SYSTEM LEVEL TESTS - DECEPTION TECHNIQUES ANALYSIS – EXAMPLE VGPO

- ▶ For MTI Radars, Doppler processing is crucial when tracking targets within velocity gates that are comparable to range gates
- ▶ False targets with a frequency shift can be used to deceive Doppler processing
- ▶ The sequence is similar to RGPO in terms of adjusting AGC and increasing the frequency offset over time
- ▶ To accurately walk off the true target return, the frequency must change in increments that are detectable at the receiving radar
- ▶ Most Doppler radars associate differential velocity changes as target acceleration and check/flag unusual behavior such as a sudden ‘jump’ or other unrealistic changes

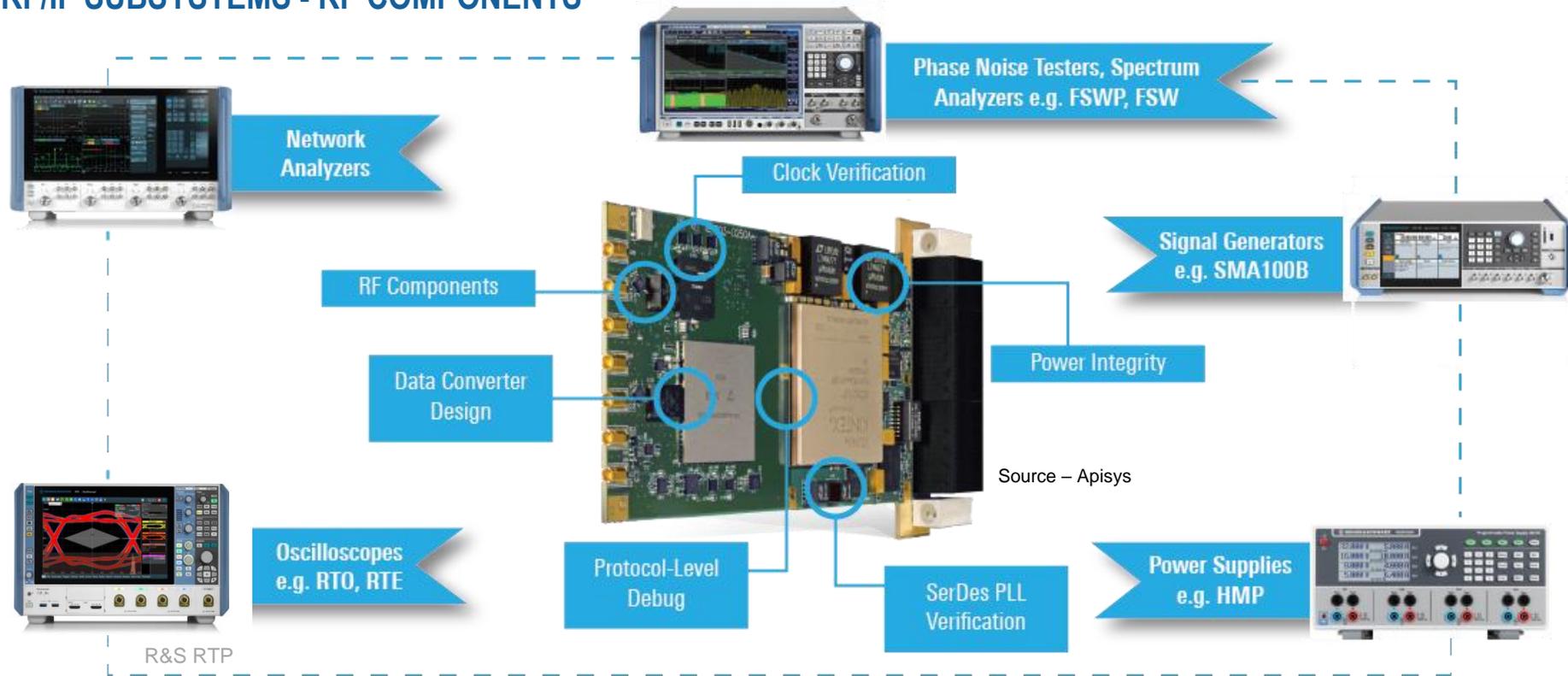


R&S RTP 'SCOPE FOR LATENCY MEASUREMENT

- ▶ A time domain instrument such as an 'scope is ideal for measuring latency
- ▶ Can measure exact time of interactions down to 1 sample
- ▶ Able to analyze both time & frequency information over a large bandwidth
- ▶ Multiple channels allows capture of both received and transmitted signals in a single instrument

DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS - RF COMPONENTS



DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS

► RF/IF Subsystems

- Spurious measurements
- Dynamic Range
- Compression point
- Gain/Phase/Frequency Response
- Noise Figure
- Input/Output Impedance
- Image rejection
- Receiver sensitivity
- IP3
- Quadrature error
- LO Phase Noise / Leakage / Long Term Stability
- Antenna radiation pattern



DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS – PHASE NOISE / VCO CHARACTERIZATION - FSWP

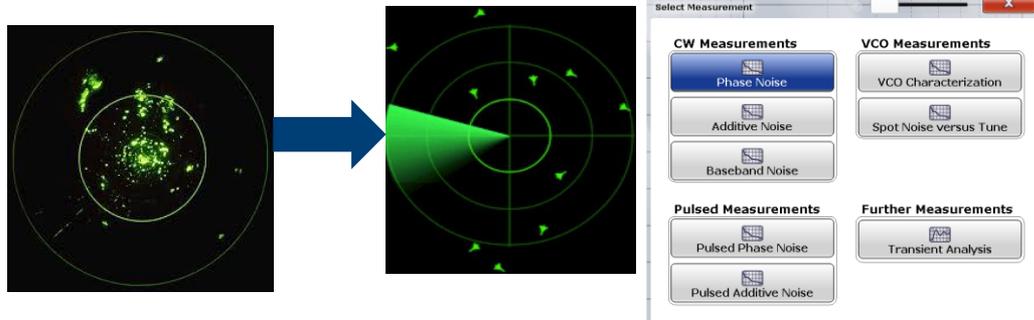


► Benefits

- Fast – from hours to minutes
- Easy – at the push of a button, no additional components
- Accurate – highest performance phase noise measurement available

► Highlights

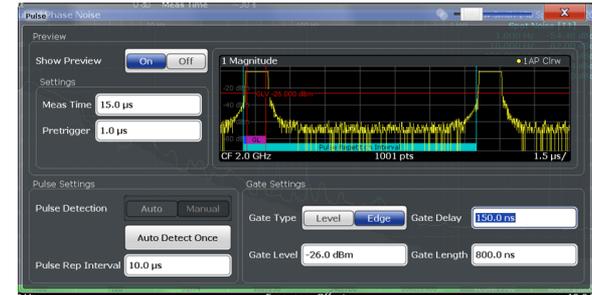
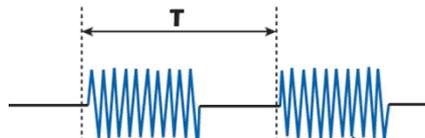
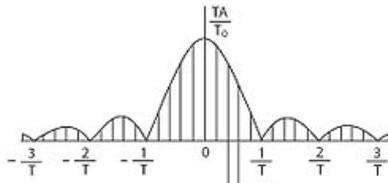
- Phase noise, VCO tester, signal and spectrum analyzer a single box
- Measurement of phase noise on pulsed sources
- Simultaneous measurement of amplitude noise and phase noise
- Internal source for measuring additive phase noise
- Low-noise internal DC sources for VCO characterization



DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS - RADAR/EW PULSED PHASE NOISE – K4

- ▶ Specifically designed for the R&S FSWP phase noise analyzer to measure:
 - Components and system level measurement
 - VCO measurements
- ▶ Simple setup & stable results
- ▶ High sensitivity cross-correlated measurements even in desensitized environment with low average signal power due to long pulse off times
- ▶ Transient gating suppression option
- ▶ Automatic pulse parameter measurement



DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS - PULSE STABILITY

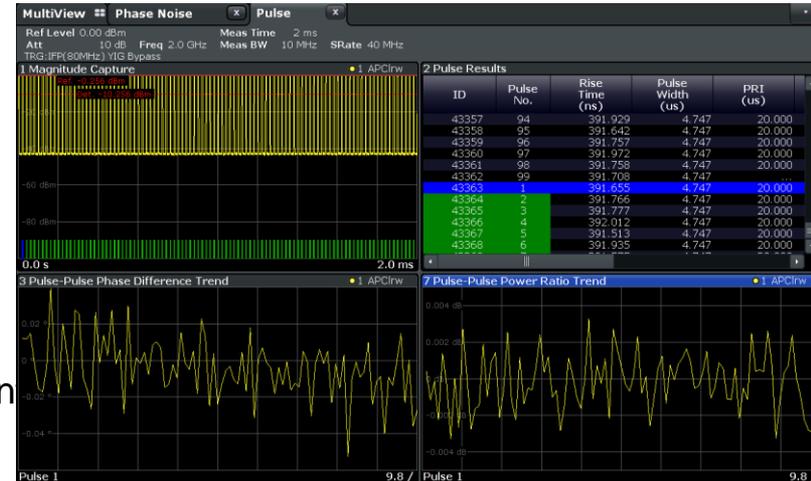
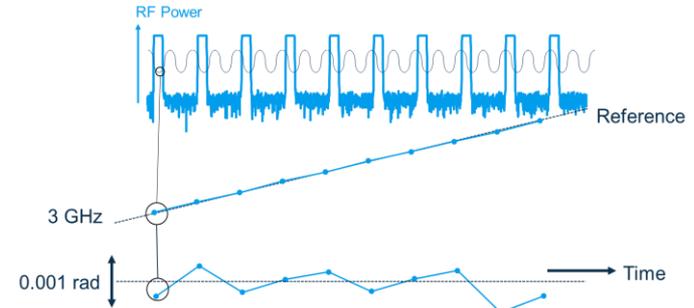
- ▶ Factors affecting pulse stability:
 - Phase noise in components such as oscillator, mixer, multiplier and filter
 - Electromagnetic perturbations
 - causing parasitic coupling between or inside modules
 - Thermal variation in power devices
 - Fluctuation in switching power supply
 - Causes ripple and slow variation of bias
 - AM-PM conversion in a saturated amplifier
 - Mismatch between different stages of the transmitter module
 - Memory effects (thermal and trapping effects)

DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS - PULSE STABILITY - FSWP-K6P

Component or system test for Coherent Radar

- ▶ Problem: GaN based ASEA systems experience heating
 - Heat distorts phase
 - Testing needed to understand distortions & compensate
 - Important for MTI & Doppler radars
- ▶ Measurement: compare multiple pulses
 - Phase compare
 - Amplitude compare
 - Compare previous pulse
 - Compare to a reference amplitude/phase
- ▶ Benefit: testing power amplifiers using relative measurement
- ▶ Problem: measuring radar and electronic warfare systems
- ▶ Measurement: Compare pulses, Absolute measurement

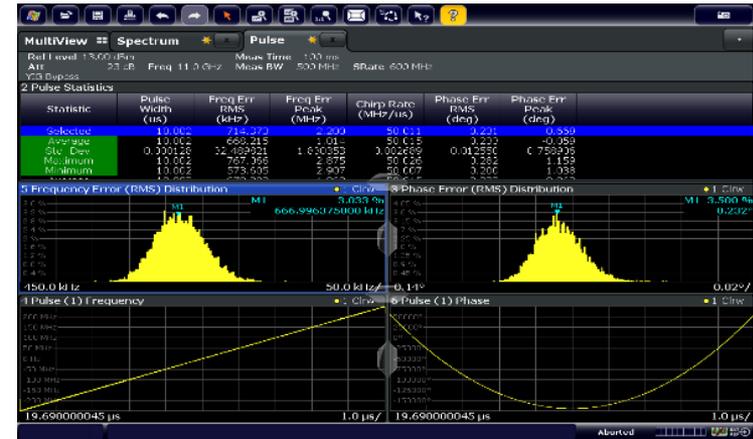


DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS - PULSE MEASUREMENTS – FSW K6

Rapid spurious identification, low phase noise, extensive pulse analysis functions and wide analysis bandwidth for the R&S FSW spectrum analyzer

- ▶ Analyzes up to 400 MS of IQ data at 100 MSps in ~ 4 seconds
 - Segmented capture allows for deep capture of low duty cycle pulses
- ▶ RF Pulse Detection
 - Threshold method with dropout tolerance for modulated bursts
 - Absolute and relative (to ref. level, peak and noise) thresholds
- ▶ Pulse Envelope Measurements
 - Timing (e.g. Width, Rise/Fall Time, PRI, etc.)
 - Amplitude (e.g. Peak Power, Average On, Average Tx, etc.)
 - Phase / Frequency (e.g. Frequency, Phase, Frequency Error, etc.)
- ▶ Measurement Displays
 - Table of pulse statistics
 - One parameter over time, for one pulse (i.e. phase vs. time)
 - One parameter over all pulses (trending)

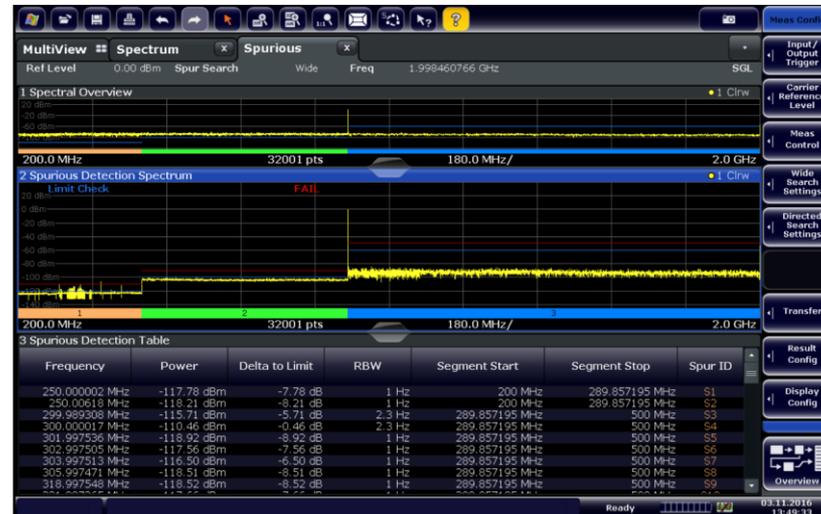


DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS - SPURIOUS MEASUREMENTS – FSW-K50

- ▶ Timesaving 1 button setup
- ▶ RBW is automatically calculated based on maximum expected spur level
- ▶ Automatically measures noise floor and sets RBW – saves a lot of time
- ▶ Uses I/Q and FFT techniques and wide-band captures to speed up search time
- ▶ Up to 30 times faster for very low level spur searches
- ▶ Verifies if identified spurs are real or internally generated
- ▶ Avoids measurement at known DUT output frequency

	Range 1	Range 2	Range 3	Range 4
Range Start	30 MHz	300 MHz	500 MHz	1 GHz
Range Stop	300 MHz	500 MHz	1 GHz	2 GHz
Spur Detection Threshold Start	-132 dBm	-130 dBm	-125 dBm	-120 dBm
Spur Detection Threshold Stop	-132 dBm	-130 dBm	-125 dBm	-120 dBm
Limit Offset to Detection Threshold	0 dB	0 dB	0 dB	0 dB
Peak Excursion	3 dB	3 dB	3 dB	3 dB
Minimum Spur SNR	10 dB	10 dB	10 dB	10 dB
Maximum Final RBW	100 kHz	100 kHz	100 kHz	100 kHz
Auto RBW	On	On	On	On
RBW	Auto	Auto	Auto	Auto
Number of FFT Averages	2	2	2	2
Ref Level	0 dBm	0 dBm	0 dBm	0 dBm
RF Attenuation	10 dB	10 dB	10 dB	10 dB
Preamp	Off	Off	Off	Off



DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS - TIME SIDELobe MEASUREMENTS – FSW K6S

- ▶ Pulse Compression measurements for FSW Spectrum Analyzer
- ▶ Features:
 - Frequency range from 2 Hz to 85 GHz; up to 500 GHz with external mixers
 - Wide analysis bandwidth up to 2 GHz
 - Low phase noise of -137 dBc (1 Hz) at 10 kHz offset (1 GHz carrier)
- ▶ Benefits
 - Can be used to analyze your own proprietary waveforms
 - Easy configuration and fast measurement results
 - Automated detection, measurement and analysis of pulses and pulse compression

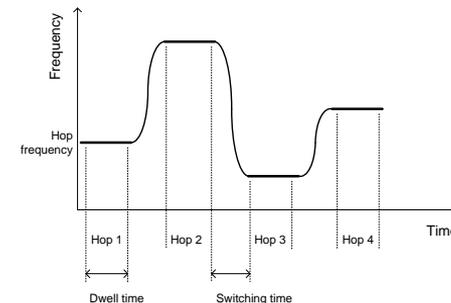
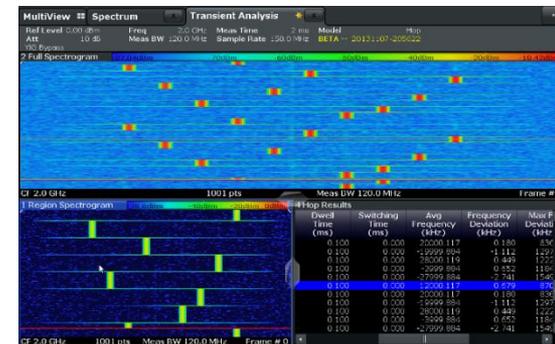
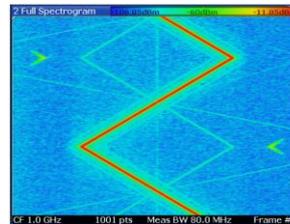


DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS - TRANSIENT SIGNAL ANALYSIS – K60

► A toolkit for the analysis of “transient signals” in time or frequency domains

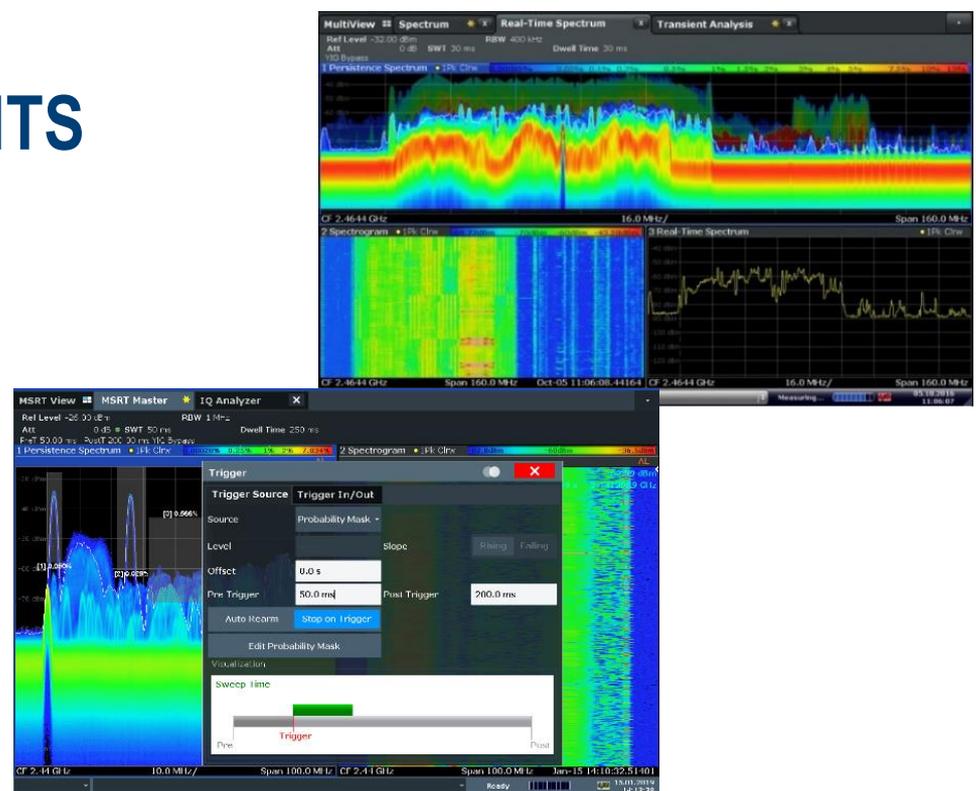
- Signals with which may **appear briefly** or **change rapidly** in time
- Radar pulses
- Frequency-hopping Signals
- Spurious emissions
- Chirped FM signals
- Oscillator lock time
- Signals with a time-varying characteristics over large bandwidths



DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS - REAL TIME ANALYSIS

- ▶ 160 MHz, 512 or 800 MHz real-time bandwidth
- ▶ More than 2 Million FFT/s
- ▶ 100% POI of 0.46 μ s at full amplitude accuracy
- ▶ Scalable FFT size (1k...32k)
- ▶ Multi standard real-time (MSRT)
- ▶ Multi display/range analysis
 - Persistence
 - Real-time spectrum
 - Spectrogram
- ▶ Up to 8 GB memory - 900 msec @ 2 GHz BW
- ▶ Pre and Post-Trigger Analysis
- ▶ Useful for Range-Gate Pull off measurements



Figures of Merit for Real-time Analysis

	R&S FSW-K161R	R&S FSW-B512R	R&S FSW-B800R
FFT Length	1024 to 16 k	1024 to 32 k	512 to 16 k
Max. RT Bandwidth	160 MHz	512 MHz	800 MHz
Max. FFT Rate (FFT/s)	585,938	1,171,875	2,343,750
POI	1.87 μ s	0.91 μ s	0.46 μs
RBW for Span/RBW	6.35 to 3200	6.25 to 6400	6.35 to 3200

DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS - ANTENNA TESTS

Test Systems
Interference, TRM,
Phase Coherent Signals



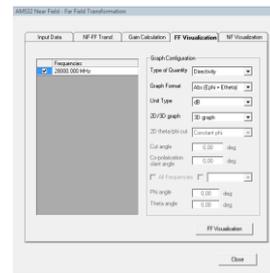
R&S ATS1000



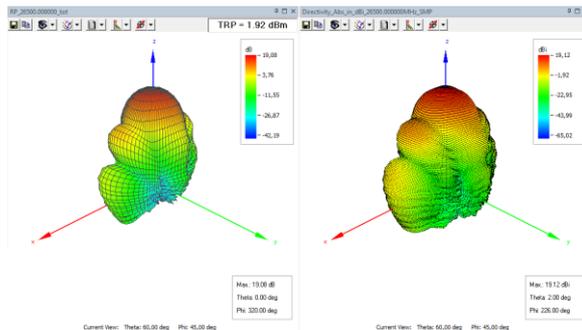
R&S DST200



R&S AMS32



R&S ZNAxx



ATS1000: Passive Antenna Measurement and Nearfield - Farfield Transformation Application Note

Products:
• RSPATS1000
• RSPATS200
• RSPATS300

This application note describes how to measure the antenna pattern of a near-field device in the RSPATS1000 oriented situation. This includes the required calibration of the measurement setup and a possible near-field to far-field transformation when measuring larger devices.

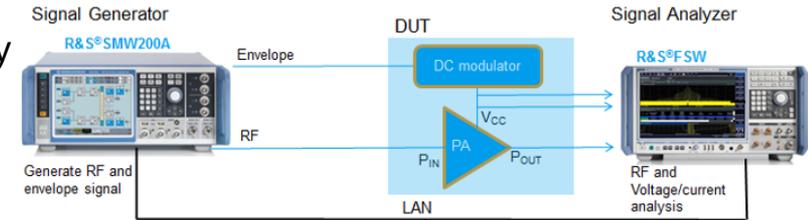
Note:
Visit our homepage for the most recent version of this application note <http://www.rohde-schwarz.com/antenna-testing>



DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS - AMPLIFIER MEASUREMENTS

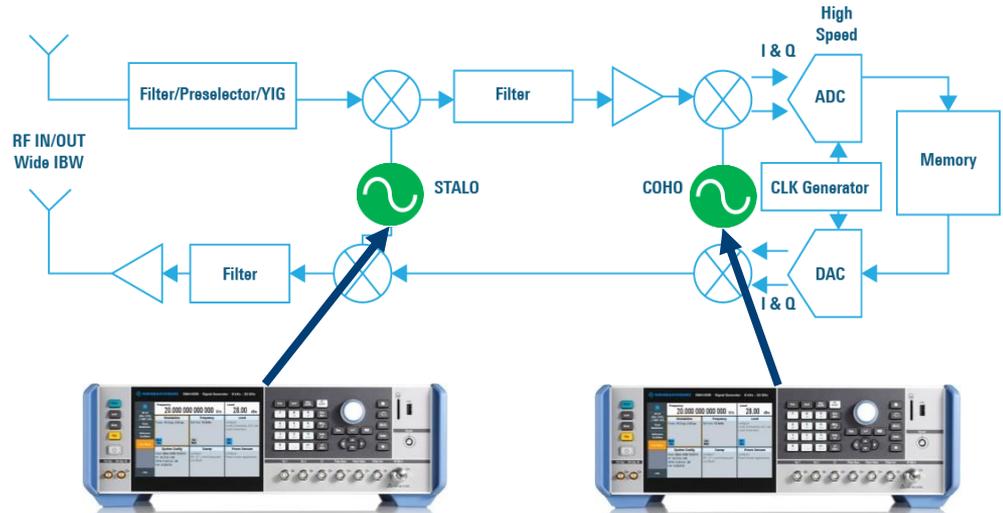
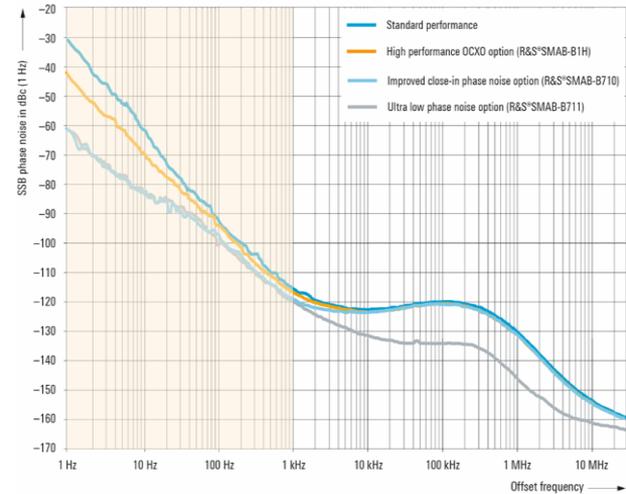
- ▶ Conventional Power Amplifier Measurements
 - Linear / Nonlinear distortion measurements
 - AM/AM, AM/PM, EVM, ACLR
 - Gain / Transfer, Channel Response, Group Delay
- ▶ Envelope Tracking Measurements
 - Full ET amplifier characterization
 - Measurement of ET impact on efficiency - Signal quality / power added efficiency (PAE)
- ▶ Digital Predistortion
 - Real-time predistortion with SMW Signal Generator
- ▶ High dynamic range for RX band noise measurement



DRFM TEST REQUIREMENTS

RF/IF SUBSYSTEMS - CLOCK SUBSTITUTION

- ▶ COHO & STALO substitution is used to provide the best quality clocks used during design verification
- ▶ R&S®SMA100B can be used as:
 - COHerent Oscillator (COHO) phase reference for the DDS, IF Digitizer and/ or I/Q modulator/demodulator
 - Stable Local Oscillator (STALO) for the microwave exciter and receiver
- ▶ Critical Requirements Addressed:
 - Phase Noise
 - AM Noise
 - Broadband Noise Floor
 - Spurious



POWER SENSORS

- ▶ Accurate power measurement of received and transmitted signals
- ▶ Accurate, absolute power measurements
- ▶ Wideband frequency response in a single sensor DC – 100 GHz)



3-path diode sensors 

OTA power sensors 

Wideband power sensors 

Thermal power sensors 

Average power sensors 

2-path diode sensors 

Frequency selective power meter 

Level range	Frequency Range
-70 dBm to +45 dBm	10 MHz to 90 GHz
-76 dBm to -19 dBm	18 GHz to 90 GHz
-60 dBm to +20 dBm	50 MHz to 50 GHz
-35 dBm to +20 dBm	DC to 110 GHz
-70 dBm to +23 dBm	18 kHz to 18 GHz
-60 dBm to +20 dBm	10 MHz to 18 GHz
-130 dBm to +20 dBm	50 MHz to 6 GHz

DRFM TEST REQUIREMENTS

DIGITAL SUBSYSTEMS

► Digital Subsystems

- Power/Signal Integrity
- LO/Clock Jitter
- Latency
- Timing
- EQ Flatness
- EMI debugging
- FPGA Tests
- DSP Tests
- ADC/DAC Tests
- SFDR
- EnoB
- Speed
- Quantization Error

Your challenge...

With data converters at the heart of almost every electronic design, this flyer focuses on the main measurement challenges in this field. It also provides an overview of the industry-leading test and measurement solutions from Rohde & Schwarz for development, characterization and production.

More information at
www.rohde-schwarz.com/data-converter

Power delivery
 To ensure proper system performance, data converters and clocks need to be powered with clean supply voltages. Low-dropout (LDO) regulators are often used to improve supply voltage stability in today's data converter designs.

Power integrity
 Power integrity issues such as noise, ripple and crosstalk have a strong impact on the performance of your data converters.

Rohde & Schwarz oscilloscopes and power rail probes efficiently detect and solve power integrity problems in your data converter designs:

- High sensitivity for measuring small signals and small interference
- Power rail probes with high offset range to increase resolution on ripples, noise and interference
- Powerful FFT and multidomain functionality to analyze signals

Clock substitution
 Proper clock performance is essential in data converter designs. Rohde & Schwarz signal generators can be used as high-quality clock replacements:

- Outstanding close-in and wideband phase noise performance to ensure superior low jitter
- High spectral purity to unveil the optimal performance of the DUT
- High output power to compensate cable losses

Clock verification
 Clock jitter and spectral purity have a direct impact on the dynamic range of the converter. Rohde & Schwarz phase noise analyzers verify phase noise and spectrum performance of your clock:

- High-sensitivity phase noise measurements to determine the true clock characteristics in a short measurement time
- Internal source for measuring additive phase noise
- Built-in spectrum and signal analyzer

Performance characterization
 Data converters are core components in many electronic and RF designs. Their performance parameters, such as effective number of bits (ENOB), signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), linearity and latency, have a direct impact on overall system performance.

Rohde & Schwarz spectrum and signal analyzers verify the signal quality at the output of the digital-to-analog converter:

- Excellent spectral purity to catch even the slightest effects
- Outstanding bandwidth and error vector magnitude (EVM) performance for testing signals with digital modulation

Rohde & Schwarz signal generators stimulate the input of the analog-to-digital converter with ideal signals:

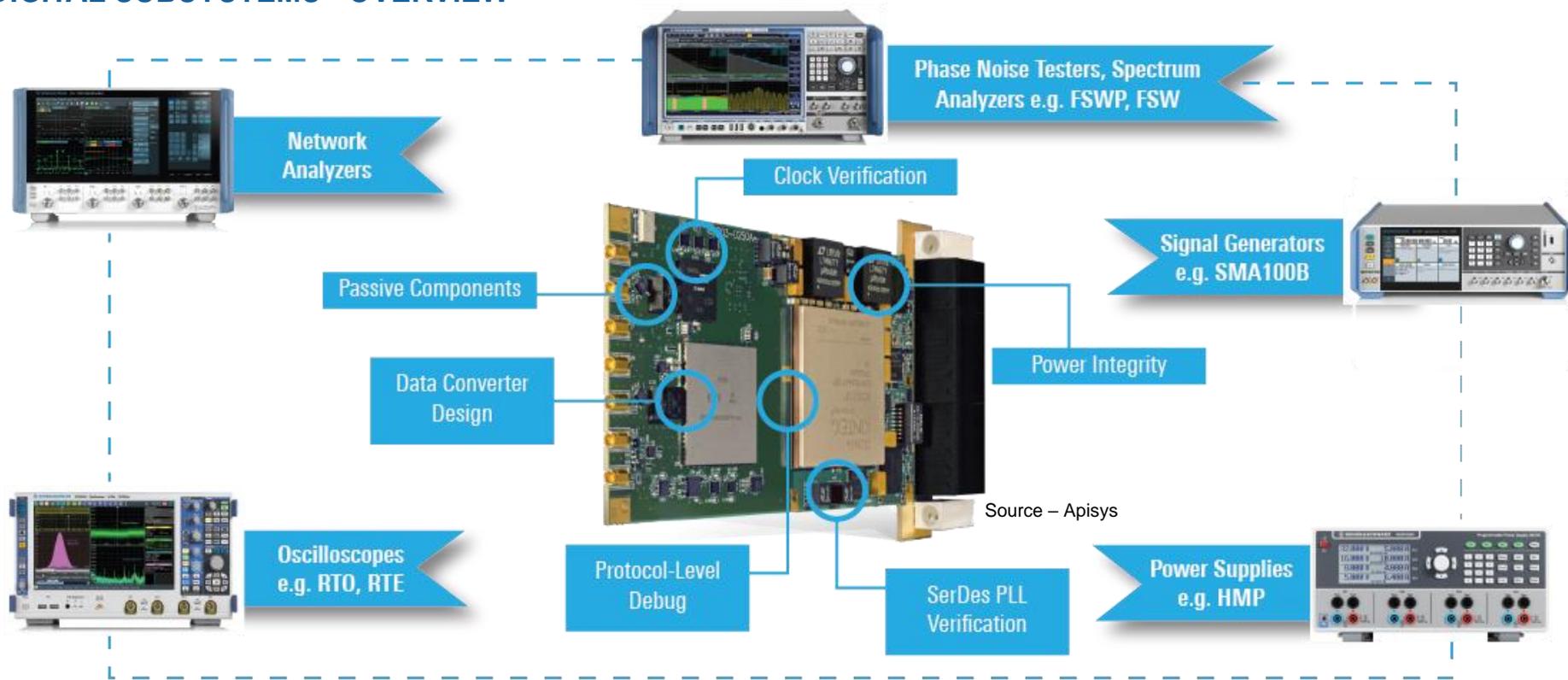
- Excellent phase noise and spectral purity to see the DUT in its best light
- Outstanding bandwidth and EVM performance to provide any signal with digital modulation

Rohde & Schwarz oscilloscopes analyze the LVDS, JESD204 input/output of the data converter:

- Digital trigger for maximum trigger accuracy
- Fast trigger and decode functionality for accurate timing measurements
- Comprehensive eye diagram and jitter analysis to examine the purity of the digital signal

DRFM TEST REQUIREMENTS

DIGITAL SUBSYSTEMS - OVERVIEW



DRFM TEST REQUIREMENTS

DIGITAL SUBSYSTEMS - POWER INTEGRITY

Building Blocks

- ▶ Power Distribution Network (PDN)
- ▶ Low DropOut (LDO) regulators

- ▶ Typical Performance Parameters
 - Power integrity: ripple, noise, ...
 - PDN impedance:
 - Resonances cause Power Integrity problems
 - Resonances cause EMI / EMS problems
 - LDO power supply rejection ratio (PSRR)



Source – Apisys



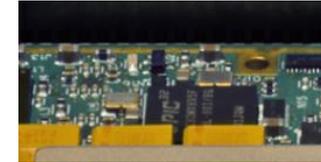
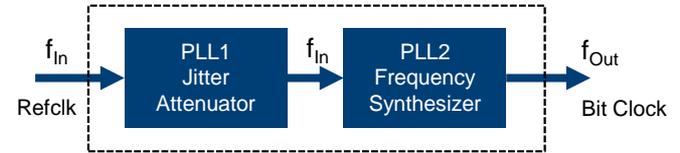
DRFM TEST REQUIREMENTS

DIGITAL SUBSYSTEMS - CLOCK JITTER

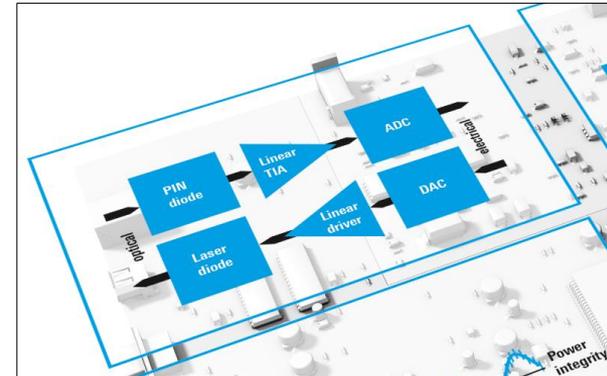
Building Blocks

- ▶ ADC / DAC clock synthesizers
- ▶ SerDes PLLs
- ▶ Often two-stage architecture

- ▶ Typical Performance Parameters
 - Absolute phase noise / jitter
 - Additive phase noise / jitter
 - Jitter attenuation (Jitter Transfer Function JTF)
 - System margin testing
 - Power supply noise rejection (PSNR)



Source – Apisys



DRFM TEST REQUIREMENTS

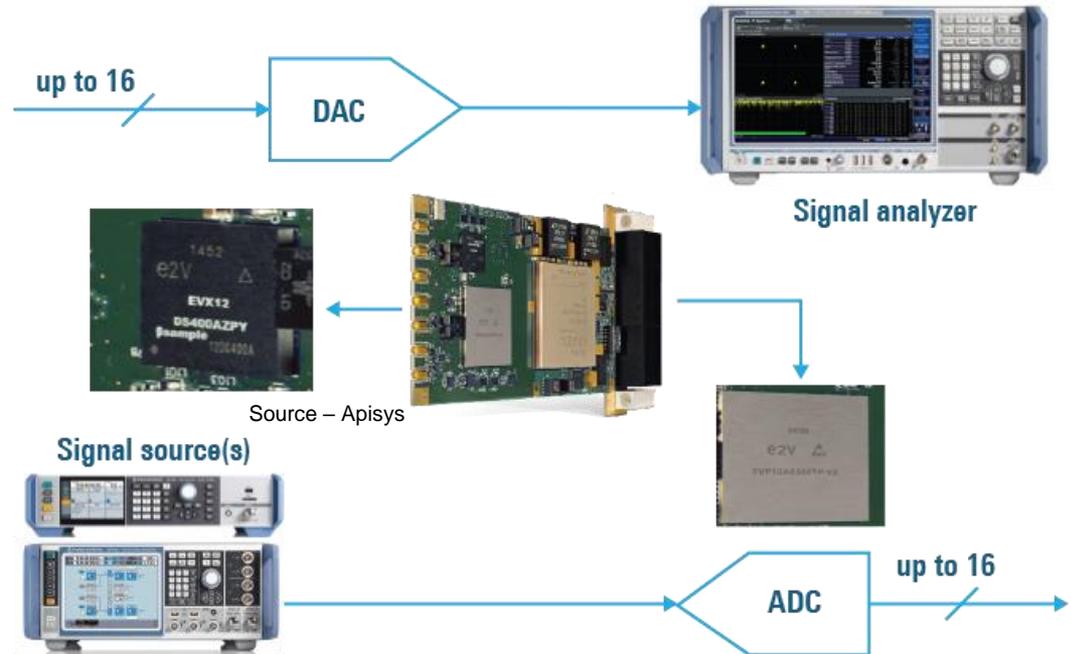
DIGITAL SUBSYSTEMS - ADC/DAC MEASUREMENTS

► DAC

- Testing of output signal quality like SFDR
- Phase noise testing
- Measurement of modulation quality for digital output signal like EVM, ACLR, ...
- Test signals generated in test mode by DAC or from an external baseband source

► ADC

- Testing of RF input circuitry
- Generic testing with single and dual tone CW signals (intermodulation)
- Test with real signal as used in later application



DRFM Test - Summary

Wideband Signal Analysis
8.5 GHz



Transient Signal Analysis
FSW – K60



Cutting Edge RF Component Tests
R&S ZNA



Modern Pulse Analysis
FSW –K6



Side-lobe measurements
FSW-K6S



Fast & Accurate Phase Noise Test
FSWP



Vector Signal Explorer



Field-to-Lab
Radar Target Generation



THANK YOU
I WELCOME QUESTIONS



APPENDIX 1 - LIST OF ACRONYMS

ADC	Analog to Digital Converter	EW	Electronic Warfare
AESA	Active Electronically Scanned Array	IFM	Instantaneous Frequency Measurement
AoA	Angle of Arrival	MTI	Moving Target Indicator
CPI	Coherent Processing Interval	RCS	Radar Cross Section
CVR	Crystal Video Receiver	RFFE	Radio Frequency Front End
DAC	Digital to Analog Converter	RGPO	Range Gate Pull Off
DF	Direction Finding	VGPO	Velocity Gate Pull Off
DIFM	Digital Instantaneous Frequency Measurement	SPG	Signal Processing Gain
DRFM	Digital RF Memory	SWaP	Size Weight and Power
DSP	Digital Signal Processor	ToT	Time on Target
FPGA	Field Programmable Gate Array	TRM	Transmit Receive Module
ECM	Electronic Counter Measure		
ECCM	Electronic Counter-Counter Measures		

APPENDIX 2 - FAIR USE STATEMENT

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