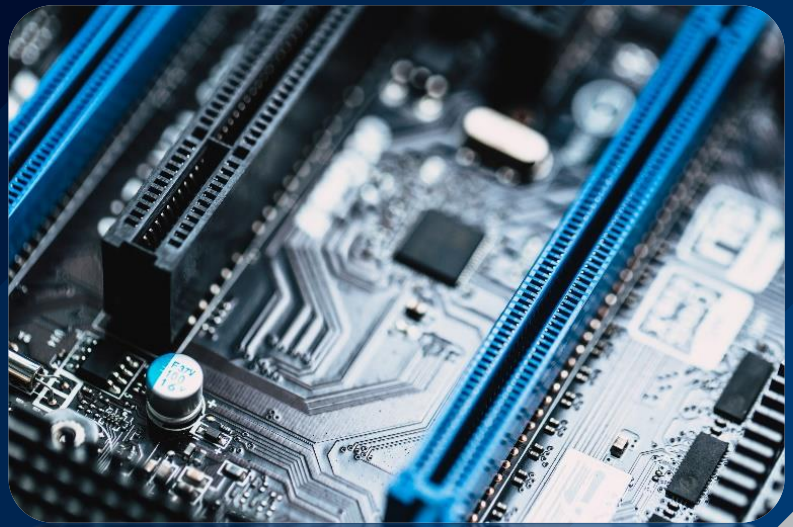
SIGNAL INTEGRITY HIGH-SPEED INTERFACE TESTING LANDSCAPE



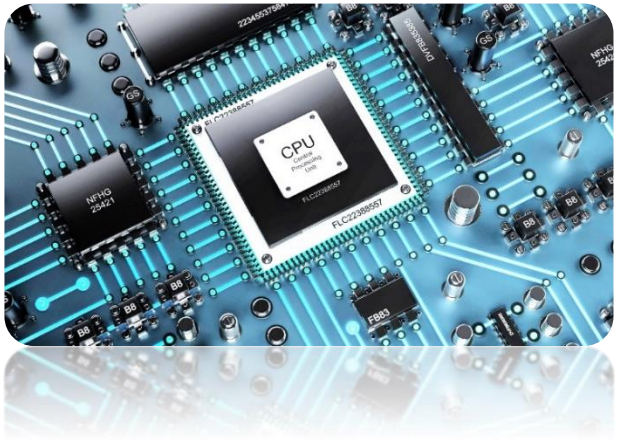
Bryant Hsu
Product Manager
Business Development and Marketing Dept.

ROHDE&SCHWARZ
Make ideas real

JPC connectivity

AGENDA

- Application Overview
- VNA Based S-Parameter for Signal Integrity Analysis
- High-Speed Interface Challenges and Test Requirements
- Accurate Measurement with Probes or Test Fixture
- Conclusions



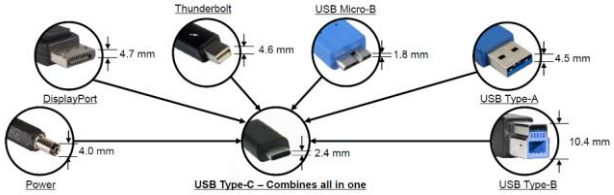
APPLICATION OVERVIEW

HIGH SPEED DIGITAL INTERFACES EXAMPLE

- USB - Universal Serial Bus
  - USB4 Gen2 (20 Gbps), Gen3 (40 Gbps)
  - USB3.2 Gen1 (5 Gbps), Gen2 (10 Gbps), Gen2x2 (20 Gbps)

- PCIe - Peripheral Computer Interconnect Express
  - PCIe Gen4 (16 Gbps), Gen5 (32 Gbps), Gen6 (64 Gbps)

- (Q/O)SFP(-DD) - (Quad/Octal) Small Form-factor Pluggable
  - 400/800 GbE using PAM-4



Picture reference: wikipedia

USB EVOLUTION

USB1.0
1.5 Mbps
Low Speed

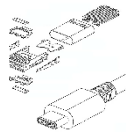
USB1.1
12 Mbps
Full Speed

USB2.0
480 Mbps
High Speed

USB3.0
5 Gbps

USB3.2 Gen1x1
5 Gbps
Super Speed

USB3.2 Gen2x1
10 Gbps
Super Speed+



USB3.2 Gen 2x2
20 Gbps
Super Speed+

1996 1998 2001 2005 2008 2010 2011 2012 2014 2017 **2019 (AUG)**

Wireless USB
rev1.0

rev1.1

USB On-The-Go

USB Type-C
rev1.0

USB Power Delivery
rev1.0

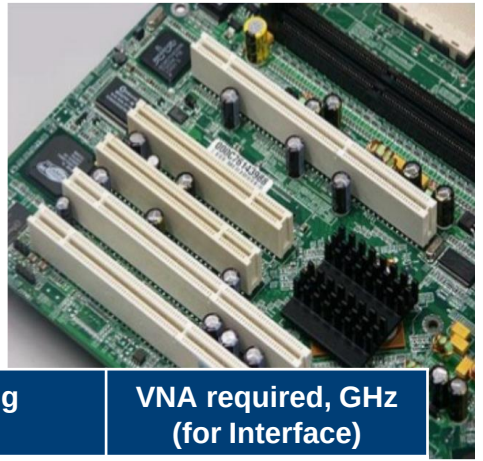
USB3.2 Gen 1x2
10 Gbps
Super Speed+

Dual Lane Mode

Key characteristics:

- Two-lane operation using existing USB Type-C cables and up to 40 Gbps operation
- Multiple data and display protocols
- Backward compatibility with USB 3.2, USB 2.0 and Thunderbolt 3

PCI EXPRESS (PCIe)



- Introduced in 2004
- Peripheral Component Interconnect Express is the de facto standard to connect high performance IO devices to the rest of the system. Eg.NICs, NVMe, graphics, TPUs
- Computer to Peripheral Communication
- Overseen by PCI-SIG
- Full-duplex bidirectional
- Backwards compatibility

Generation	Transfer Rate	Total x 16 BW	Coding	VNA required, GHz (for Interface)
PCIe 1.x	2.5 GT/s	4 GB/s	8b/10b	ZNB8
PCIe 2.x	5.0 GT/s	8 GB/s	8b/10b	ZNB8
PCIe 3.x	8.0 GT/s	~ 16 GB/s	128b/130b	ZNB20
PCIe 4.x	16.0 GT/s	~ 32 GB/s	128b/130b	ZNB20
PCIe 5.x	32.0 GT/s	~ 64 GB/s	128b/130b	ZNB40
PCIe 6.x	64.0 GT/s	~ 128 GB/s	128b/130b (PAM)	ZNB40 (spec. in progress)

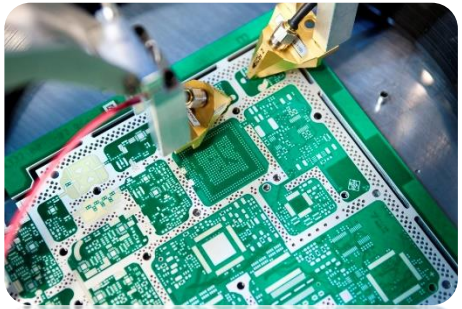
HIGH SPEED ETHERNET INTERFACE

IEEE spec.	Infiniband	Form factor	Baud rate, GBd	Code rate	Data Rate, Gbps (per lane)	VNA requirement, GHz
802.3bj	EDR	SFP28 QSFP28	25.78125	64b/66b, NRZ	25	25
802.3cd	HDR	SFP56 SFP-DD-100G QSFP56 QSFP-DD-400G OSFP-400G	26.5625	64b/66b, PAM4	50	26.565
802.3ck	NDR	SFP112 SFP-DD112 QSFP112 QSFP-DD-800G OSFP-800G	53.125	64b/66b, PAM4	100	40~50 (spec in progress)

HIGH SPEED INTERFACE CHAIN FOR MOTHERBOARD

PCB material manufacture

- Glass fiber / Fiberglass cloth
- Copper foil
- PI / Resin



PCB manufacture

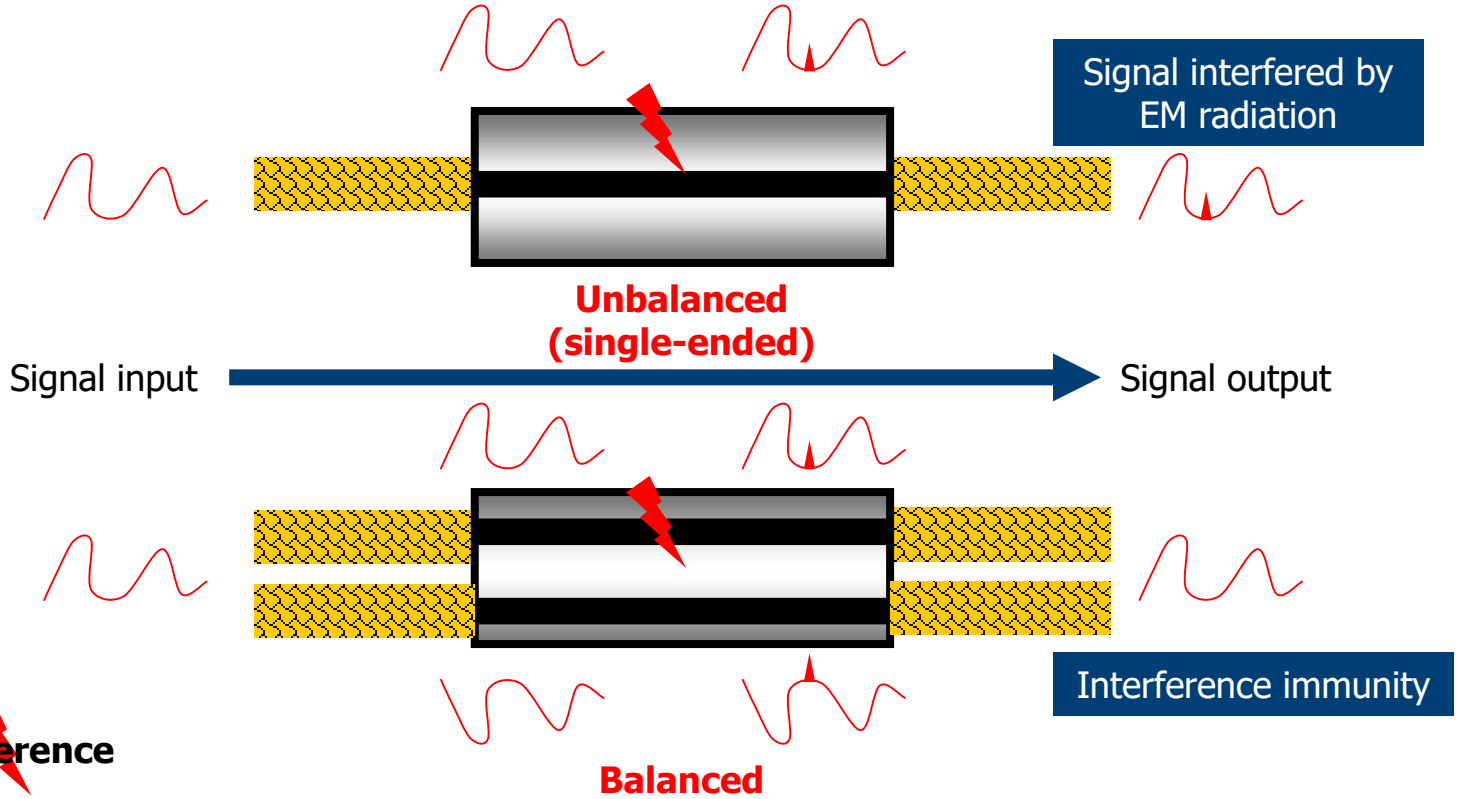
- Copper foil substrate
- PCB /FPC
- IC packaging substrate

Electronics product

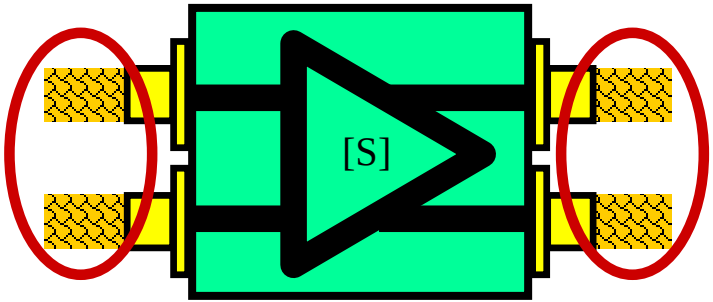
- TV / Laptop
- Smart phone
- Consumer products

VNA BASED S-PARAMETER FOR SIGNAL INTEGRITY ANALYSIS

BALANCED AND UNBALANCED MODE



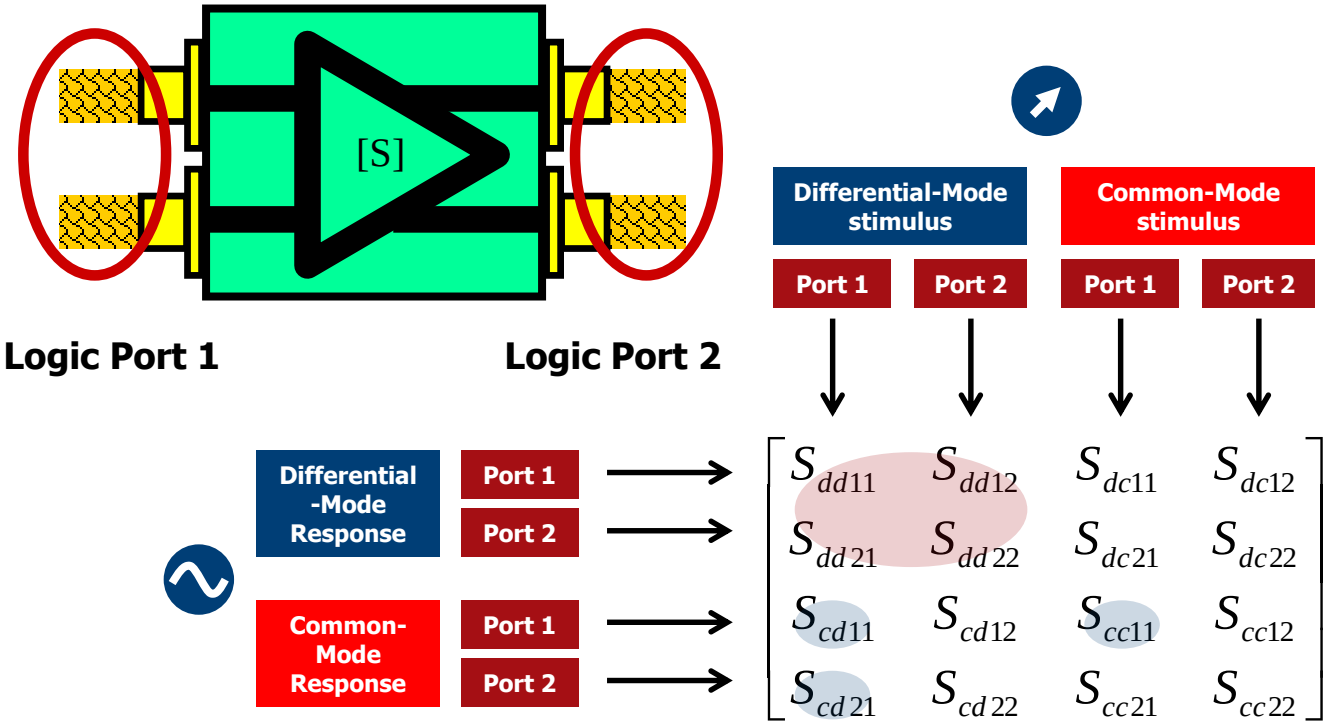
MIXED-MODE S-PARAMETER MATRIX



$$S_{xyab}$$

x and y can be:
- d (differential mode)
- c (common mode)

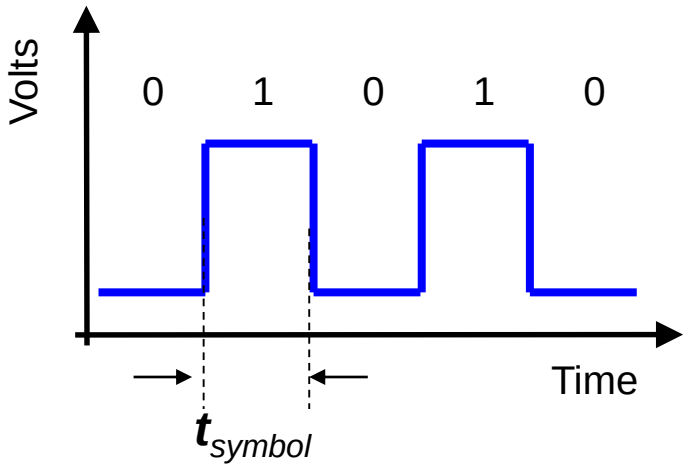
MIXED-MODE S-PARAMETER MATRIX

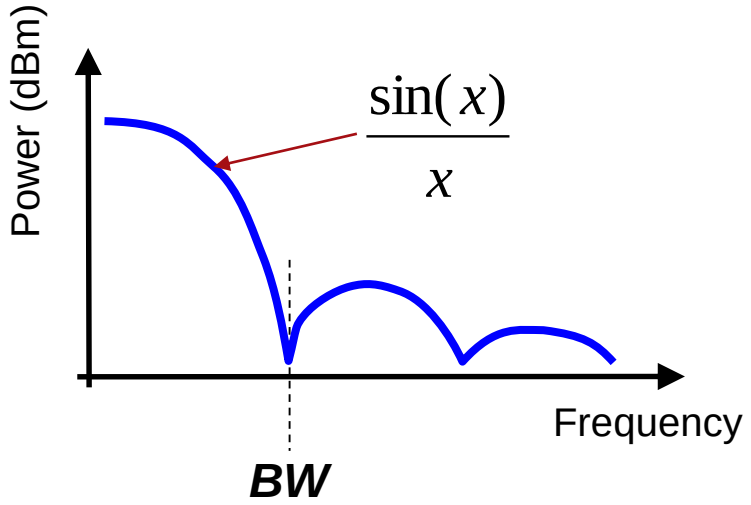


HIGH-SPEED INTERFACE CHALLENGES AND TEST REQUIREMENTS

TIME VS. FREQUENCY FOR A SIGNAL

Ideally

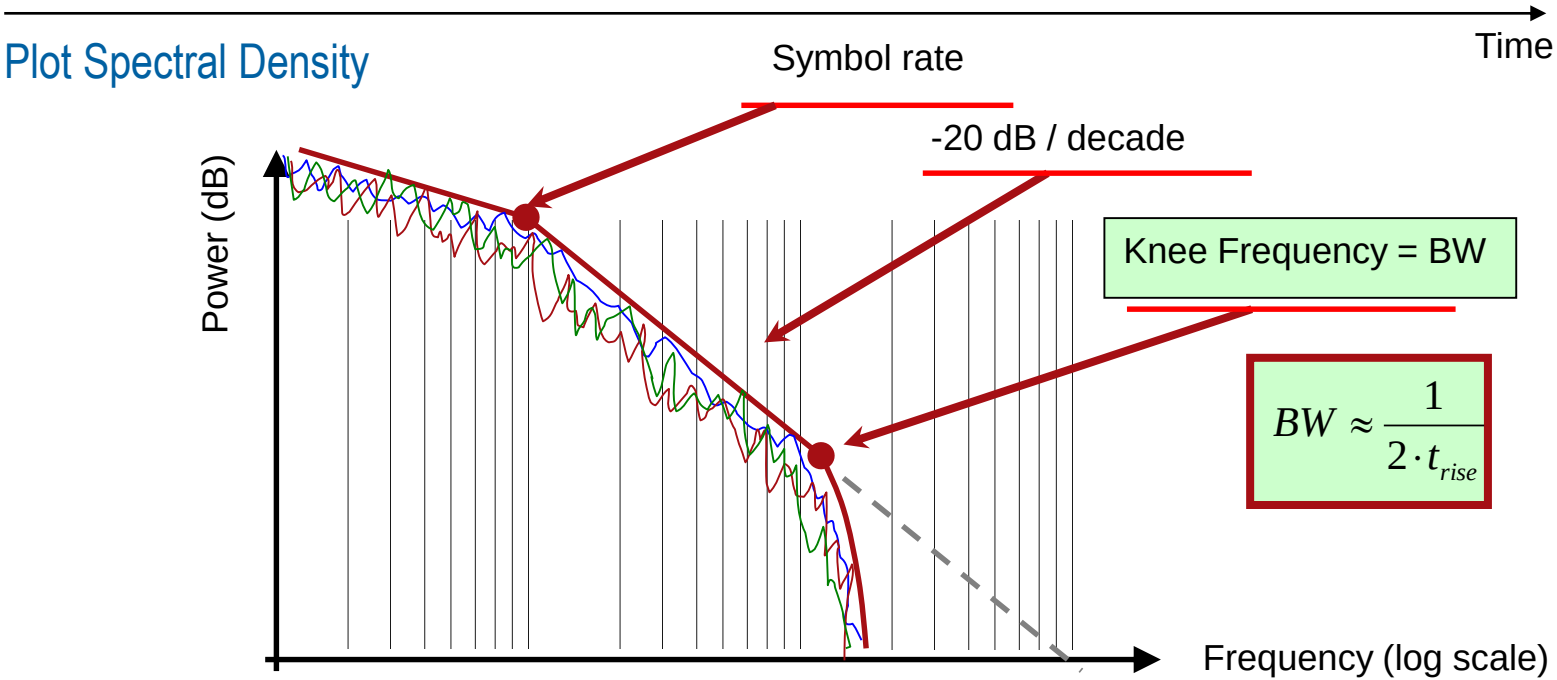




$$BW \approx \frac{1}{t_{symbol}} = Symbol\ rate$$

WHAT IS THE REQUIRED BW?

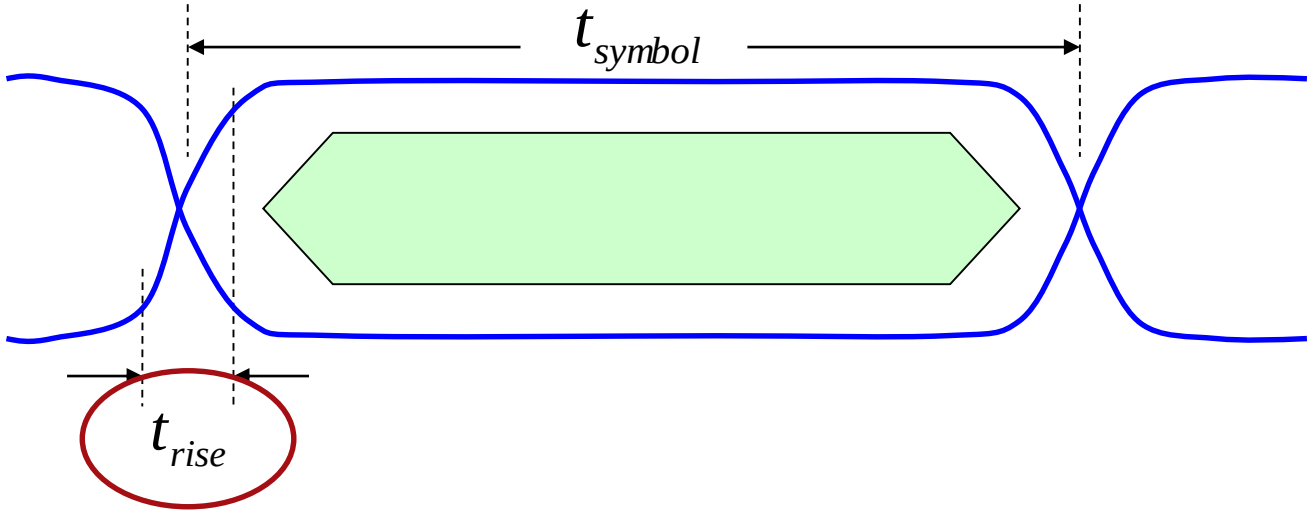
Actually



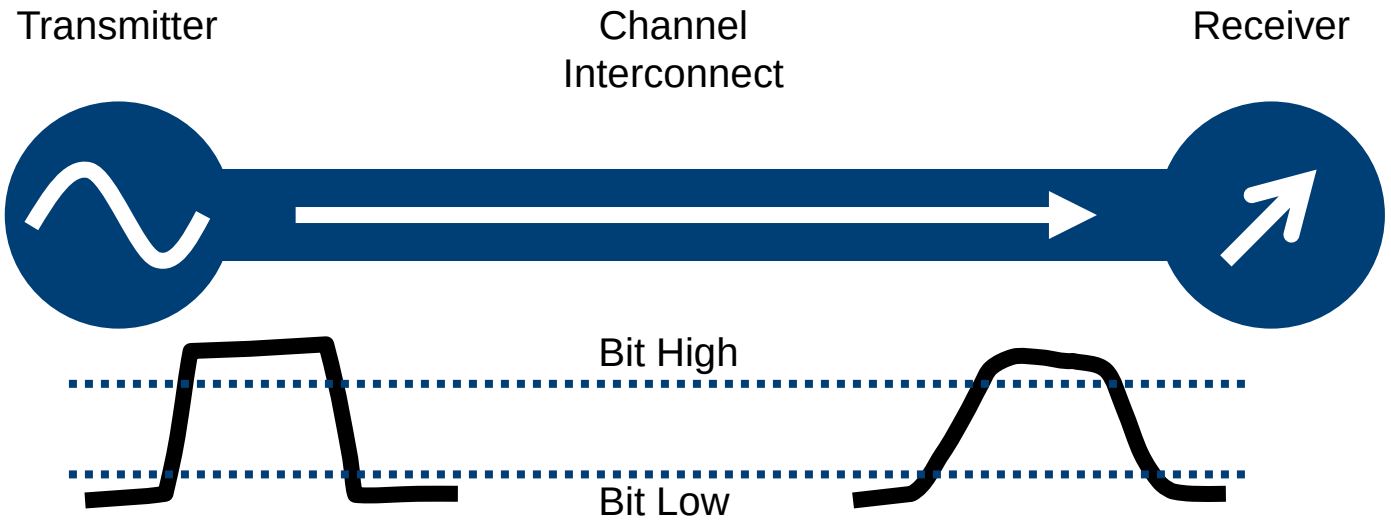
REQUIRED BW CALCULATION

- Transmitter's Rise Time is specified as 50 ps
- Estimate the require bandwidth

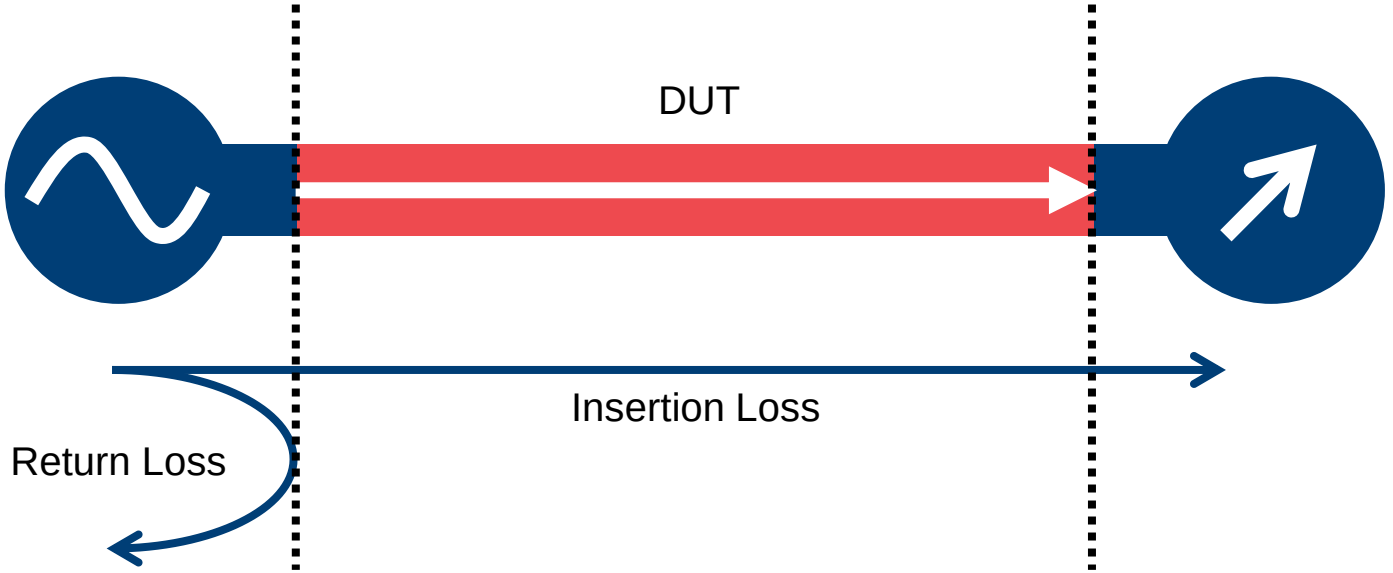
$$BW \approx \frac{1}{2 \cdot t_{rise}} = \frac{1}{100\,ps} = 10GHz$$



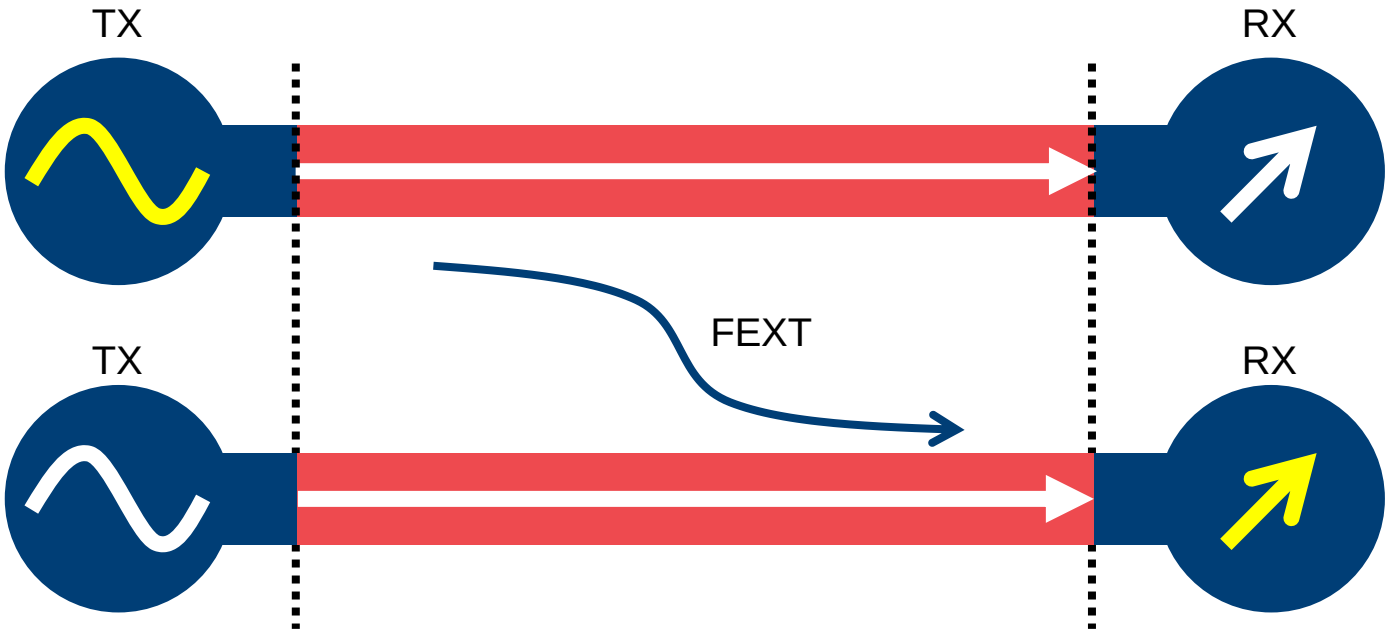
SIGNAL TRANSMISSION



SIGNAL INTEGRITY TEST REQUIREMENTS

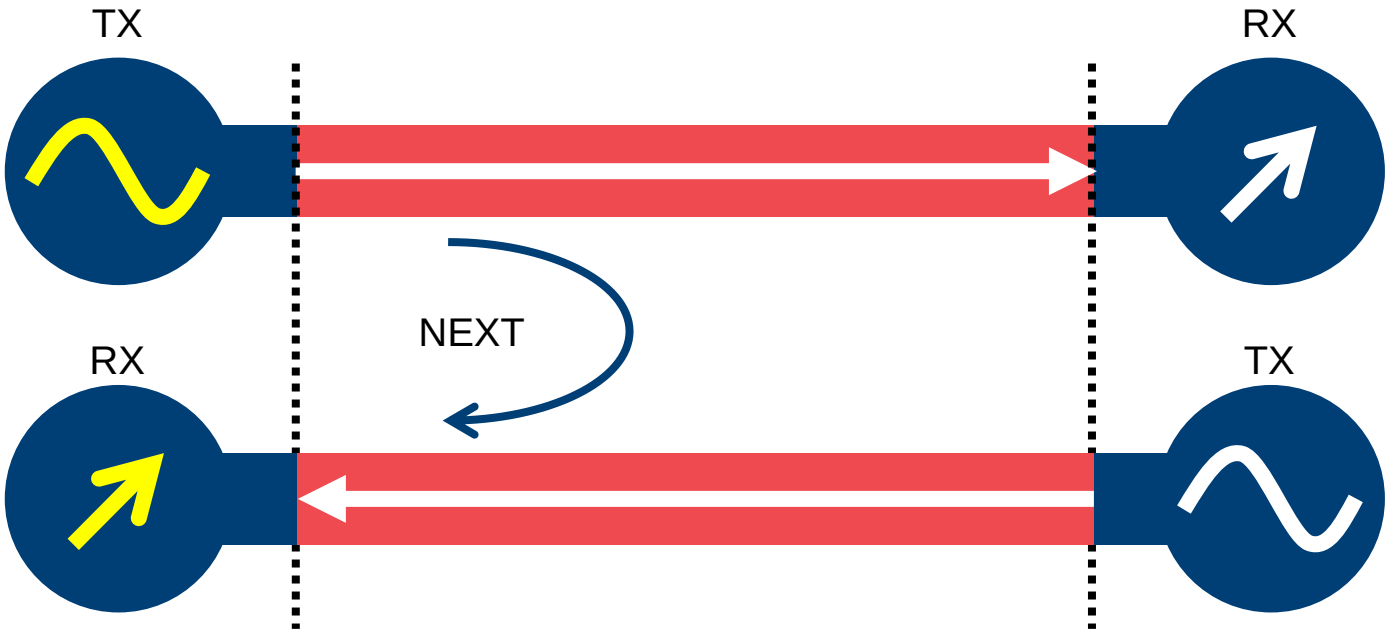


SIGNAL INTEGRITY TEST REQUIREMENTS



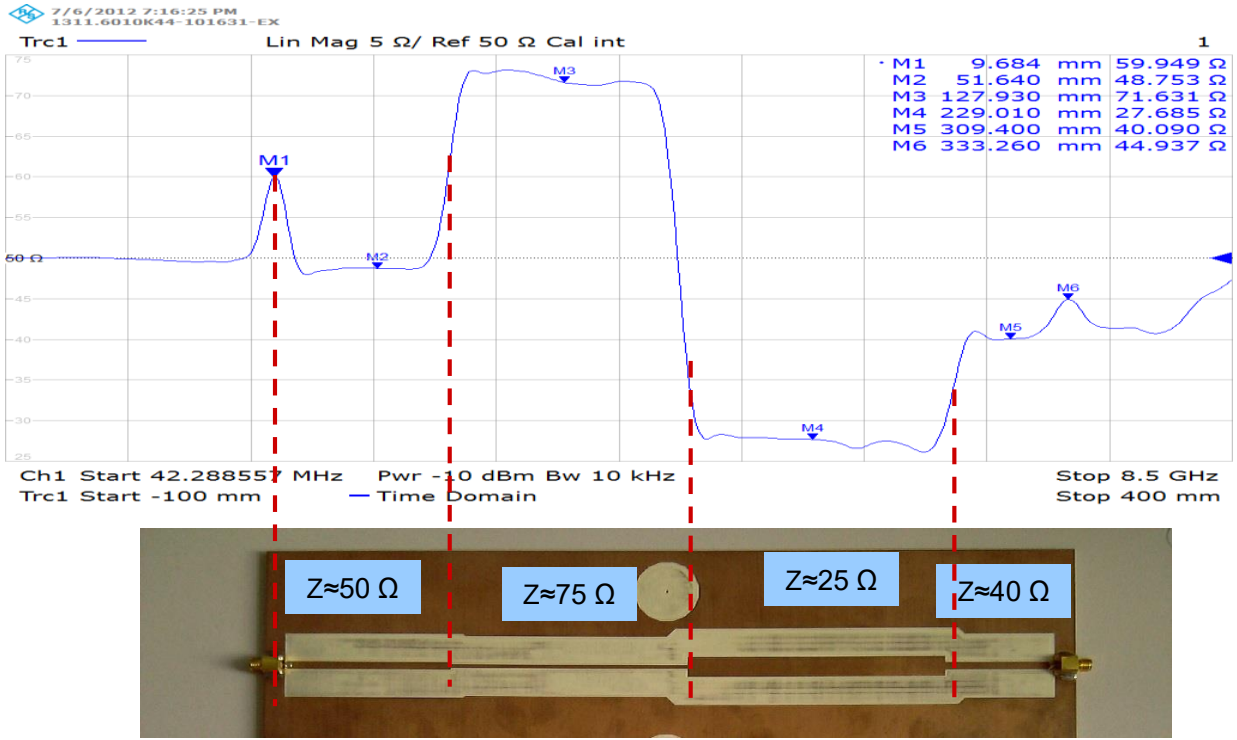
Far-End Crosstalk (FEXT)

SIGNAL INTEGRITY TEST REQUIREMENTS

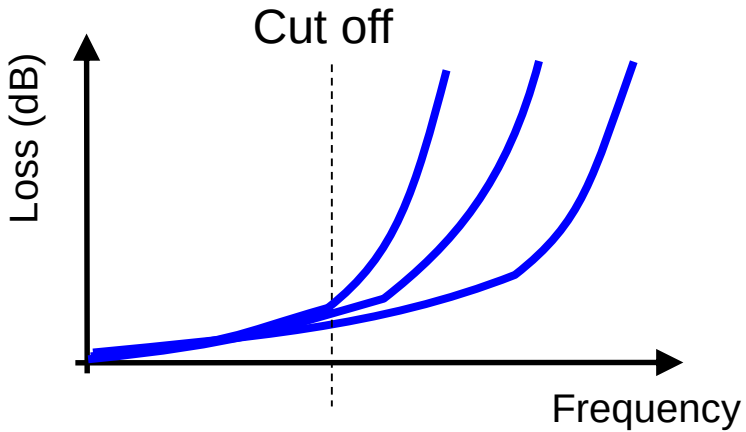


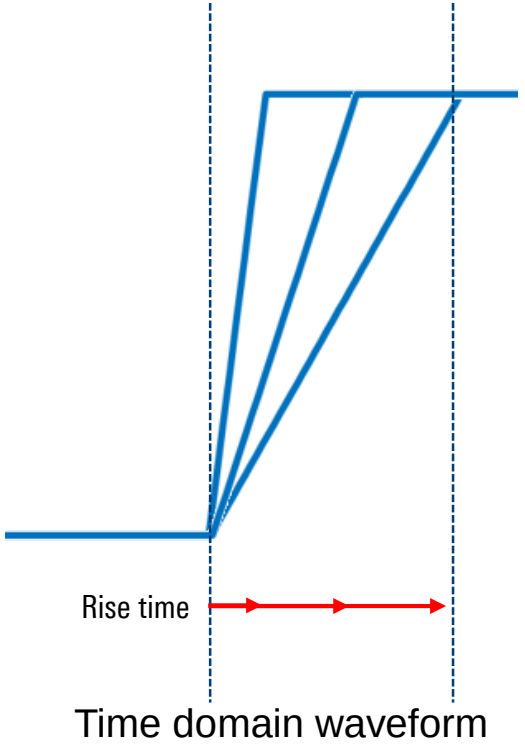
Near-End Crosstalk (NEXT)

TDR IMPEDANCE MEASUREMENT

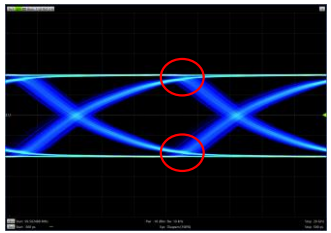


TDT RISE TIME





EYE DIAGRAM

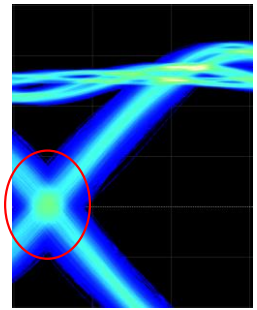


Emphasis

Generator

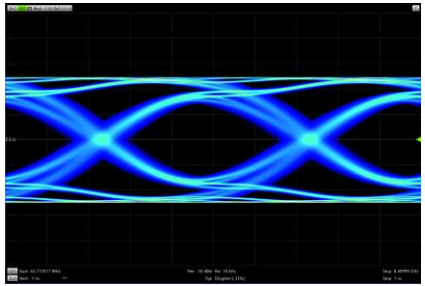
Channel

Receiver

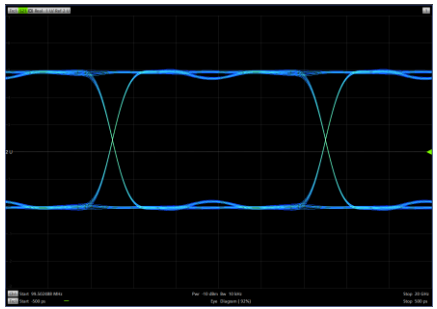


Jitter

Noise



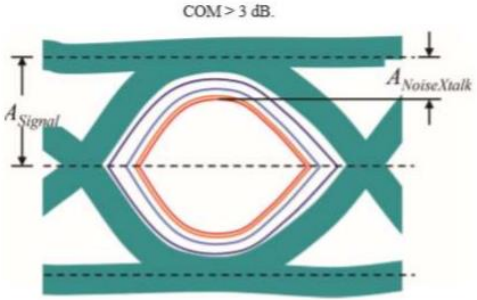
Distorted Channel

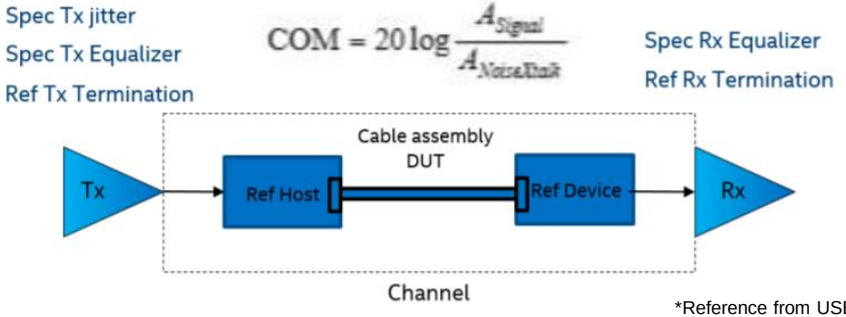


Equalization

EFFECTIVE RETURN LOSS (ERL) AND CHANNEL OPERATION MARGIN (COM)

- Effective Return Loss (ERL)
  - Return loss with receiver EQ
  - Transmitter noise
  - Receiver frequency response
- Channel Operation Margin (COM)
  - Insertion loss
  - Isolation for FEXT and NEXT
- Integrated Crosstalk Noise (ICN)
  - Effective voltage for power sum of NEXT and FEXT crosstalk
- Integrated Common-Mode Conversion Noise (ICMCN)
  - Effective voltage for power sum of Scd21

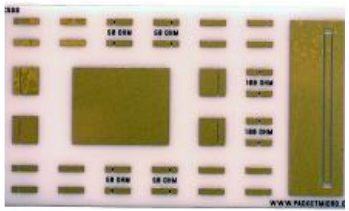


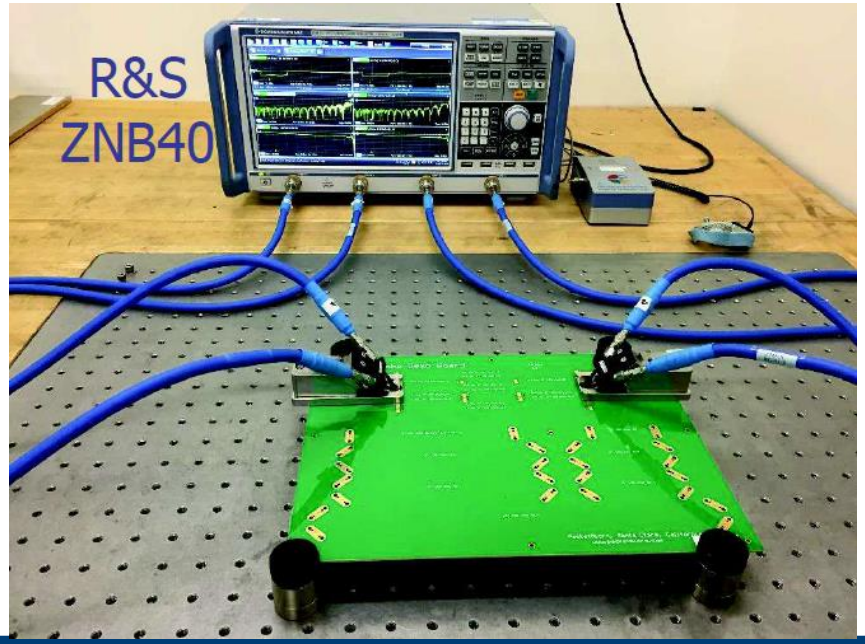


*Reference from USB-IF

ACCURATE MEASUREMENT WITH PROBES OR TEST FIXTURE

POSSIBLE SOLUTION: DIRECTLY PROBE THE DUT WITH RF MEASUREMENT PROBES



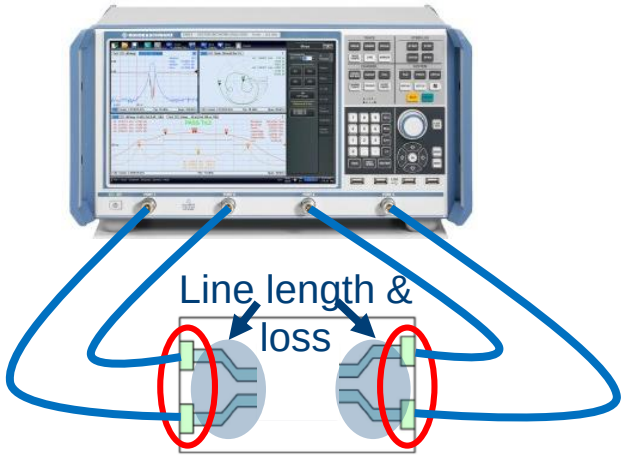


As an example using Packet Micro RF Probes.

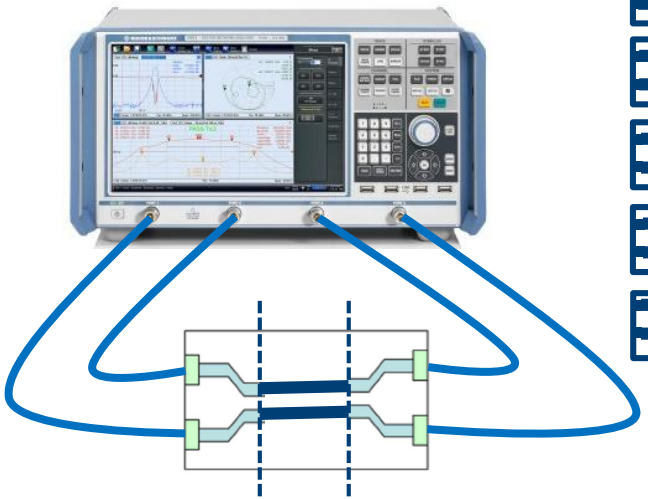
Required: S-Parameter of the RF probes

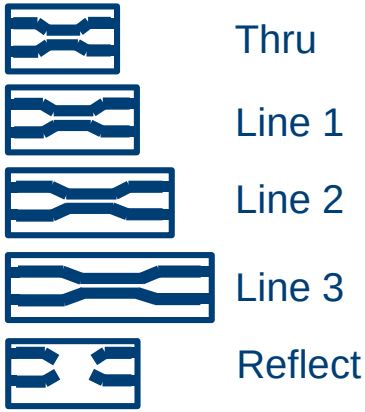
POSSIBLE SOLUTION: STANDARD FEATURE

Auto Length and Loss



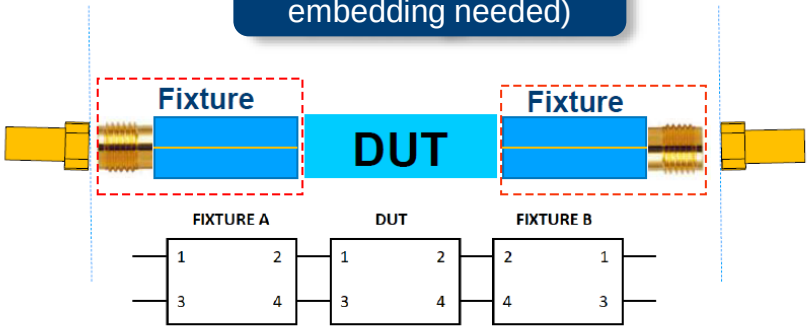
TRL Calibration





POSSIBLE SOLUTION: DE-EMEDDING SW ALGORITHMS

Fixture modeling (De-embedding needed)



Calibration plane
(end of Co-axial connector)

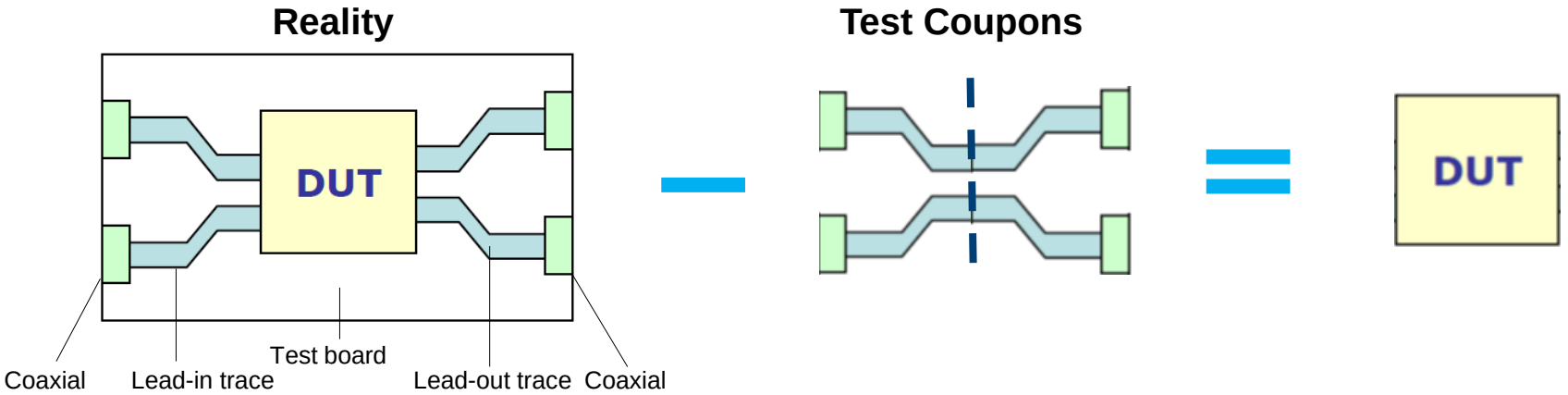
Calibration plane
(end of Co-axial connector)

Your measurement can easily be corrupted by improper fixture design. Even worse, you may not be aware of it!

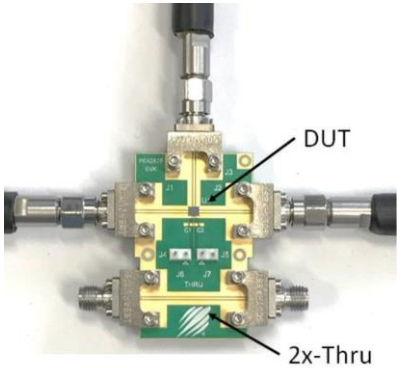
IEEE-P370 Objectives

Used of Beatty Standard to analyze de-embed quality

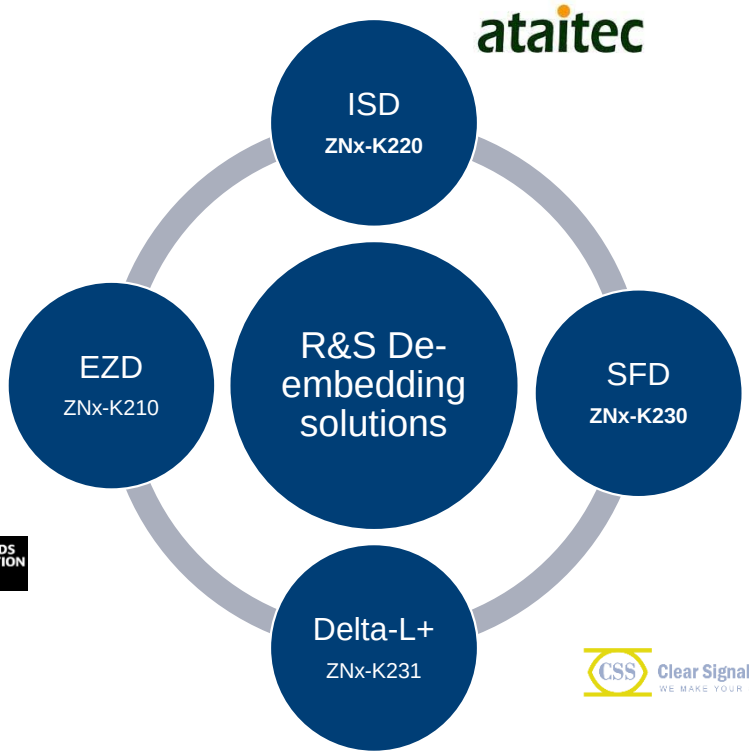
DE-EMBEDDING PRINCIPLE



- Test board + DUT
  - Fixture with lead-in + lead-out structure and DUT on it
- Test coupons
  - PCB with only lead-in + lead-out to form a through-like structure



R&S VNA TEST FIXTURE DE-EMBEDDING SOLUTION

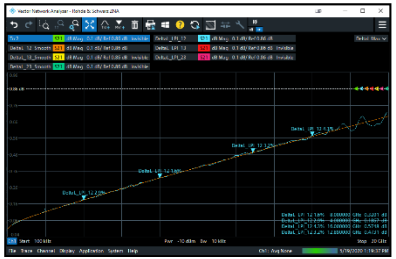


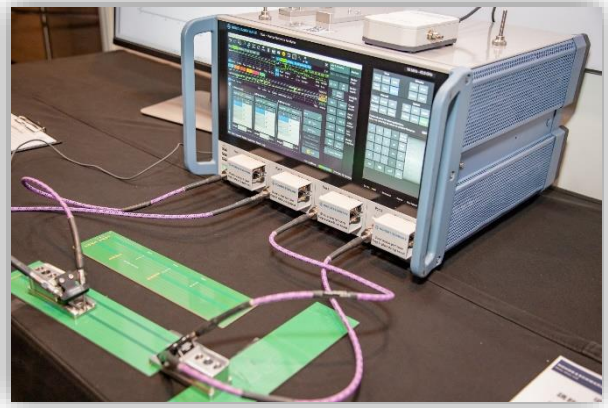
- Available for R&S ZNA / R&S ZNB R&S ZNBT / R&S ZND VNA models
- Industry accepted SW algorithms
  - IEEE P370 verified de-embedding tools: EZD, ISD, SFD
  - PCB Characterization: Delta-L V4.0
- Easy to use
  - One box solution
  - Workflow GUI
  - Full remote support

DELTA-L GUI EXAMPLE
SOLUTION WALKTHROUGH – OPTION ZNX-K231

- Press Offset Embed button, Delta-L calculation is a simple 3-step process:

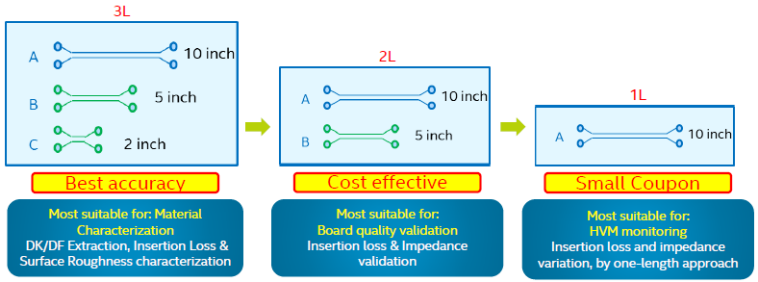
1. Delta-L setup
2. Measurement
3. Algorithm results





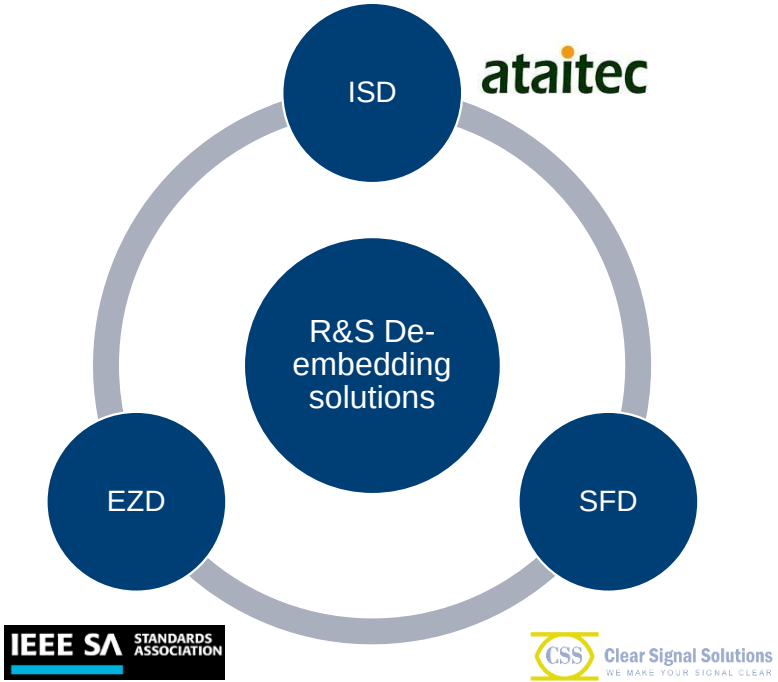
Delta-L V4.0 demo

- All of these steps can be operated via SCPI as well.



FIXTURE MODELING DE-EMBEDDING TECHNIQUES

R&S SOLUTION TEST FIXTURE DE-EMBEDDING

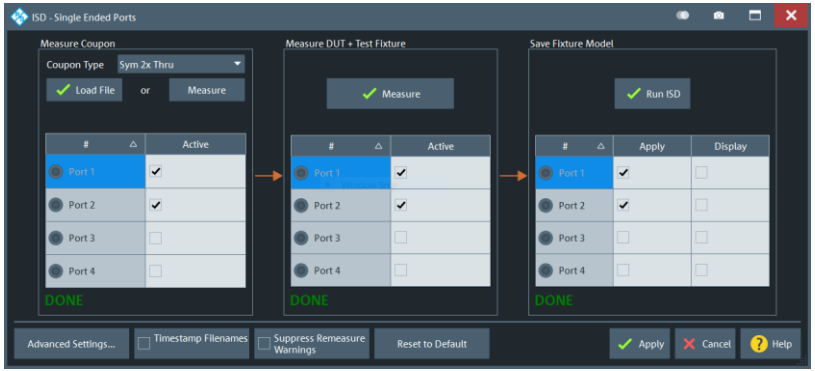


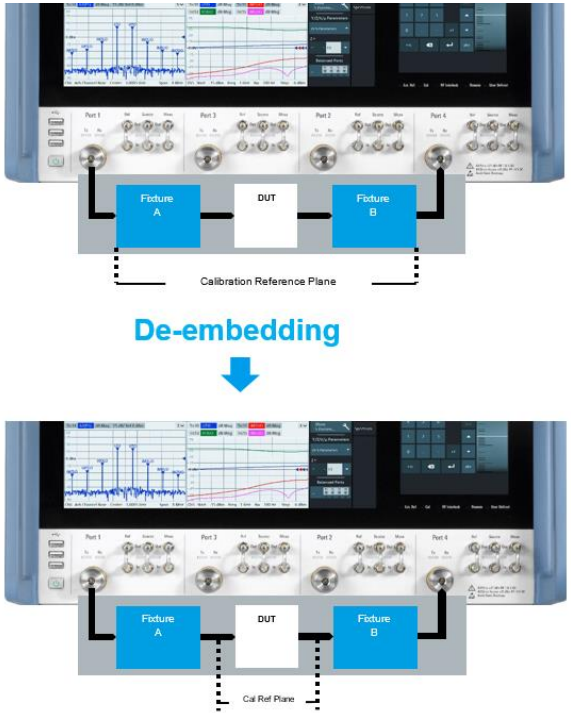
- Industry accepted SW algorithms
  - ISD: In-Situ De-embedding
  - SFD: Smart Fixture De-embedding
  - EZD: Eazy De-embedding

Test Coupon	ISD	SFD	EZD
2x Thru	●	●	●
1x Open	●	●	
1x Short	●	●	
1x Open + 1 x Short	●		

ISD GUI EXAMPLE

- Press Offset Embed button, ISD calculation is a simple 3-step process:
  1. Measure the 2x Thru
  2. Measure the total structure: DUT + test fixture
  3. Push the ‘Run ISD’ button and the VNA considers the algorithm results automatically
- All of these steps can be operated via SCPI as well.





ISD IMPEDANCE CORRECTION

CONCLUSIONS

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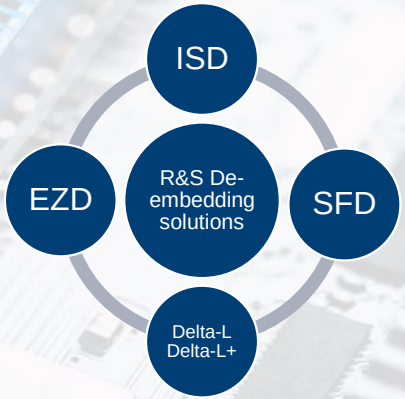
- Most popular interfaces such as USB4, PCIe, and 400/800G Ethernet produces signal integrity issues due to higher data rate achieved and higher bandwidth required.

- Signal integrity analysis for high speed interface measurement items covers
  - Frequency domain: return loss, insertion loss, NEXT, FEXT, mode conversion…
  - Time domain: TDR impedance, TDT rise time, TDT skew…
  - Signal domain: emphasis, jitter, noise, distorted channel, equalization, COM, ERL, ICN, ICMCN…

- R&S VNA offers de-embedding methods:
  - General de-embedding tools: EZD, ISD, SFD
  - PCB characterization: Delta-L V4.0



THANKS FOR YOUR ATTENTION