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The Future Trends of PCIe5 Cable Assemblies and Test Fixtures

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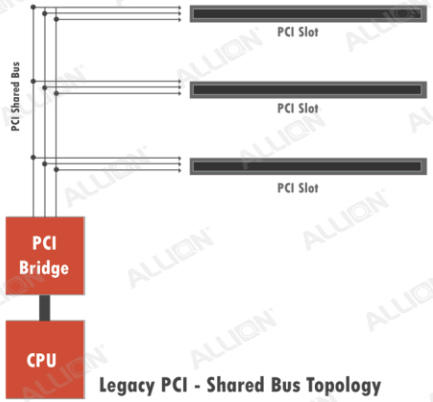
PCIe to PCIe 4.0的歷史

PCIe to PCIe 3.0

1. 2003年，PCIe 第一代問世，速率為2.5GT/s。
2. 2007年，2.0規格釋出，速率翻倍到5.0GT/s。
3. 2010年，PCIe 3.0並沒有翻倍到10GT/s, 而是來到了8GT/s：
   - 原先的Encoding(防止Cable線內DC電荷累積用編碼)由原來的8b/10b增加到128b/130b， 使得傳輸效率提高了一倍之多。
   - 128b/130b有較好的效率之外可靠度也比8b/10b高。
   - 3.0以8GT/s替代10GT/s ，是屬於策略性的改變。
   - 3.0發展成低功耗傳輸的互連架構。

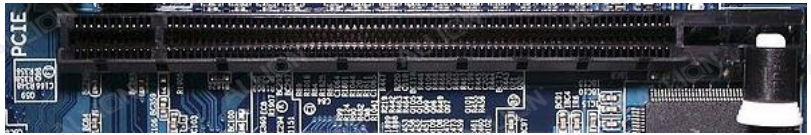
Source: Wikipedia



Source: Wikipedia

PCIe 4.0

1. 2017年PCIe4.0速率到達16GT/s。
2. **低功耗**與**低成本**也是規格重點。



Source: Wikipedia

3. 傳輸速率開始受限於PCB的物理材料特性。

   解決方式：

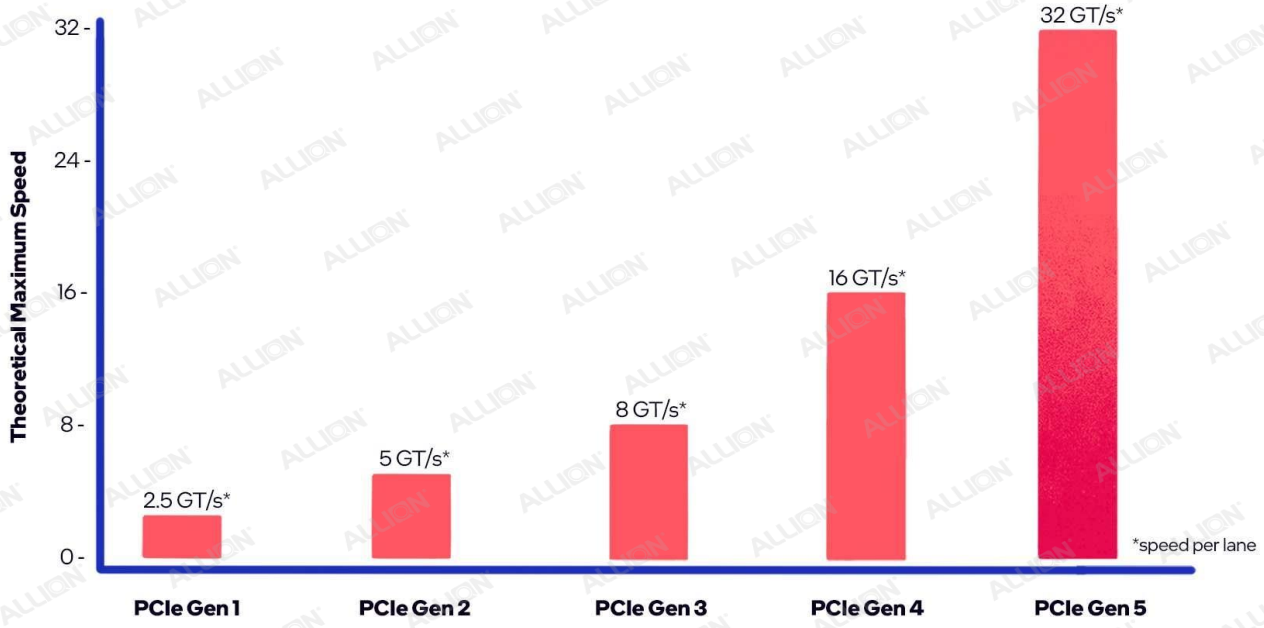
   a. 使用色散小的電路板，例如 Magtron4 或 6 或是 Rogers RO4350B

   b. 在物理層(Physical Layer)增加Re-timer

4. 利用強大的**資料交換功能**，增強了RAS --- 可靠性(Reliability)、可用性(Availability)與可維護性(Serviceability)

進入PCIe 5.0

PCIe 5.0



PCIe 5.0

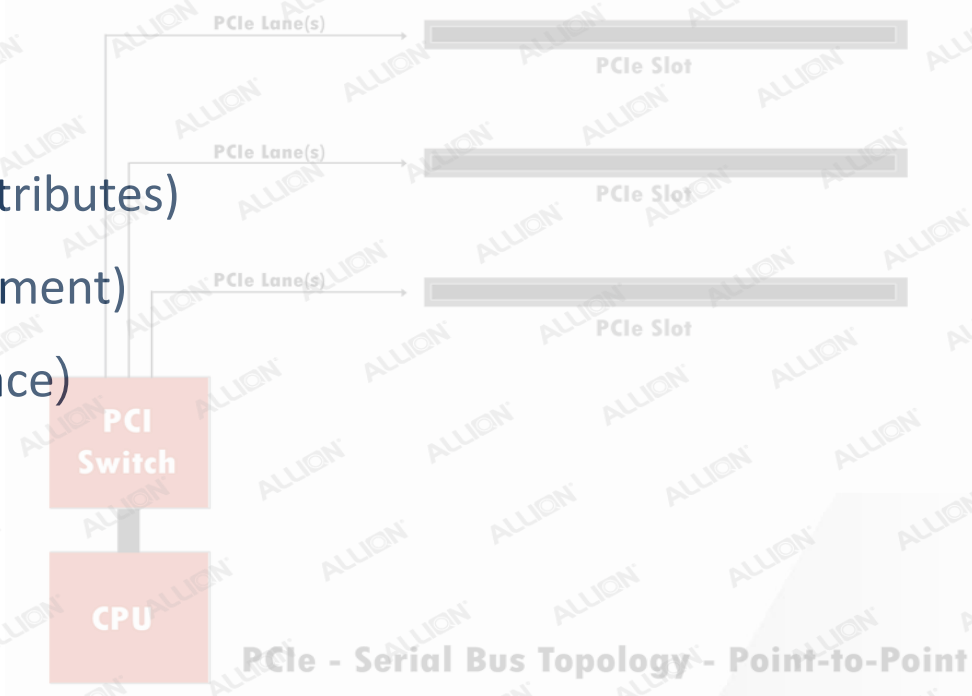
1. 2019年PCIe5.0規格問世，速率再從16GT/s翻倍到32GT/s。
2. 進入了高速應用的另一個里程碑：
    a. 機器人學習 (Machine Learning)
    b. 邊際運算 (Edge Computing)
    c. AI人工智慧
    d. 雲端
    e. 其他
3. 除了運算速率變高，儲存容量與存取頻寬需求也跟著上升。

PCIe 5.0

	PCIe 4.0	PCIe 5.0
Data Rate	16 GT/s	32 GT/s
Modulation Scheme	NRZ	
Bit Encoding Scheme	128B/130B	
Channel Loss	-27 ~ -30 dB	-34 ~ -37 dB
Common Clock (RefClk) Phase Jitter	≦0.5 ps rms	≦0.15 ps rms
Transmitter Equalization	3-Tap FFE	
Ref. Receiver CTLE	2-pole, 1-zero, adjustable gain in 1 dB steps from -1 to -9 dB	4-pole, 2-zeros, adjustable gain in 1 dB steps from -5 to -15 dB
Ref. Receiver DFE	2-Tap DFE	3-Tap DFE
Minimum Post Eq EH12	15 mV	15 mV
Minimum Post Eq EW12	18.75 ps	9.375 ps
BER	$\leq 2.5 \times 10^{-13}$	
Eye at Receiver Input	Closed	

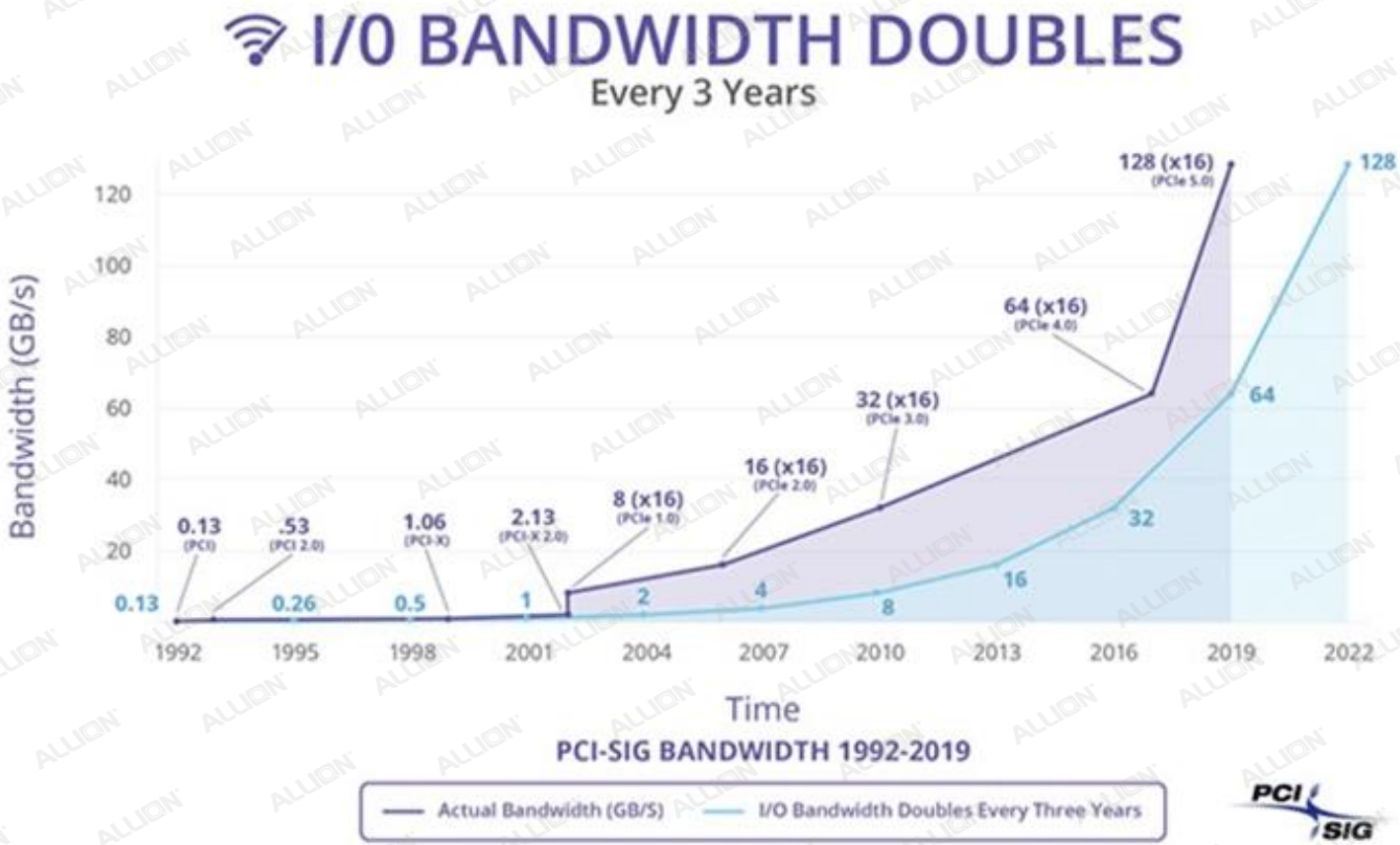
PCIe 5.0

- 5.0規範中定義：
  - 架構 (architecture)
  - 互聯屬性規範(interconnect attributes)
  - 網路結構管理 (fabric management)
  - 編程介面(programming interface)



Source: Wikipedia

PCIe 5.0



Internal Cable Assemblies

Internal Cable需求趨勢的形成：

PCIe在電腦以及大型網路儲存系統無所不在的原因：

1. 提升電腦內部匯流排的速度。
2. 更高頻寬的串列傳輸系統。(x1, x4, x8, x16, 再搭配更高的傳輸速度GT/s)
3. 通用性。它對於軟體開發者完全透明。
4. 能增強系統效能。
5. NVMe SSD用了PCIe標準。

Internal Cable需求趨勢的形成：

6. 從PCIe 4.0開始，一般的PCB無法滿足遠距離傳輸 (>25cm) 的需求
7. 供電提升至375W (150W x 2 + 75W)

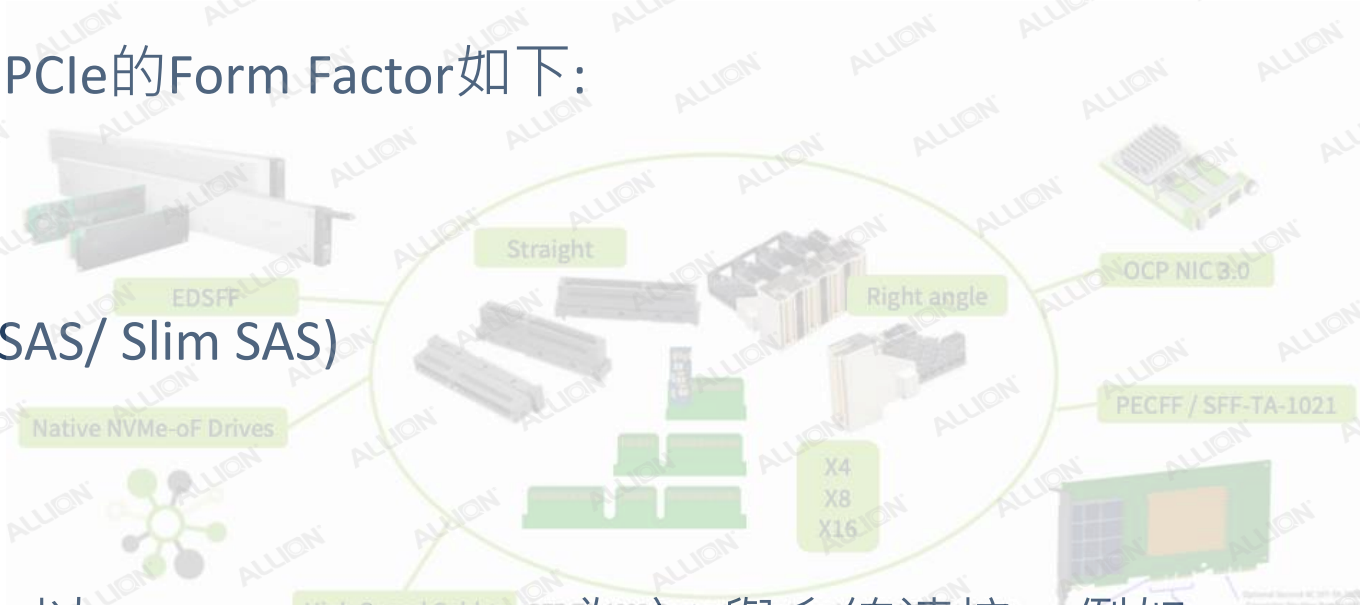
6-pin Power Connector (75W)		8-pin Power Connector (150W)	
1	+12V	1	+12V
2	Non	2	+12V
3	+12V	3	+12V
4	GND	4	Sense1
5	Sense	5	GND
6	GND	6	Sense0
		7	GND
		8	GND

Internal Cable Assemblies

- Internal Cable的Form Factor必須注意以下特性：
  - 良好的高頻SI特性
  - 耐高溫、高電壓、高電流、體積小
- Internal Cable的Raw Cable必須注意以下特性：
  - 溫度的穩定性
  - 抗EMI、Crosstalk
  - 折彎的穩定性
  - 不影響電氣效能的情況下實現高度彎曲和折疊

Internal Cable Assemblies

- 目前可以傳輸PCIe的Form Factor如下:
  - PCIe
  - M.2
  - U.2
  - SAS (mini SAS/ Slim SAS)
  - OCuLink
  - MCIO
  - Gen-Z



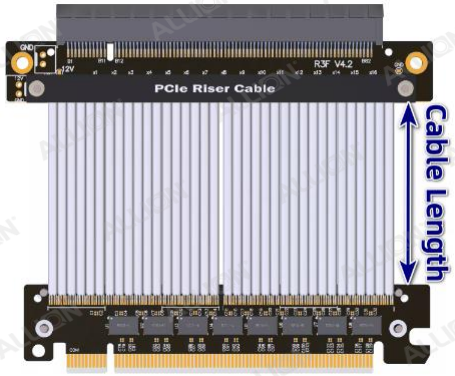
- 小型的Storages以narrow link(x 2、x4 為主) 與系統連接，例如M.2。
- Server則以PCIe x8 與 x16作為介面，而以Cable Assemblies分散至各個儲存單元則以x4 或 x 8為主。

Source: SNIA

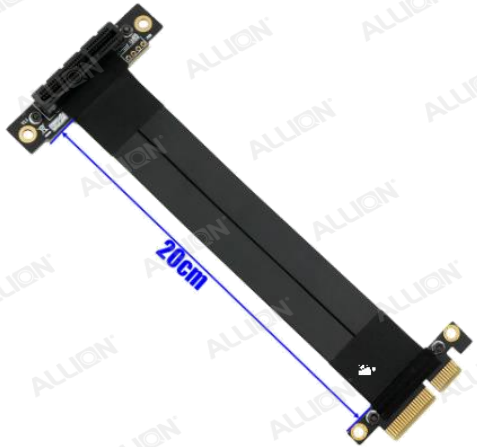
Riser Cable Assemblies 特性

- 卓越的信號完整性
  - Impedance: 85+/-10% 歐姆
  - FEXT & NEXT Power Sum: 40dB up to 25GHz
  - 符合PCIe to CEM Compliant
- 堅固的機械結構
  - 線纜有好的彎曲表現
  - 系統獲得好的散熱表現
  - 能提供靈活的各種應用

Riser Cable Assemblies



Riser Cable PCIe x 16
Source: www.aliexpress.com



Riser Cable PCIe x 4
Source: www.aliexpress.com

Riser Cable PCIe x 4 to M.2 NGFF NVMe M
Source: www.amazon.com

Riser Cable PCIe x 4 to U.2 NVMe SSD
Source: www.performance-pcs.com

Internal Cable Assemblies

- Server的儲存單元，主流以MCIO(Mini Cool Edge IO) 與 Gen-Z 為主。
  下列是MCIO與Gen-Z的尺寸:

	MCIO, 8i	Gen-Z, (1C)
Pitch (mm)	0.6	0.6
Contacts	74	56
Wide(mm)	31.6	28

MCIO Plug 8i, Source: IAT, www.iatconn.com

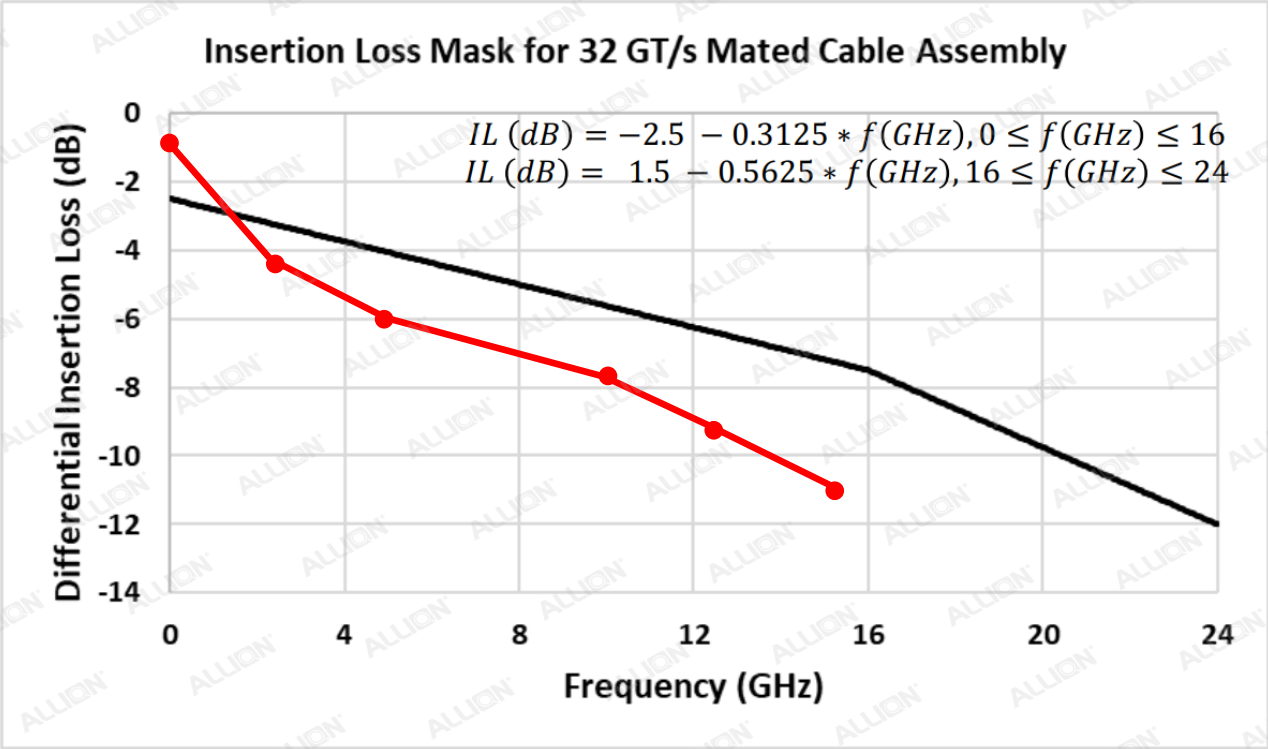
Gen-Z Plug 1C, Source: IAT, www.iatconn.com

PCIe Cable的量測與治具

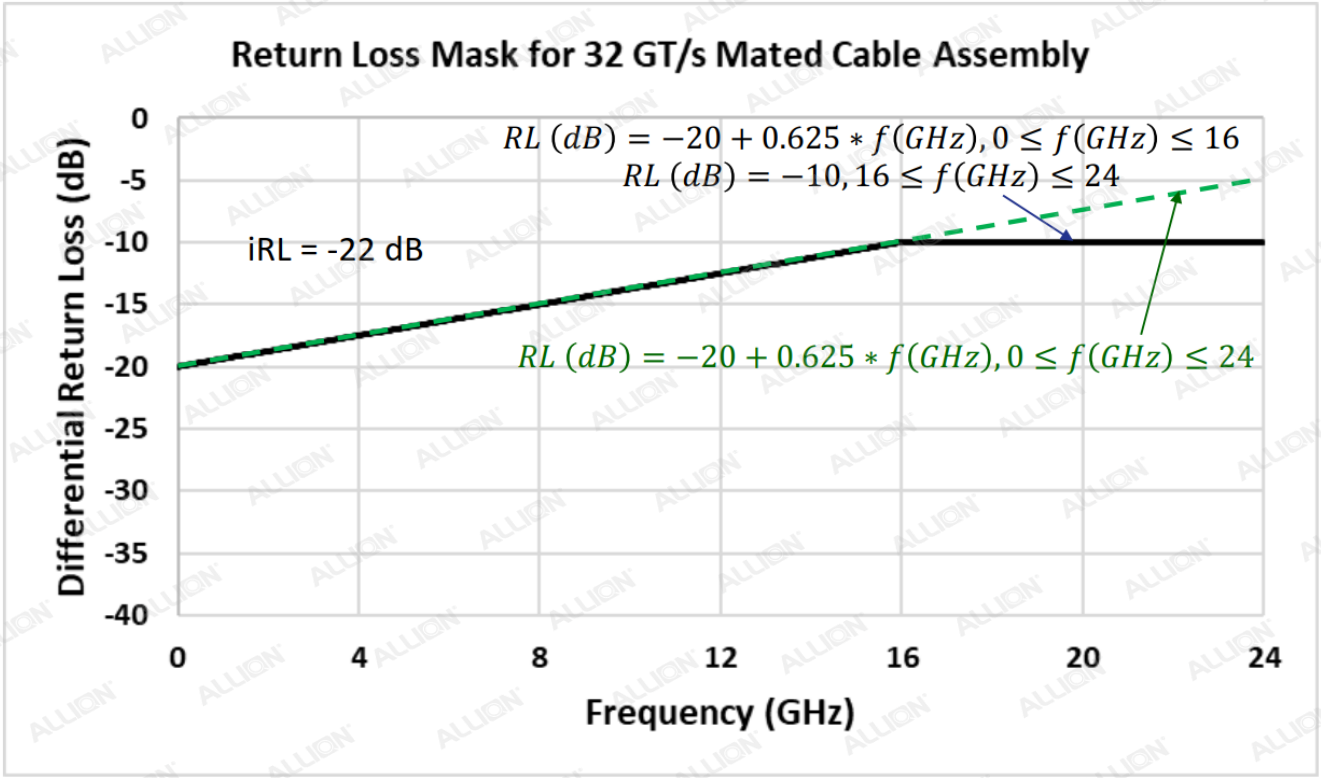
Internal Cable Specification

- 依據PCIe **5.0/6.0** v0.7 Internal Cable Specification文件
- 量測S-Parameter(DC to 24GHz) :
  - Insertion Loss
  - Return Loss
  - PSNEXT
  - PSFEXT
  - Effective Intra-Pair Skew (EIPS)
- 量測前，須將治具上的Trace以及PCIe Receptacle特性做**de-embedded.**

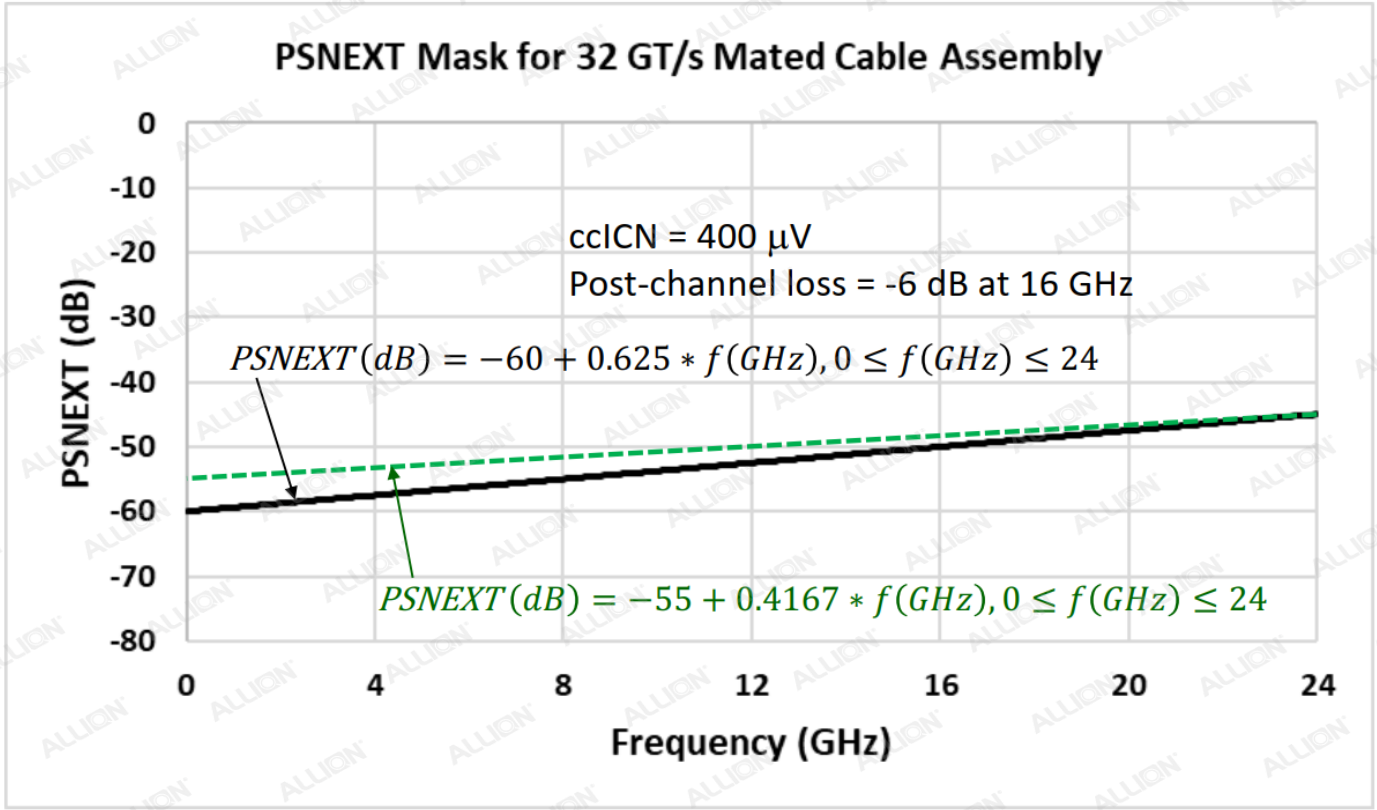
Insertion Loss



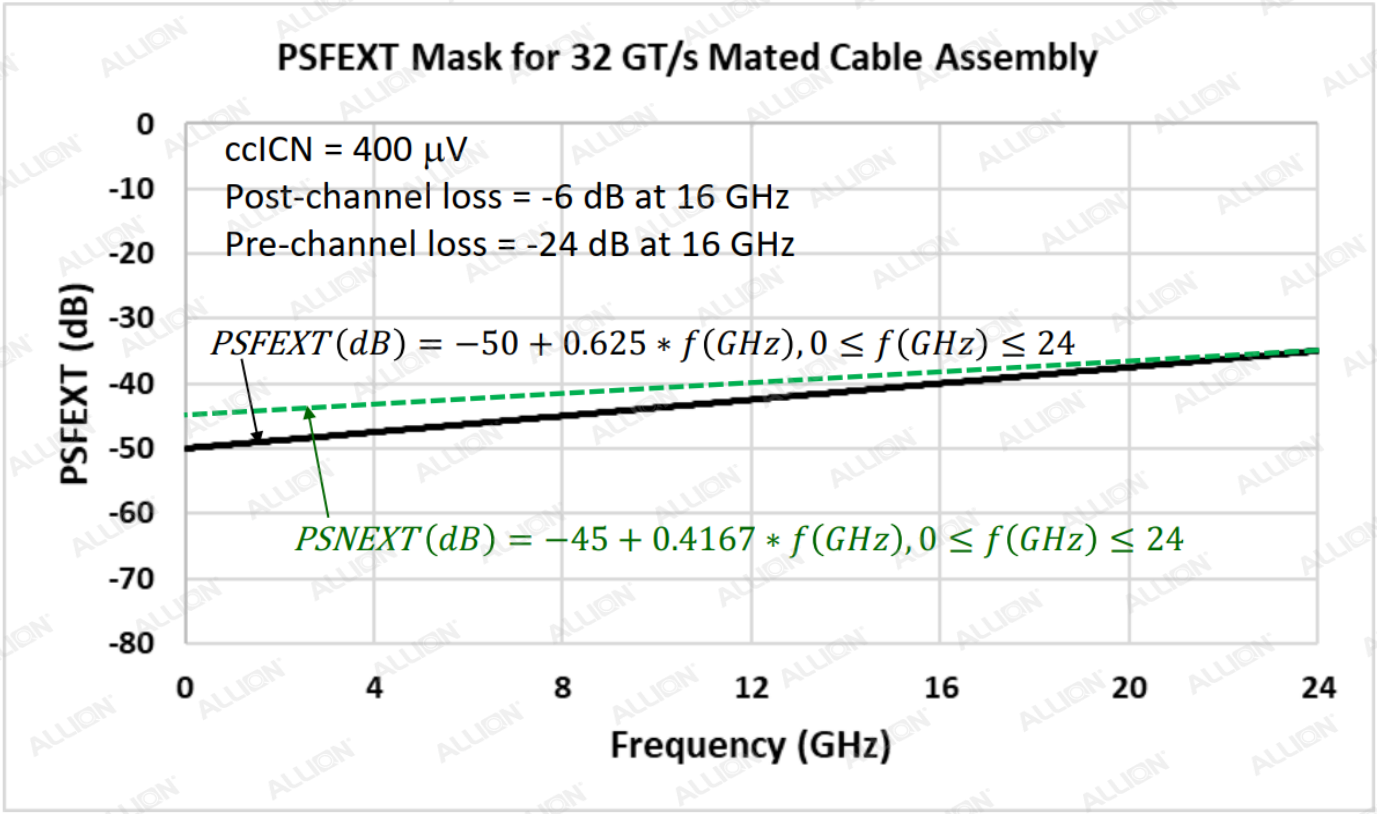
Return Loss



PSNEXT



PSFEXT



Effective Intra-Pair Skew (EIPS)

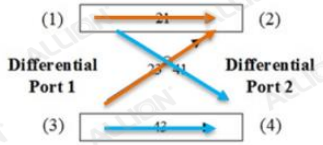
1. Frequency-domain Skew

(EIPS) < 4 ps

The modified mixed-mode insertion loss can be represented by the single-ended S-parameter equations:

$$S2d1 = 1/\sqrt{2} \cdot (Sdd21 + Scd21) = 1/\sqrt{2} \cdot (S21 - S23)$$

$$S4d1 = 1/\sqrt{2} \cdot (Sdd21 - Scd21) = 1/\sqrt{2} \cdot (S43 - S41)$$



The skew can be obtained by calculating the difference between the two phase delays

$$\Delta t_1 = \text{-unwrap (phase } (S2d1))/\ (2\pi f)$$

$$\Delta t_2 = \text{-unwrap (phase } (S4d1))/\ (2\pi f)$$

$$skew(f) = \Delta t_1(f) - \Delta t_2(f)$$

2. Integration of the magnitude of skew after multiplying weighting funciton

$$EIPS = \int_{fmin}^{fmax} W(f) \cdot |skew(f)| df = df \sum_{k=1}^{N_{max}} W(k \cdot df) \cdot |skew(k \cdot df)|$$

where

$$W(f) = \frac{|db(S_{cd21,ave\ skew}) - db(S_{cd21,0skew})| \cdot PSD}{\int_{fmin}^{fmax} |db(S_{cd21,ave\ skew}) - db(S_{cd21,0skew})| \cdot PSD df}$$

$$|Scd21|_{0psec\ skew} = 1/2 \cdot (S21 - S23 + S41 \cdot \exp(j2\pi f \cdot skew(f)) - S43 \cdot \exp(j2\pi f \cdot skew(f)))$$

$$|Scd21|_{ave\ skew} = 1/2 \cdot (S21 - S23 + S41 \cdot \exp(j2\pi f \cdot (skew(f) - skew_{ave})) - S43 \cdot \exp(j2\pi f \cdot (skew(f) - skew_{ave}))$$

$$skew_{ave} = average(|skew(f)|)$$

$$PSD = sinc(\frac{f}{f_b})^2 \cdot \frac{1}{1+(f/f_r)^8} \cdot \frac{1}{1+(f/f_t)^4}$$

Lane-to-Lane Skew

Lane-to-Lane Skew for PCIe 5.0 32 GT/s: Mated Cable Assembly

- Lane-to-Lane Skew < 200 ps for max cable length of 1000mm

Test Fixture

- 依據PCI Express Card Electromechanical Specification Revision 5.0 的CEM製作。
- 確認Receptacle 合乎規範。
- 確認Plug合乎規範。
- 擷取Receptacle的S2p作為量測Cable Assembly的 de-embedded檔案。
- PCIe 5.0 CEM的NEXT量測手法與PCIe 4.0不同，且需要多加測FEXT。

Insertion Loss

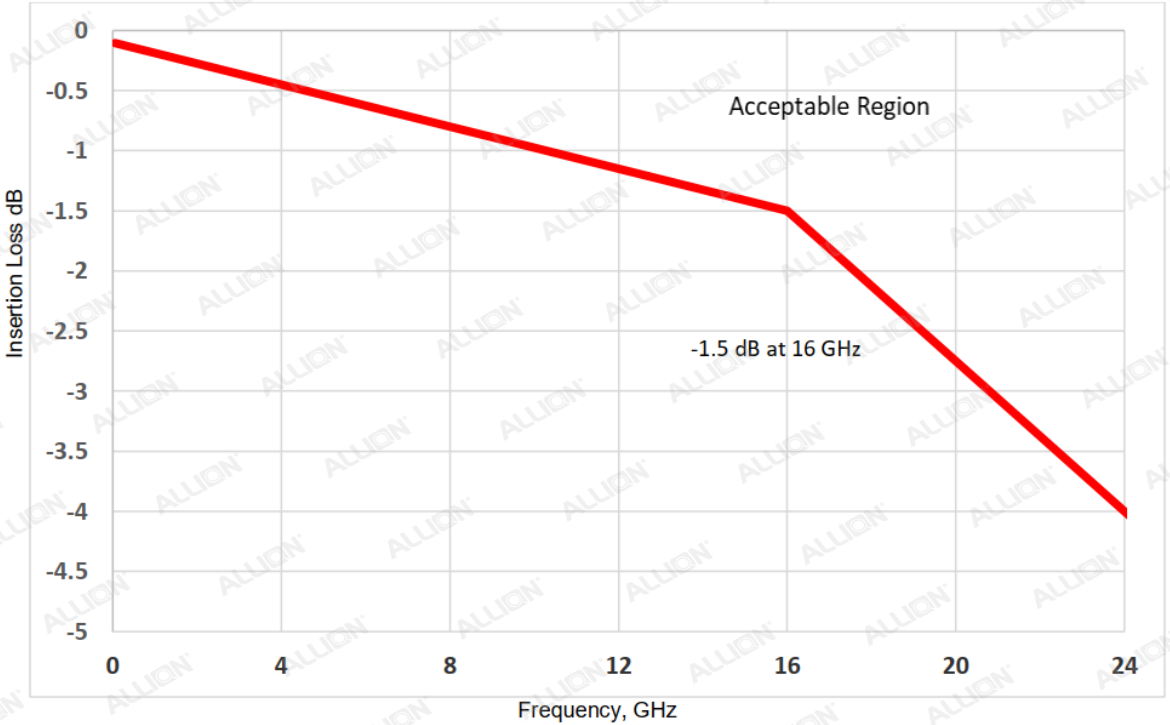


Figure 6-12. Differential Insertion Loss Limits for 32.0 GT/s Operation

Return Loss

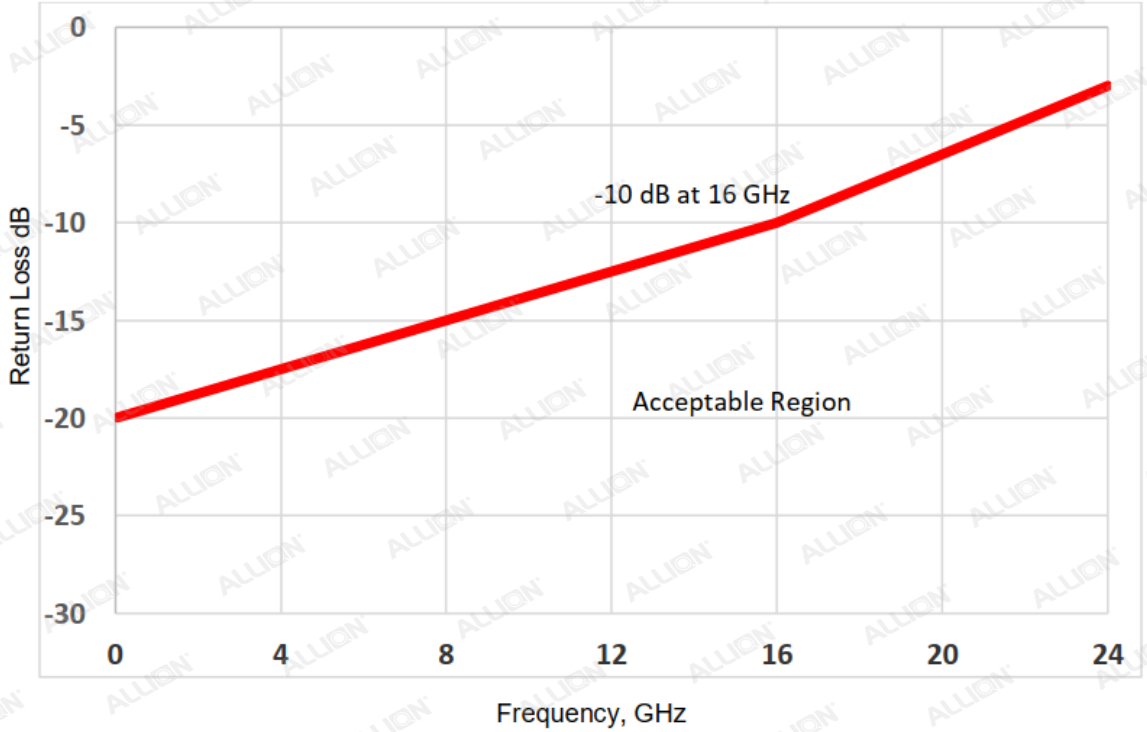
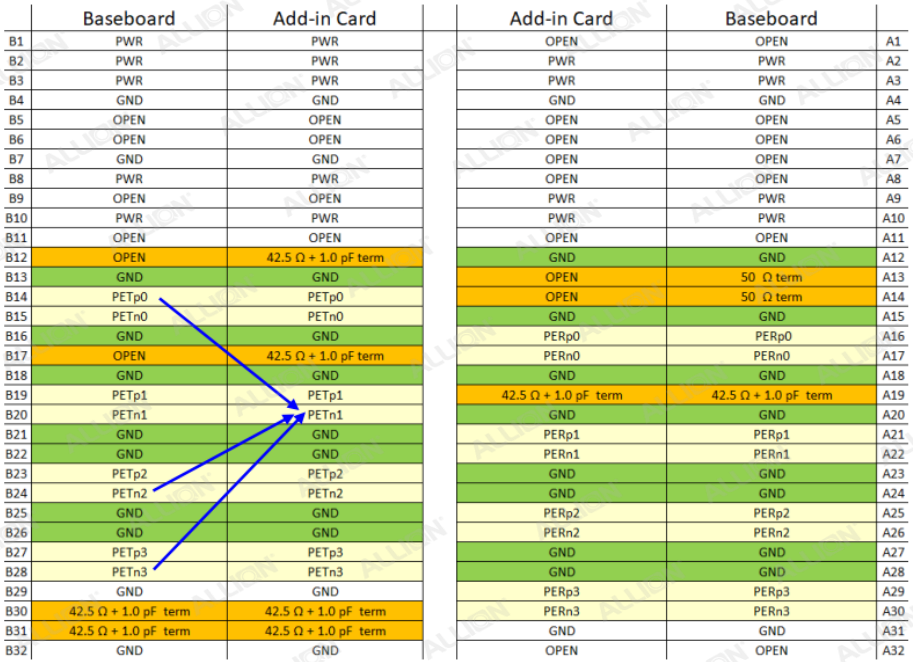


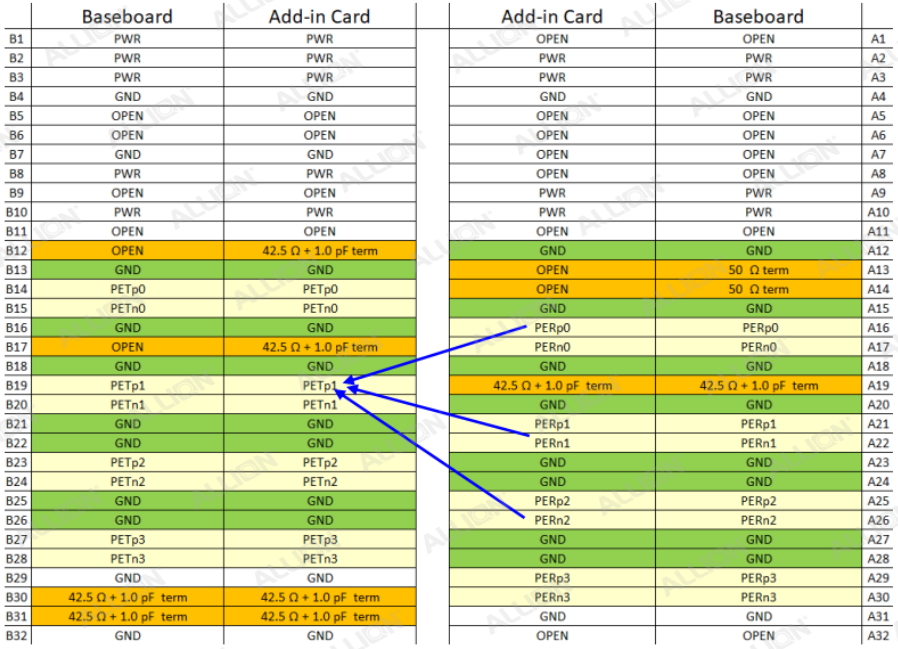
Figure 6-13. Differential Return Loss Limits for 32.0 GT/s Operation

Cross Talk - NEXT, FEXT 量測對應圖



	Baseboard	Add-in Card	Add-in Card	Baseboard	
B1	PWR	PWR	OPEN	OPEN	A1
B2	PWR	PWR	PWR	PWR	A2
B3	PWR	PWR	PWR	PWR	A3
B4	GND	GND	GND	GND	A4
B5	OPEN	OPEN	OPEN	OPEN	A5
B6	OPEN	OPEN	OPEN	OPEN	A6
B7	GND	GND	OPEN	OPEN	A7
B8	PWR	PWR	OPEN	OPEN	A8
B9	OPEN	OPEN	PWR	PWR	A9
B10	PWR	PWR	PWR	PWR	A10
B11	OPEN	OPEN	OPEN	OPEN	A11
B12	OPEN	42.5 Ω + 1.0 pF term	GND	GND	A12
B13	GND	GND	OPEN	50 Ω term	A13
B14	PETp0	PETp0	OPEN	50 Ω term	A14
B15	PETn0	PETn0	GND	GND	A15
B16	GND	GND	PERp0	PERp0	A16
B17	OPEN	42.5 Ω + 1.0 pF term	PERn0	PERn0	A17
B18	GND	GND	GND	GND	A18
B19	PETp1	PETp1	42.5 Ω + 1.0 pF term	42.5 Ω + 1.0 pF term	A19
B20	PETn1	PETn1	GND	GND	A20
B21	GND	GND	PERp1	PERp1	A21
B22	GND	GND	PERn1	PERn1	A22
B23	PETp2	PETp2	GND	GND	A23
B24	PETn2	PETn2	GND	GND	A24
B25	GND	GND	PERp2	PERp2	A25
B26	GND	GND	PERn2	PERn2	A26
B27	PETp3	PETp3	GND	GND	A27
B28	PETn3	PETn3	GND	GND	A28
B29	GND	GND	PERp3	PERp3	A29
B30	42.5 Ω + 1.0 pF term	42.5 Ω + 1.0 pF term	PERn3	PERn3	A30
B31	42.5 Ω + 1.0 pF term	42.5 Ω + 1.0 pF term	GND	GND	A31
B32	GND	GND	OPEN	OPEN	A32

Figure 6-11. Differential Far End Crosstalk Victim-Aggressor Pattern for 32.0 GT/s Operation



	Baseboard	Add-in Card	Add-in Card	Baseboard	
B1	PWR	PWR	OPEN	OPEN	A1
B2	PWR	PWR	PWR	PWR	A2
B3	PWR	PWR	PWR	PWR	A3
B4	GND	GND	GND	GND	A4
B5	OPEN	OPEN	OPEN	OPEN	A5
B6	OPEN	OPEN	OPEN	OPEN	A6
B7	GND	GND	OPEN	OPEN	A7
B8	PWR	PWR	OPEN	OPEN	A8
B9	OPEN	OPEN	PWR	PWR	A9
B10	PWR	PWR	PWR	PWR	A10
B11	OPEN	OPEN	OPEN	OPEN	A11
B12	OPEN	42.5 Ω + 1.0 pF term	GND	GND	A12
B13	GND	GND	OPEN	50 Ω term	A13
B14	PETp0	PETp0	OPEN	50 Ω term	A14
B15	PETn0	PETn0	GND	GND	A15
B16	GND	GND	PERp0	PERp0	A16
B17	OPEN	42.5 Ω + 1.0 pF term	PERn0	PERn0	A17
B18	GND	GND	GND	GND	A18
B19	PETp1	PETp1	42.5 Ω + 1.0 pF term	42.5 Ω + 1.0 pF term	A19
B20	PETn1	PETn1	GND	GND	A20
B21	GND	GND	PERp1	PERp1	A21
B22	GND	GND	PERn1	PERn1	A22
B23	PETp2	PETp2	GND	GND	A23
B24	PETn2	PETn2	GND	GND	A24
B25	GND	GND	PERp2	PERp2	A25
B26	GND	GND	PERn2	PERn2	A26
B27	PETp3	PETp3	GND	GND	A27
B28	PETn3	PETn3	GND	GND	A28
B29	GND	GND	PERp3	PERp3	A29
B30	42.5 Ω + 1.0 pF term	42.5 Ω + 1.0 pF term	PERn3	PERn3	A30
B31	42.5 Ω + 1.0 pF term	42.5 Ω + 1.0 pF term	GND	GND	A31
B32	GND	GND	OPEN	OPEN	A32

Figure 6-10. Differential Near End Crosstalk Victim-Aggressor Pattern for 32.0 GT/s Operation

Cross Talk - NEXT, FEXT

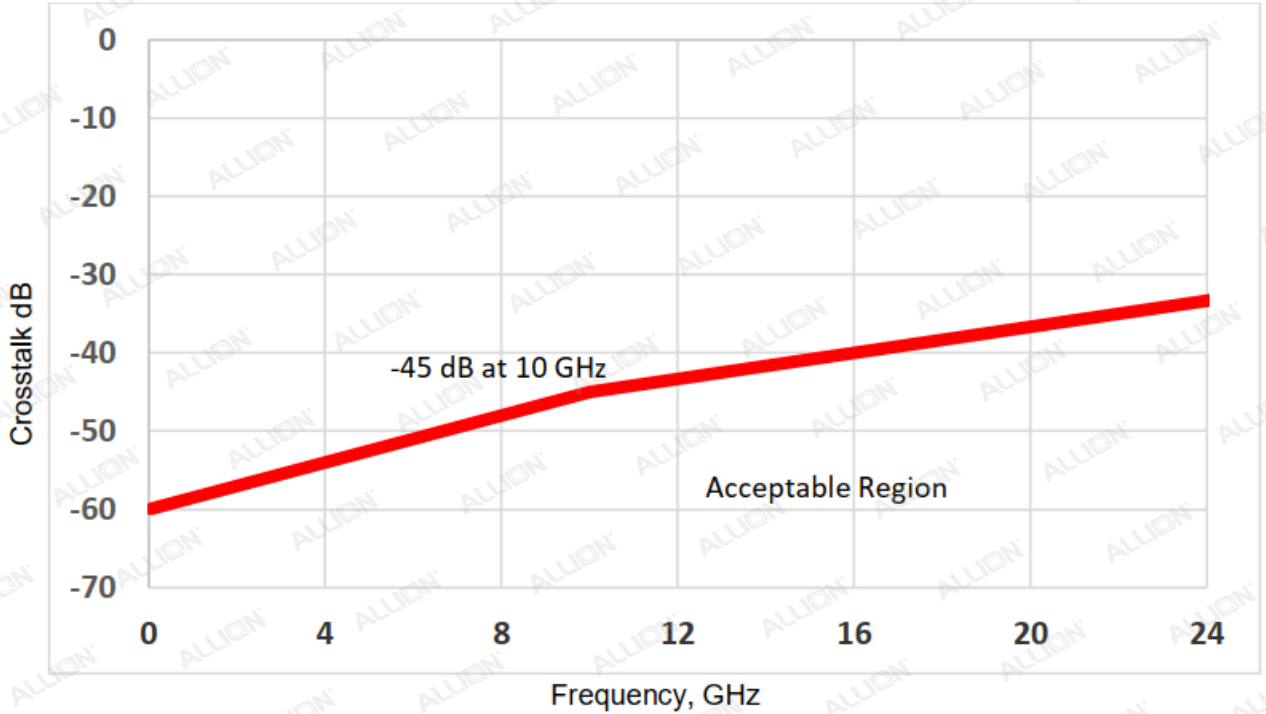


Figure 6-14. Differential Near/Far End Crosstalk Limits for 32.0 GT/s Operation

Cross Talk - ccICN$_{NEXT}$, ccICN$_{FEXT}$

- 若Power Sum crosstalk無法符合，則以ccIN$_{NEXT}$, ccIN$_{FEXT}$，公式再次確認。

$$ccICN_{NEXT} = \sqrt{\frac{1}{2}df\sum_{k=1}^{N_{max}}\left(\frac{A_{NT}{}^2}{f_b}\right)sinc^2\left(\frac{k\cdot df}{f_b}\right)10^{\left(2\frac{IL_{post-channel}(k)}{10}\right)}\left[\frac{1}{1+\left(\frac{k\cdot df}{f_t}\right)^4}\right]\left[\frac{1}{1+\left(\frac{k\cdot df}{f_r}\right)^8}\right]10^{\frac{MDNEXT(k)}{10}}}$$

$$ccICN_{FEXT} = \sqrt{\frac{1}{2}df\sum_{k=1}^{N_{max}}\left(\frac{A_{FT}{}^2}{f_b}\right)sinc^2\left(\frac{k\cdot df}{f_b}\right)10^{\left(\frac{IL_{pre-channel}(k)}{10}+\frac{IL_{post-channel}(k)}{10}\right)}\left[\frac{1}{1+\left(\frac{k\cdot df}{f_t}\right)^4}\right]\left[\frac{1}{1+\left(\frac{k\cdot df}{f_r}\right)^8}\right]10^{\frac{MDFEXT(k)}{10}}}$$

- $IL_{pre-channel}(k) = -\left(\frac{25}{f_b/2}\right)\cdot k\cdot df$, $IL_{post-channel}(k) = -\left(\frac{9.5}{f_b/2}\right)\cdot k\cdot df$
- f_{max} = 24 GHz, f_{min}=10 MHz, df = 10 MHz, f_b = 32 GHz
- A_{FT}= 800 mVpp, A_{NT}= 800 mVpp
- f_t = 31.53 GHz, f_r = 24 GHz

治具製作的注意事項

- Add-in Card 板厚: 1.57 mm
- 規範建議使用FR4的板子，但依據百佳泰實際經驗使用穩定性較好的Rogers系列或是Magtron系列的板材為佳。
- Layout請製作成Single-End Trace。
- Layout長度不超過48mm。
- Trace上不要有Via, 除非特殊設計能降低不必要的反射或共振效果。
- 2X Thru 必須要在同一個板子上。

治具製作的注意事項

- Add-in Card (Form Factor)特別注意事項：
  - Plug的金手指部分必須特別注意與connector母座的阻抗要互相匹配，否則高頻情況下會有Stub的效應出現，造成高頻信號的嚴重反射。
  - 注意NEXT 與 FEXT的干擾問題，需增加屏蔽。
- Add-in Card金手指的尺寸與屏蔽在規範內有清楚說明。

(※如下一頁說明)

最內層尺寸與鋪銅方式

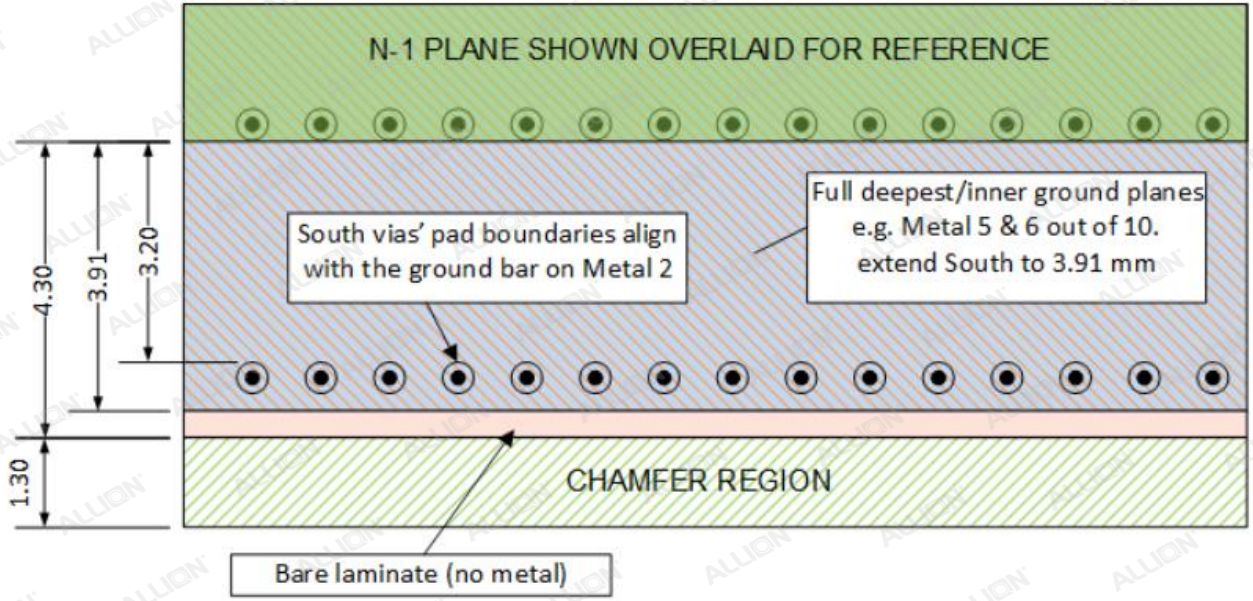


Figure 11-17: Detail of the Core Shielding Ground Plane beneath the Add-in Card Edge-Fingers

最外層尺寸與鋪銅 、屏蔽方式

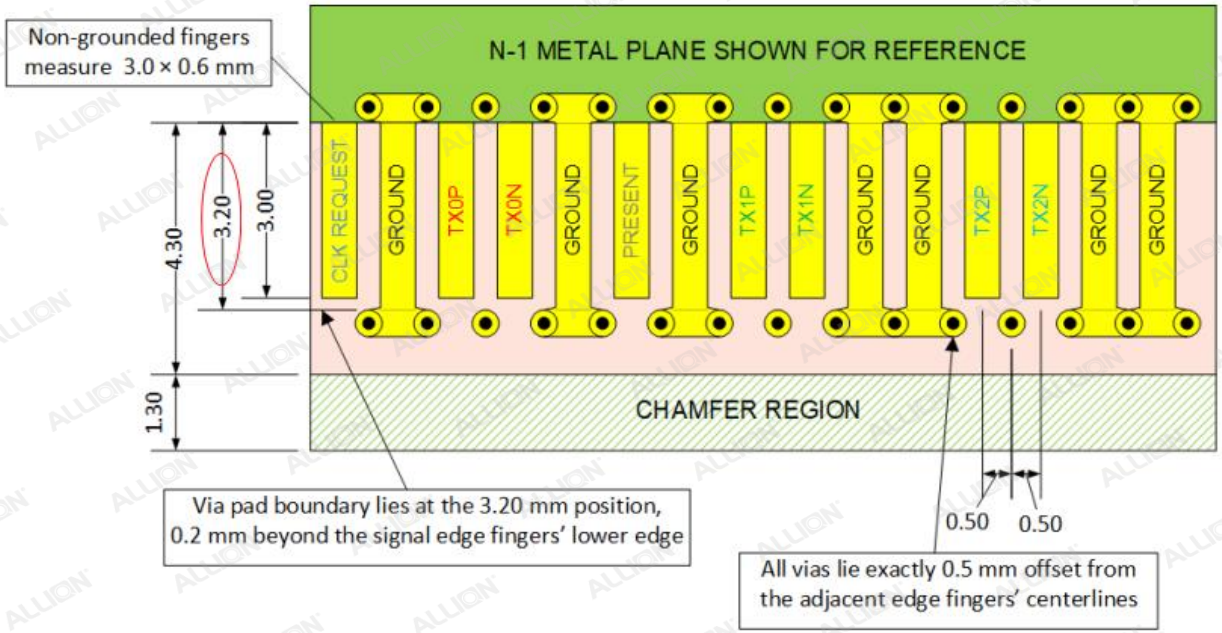


Figure 11-18: Add-in Card Edge-Finger Region, South Edge Ground Vias Indicated. A portion of the N-1 plane (e.g. Metal 2) is shown for reference

第二層與第N-1層的鋪銅方式

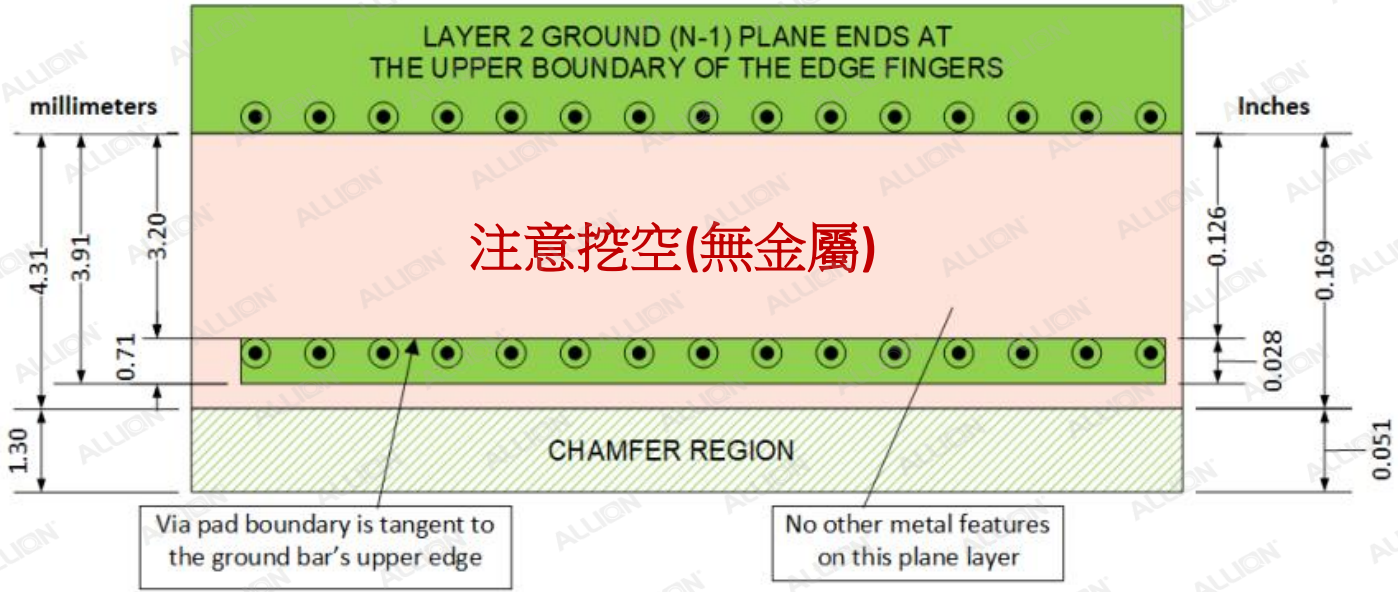


Figure 11-19: Detail of the N-1 Layer Geometry, Highlighting the Lateral South Ground Bar

PCIe Gen5 測試治具

實作 ISI Board

- 右圖是Differential結構的ISI Board。
- ISI board 用在接收端量測上模擬通道衰減的元件，在路徑上減弱信號用。
- 擔心的問題：
  - 頻寬是否如預期?

  某頻率出現劇烈衰減 → Fail
  - 衰減是否線性?

  呈拋物線向下 → Fail

Differential Structure of ISI Board

PCIe Gen5 測試治具

實測結果

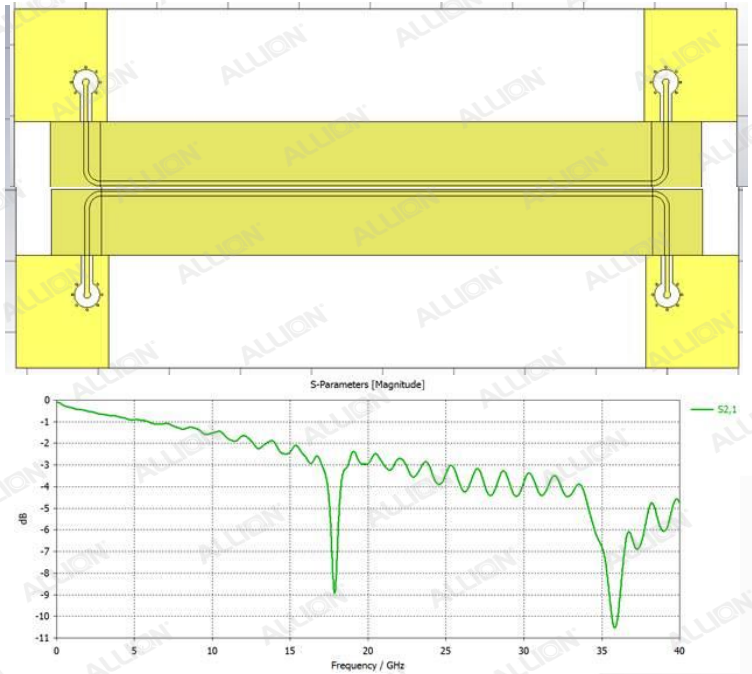
- 完成電路板，直接用VNA量測。
- 有小抖動，但整體來說是直線傾斜下降
- 很明顯的在16~17GHz以及在25GHz有兩波很急遽的衰減，代表在16GHz與25GHz頻寬不足
- 此 ISI Board，設計失敗。

Measurement Results by VNA

PCIe Gen5 測試治具

透過CST是否也能看到相同問題

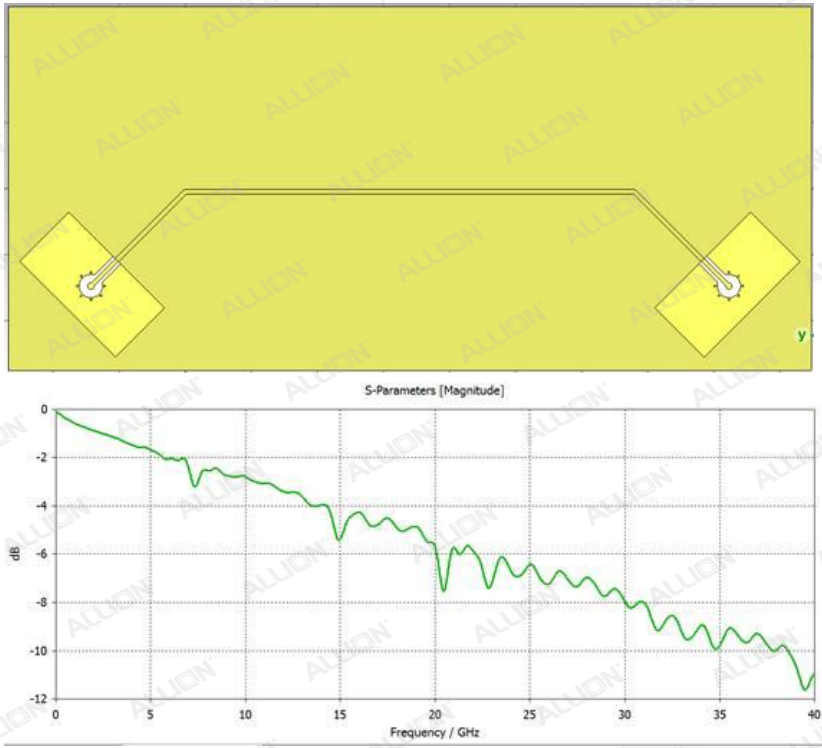
- 將實作的差動結構重新繪製到CST模擬軟體中。
- 模擬結果的確如實測結果，在16GHz附近出現急遽的衰減。另外一個Drop雖然不在25GHz附近，模擬也足以證明這樣的結構是不能使用的。



PCIe Gen5 測試治具

利用CST 獲得改善方法 (一)

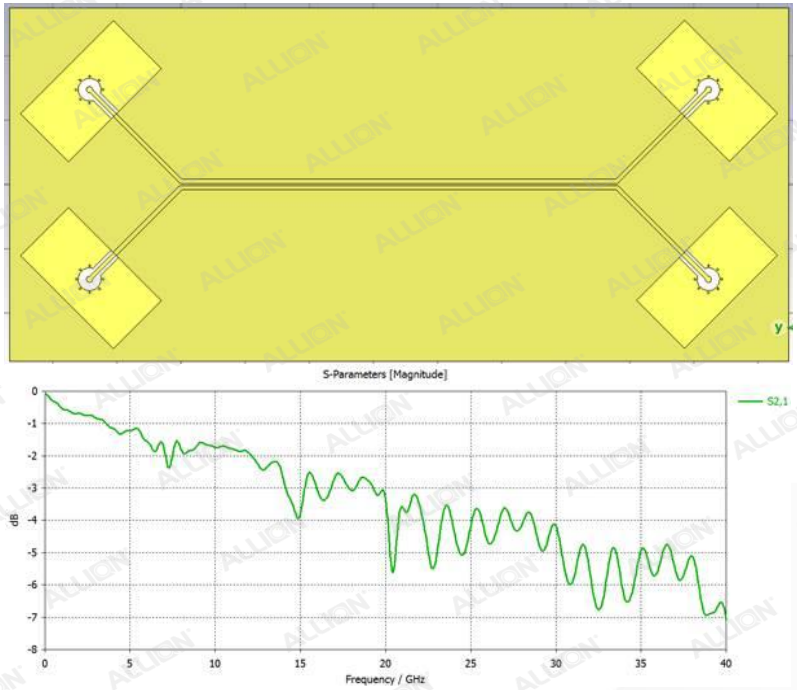
- 改變Layout Pattern 以及相關結構
- 原來16GHz的急遽衰減不見了。
- 大幅的改善。



PCIe Gen5 測試治具

利用CST 獲得改善方法 (二)

- 再次改變Layout Pattern 以及相關結構
- 雖然曲線震盪很大，但實際上衰減量相比之前有小幅降低。
- 還有改善空間。

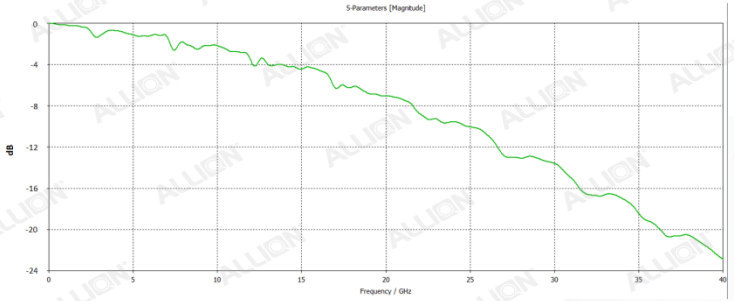


PCIe Gen5 測試治具

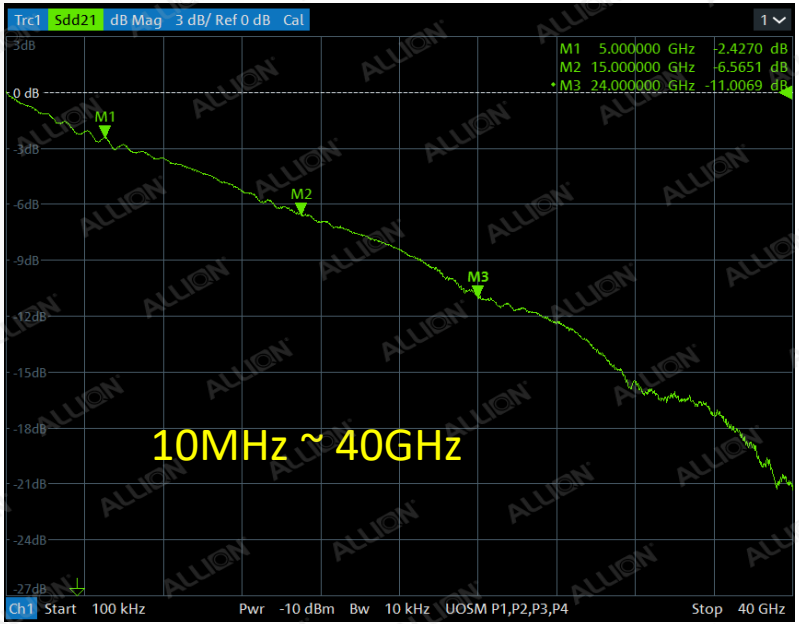
模擬後，重新製板

- 整個曲線已如期待線性斜線往下。
- 頻寬問題解決。
- 可以當衰減用 ISI Board使用。

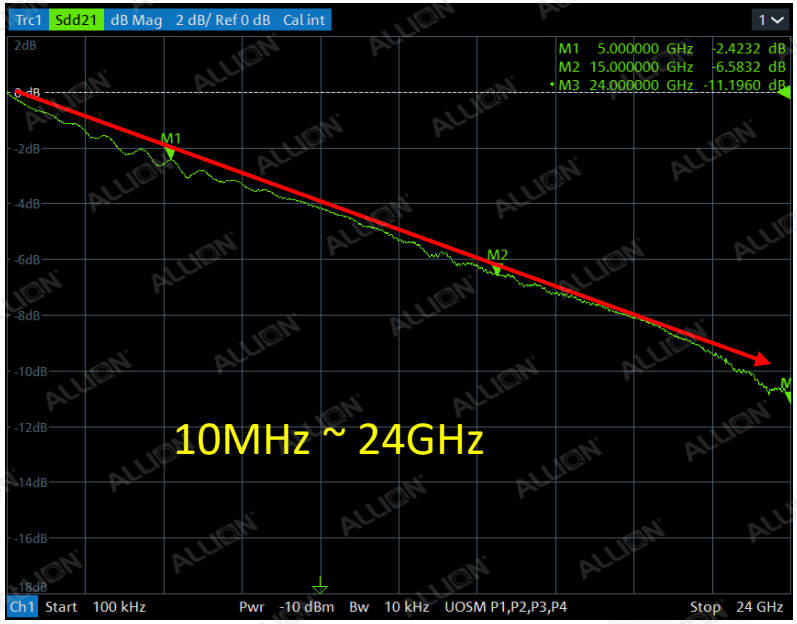
New Differential ISI Board



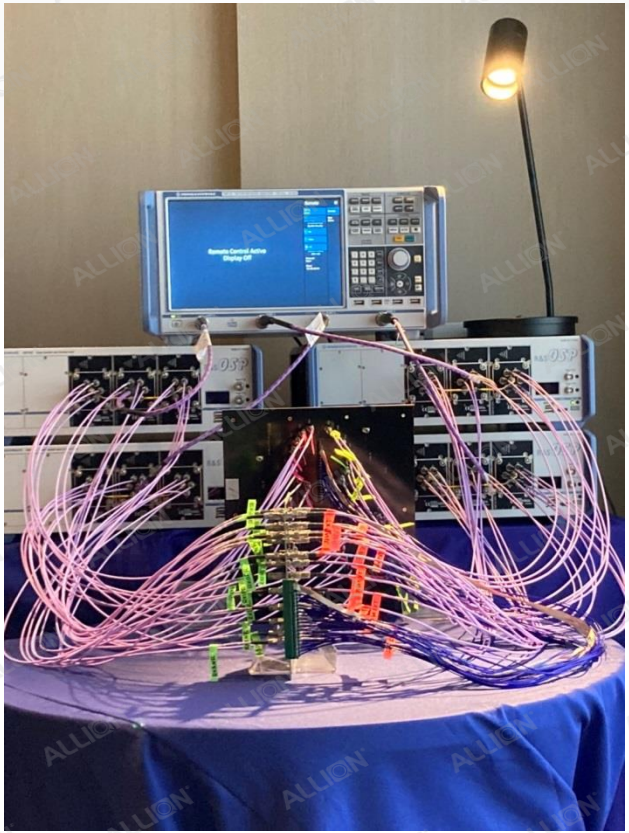
PCIe Gen5 測試治具

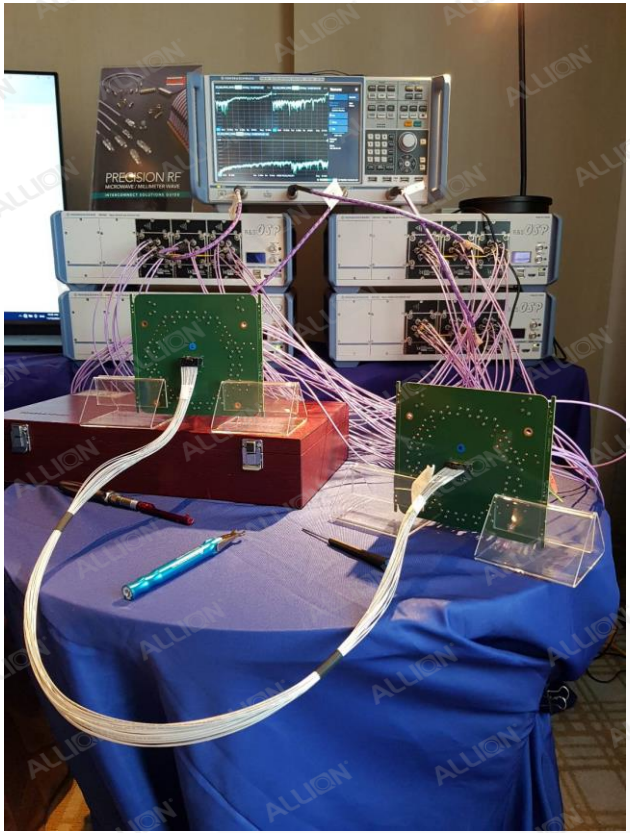


放大

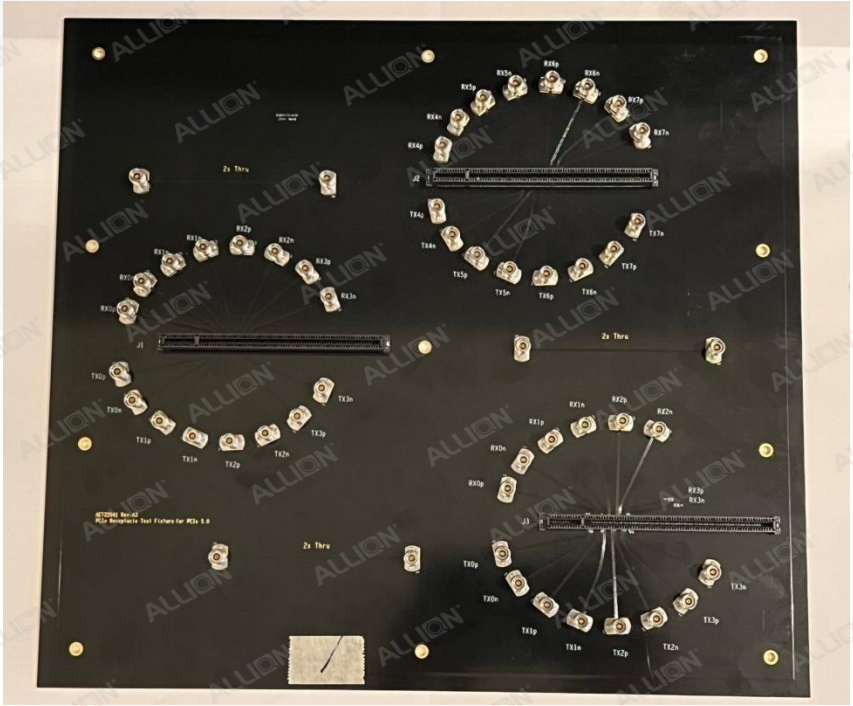


PCIe Gen5 測試治具

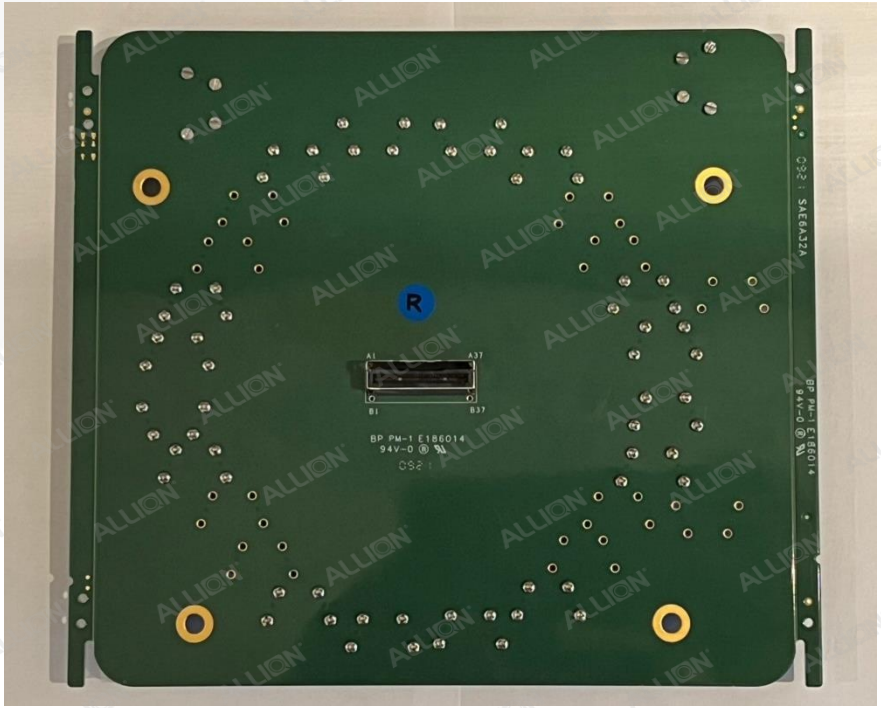


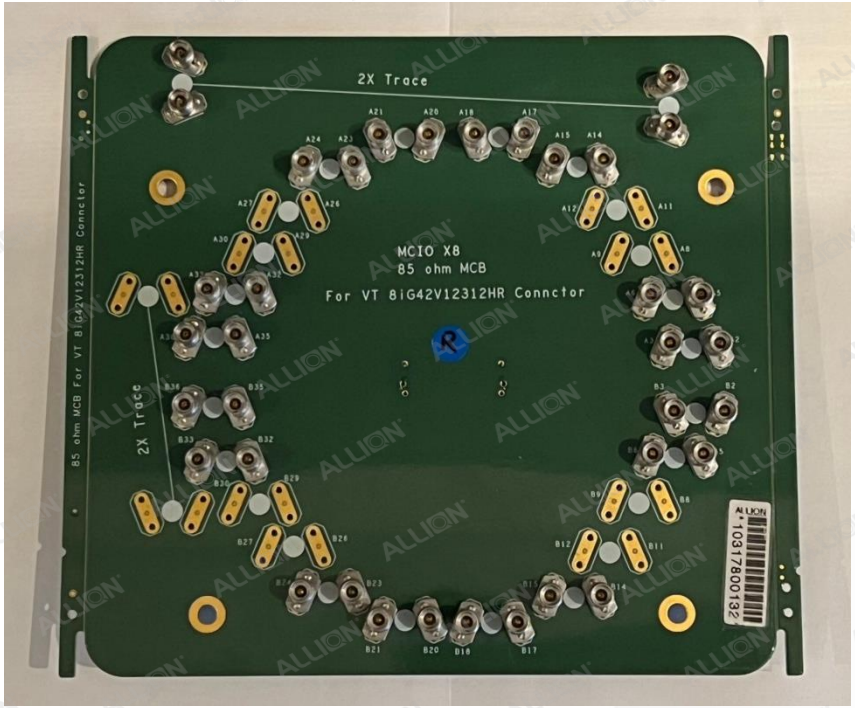


PCIe Gen5 測試治具



PCIe Gen5 測試治具





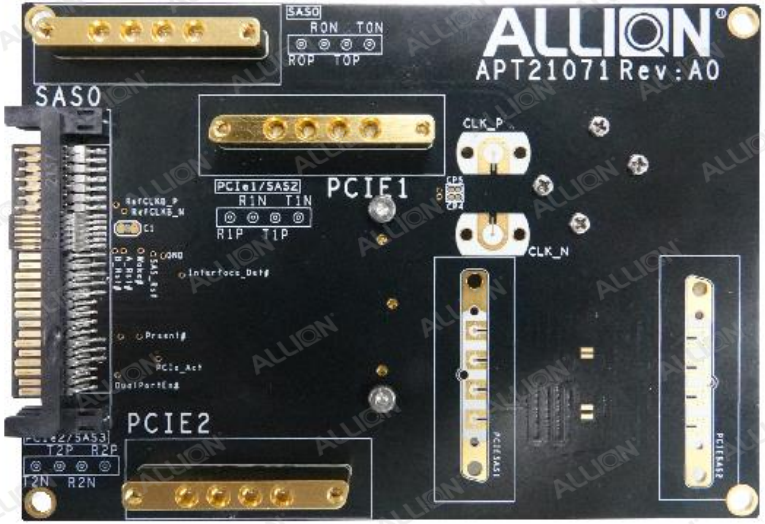
PCIe Gen5 測試治具

- OCP NIC3.0
- EDSFF (Enterprise and Data Center SSD Form Factor) 4C/4C+
- PCIe Gen4/Gen5 Test Fixture Set for Tx/Rx
- 適用於 EDSFF 規格 TA-1002 4C/4C+、OCP NIC3.0、GEN-Z、PECFF、SNIA Native NVME of Drive Tx & Rx.
- 強化SMPM連接器結構，可支援至40GHz
- 縮小尺寸更便於量測
- 兩倍校正線

PCIe Gen5 測試治具

- EDSFF(Enterprise and Data Center SSD Form Factor) E1 PCIe CLB5.0 Test Fixture Set for Tx/Rx
- 適用於E1.S / E1.L(TA-1006/TA-1007)
- 強化SMPM連接器結構，可支援至40GHz
- 縮小尺寸更便於量測
- 線盒模組化，安裝簡單化
- 兩倍校正線

PCIe Gen5 測試治具



- U.2 PCIe Gen5 & SAS 4 Compliance Test for Tx/Rx
- U.3 PCIe Gen5 & SAS 4 Compliance Test for Tx/Rx
- 適用於U.2 & U.3 認證測試
- 採用最新SAS 連接器，可滿足SAS4以及 PCIe Gen5的規格
- 強化SMPM連接器結構，可支援至40GHz
- 線材模組化，安裝簡單化
- 兩倍校正線

PCIe Gen5 測試治具

- PCI Express Gen4 & Gen5 Compliance Test for Tx/Rx
- 適用於PCIe M.2 Gen4 / Gen5 Electrical Test for Tx & Rx
- 強化SMPM連接器結構，可支援至40GHz
- 線材模組化，安裝簡單化
- 兩倍校正線

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