從設計到實現RF待測物
— EDA模擬中RF功率放大器線性化的優勢

Dr. Milton Lien, Sr. Principal Application Engineer, Cadence
Arsene Chen, Application Engineering Manager, R&S Taiwan

ROHDE&SCHWARZ
Make ideas real

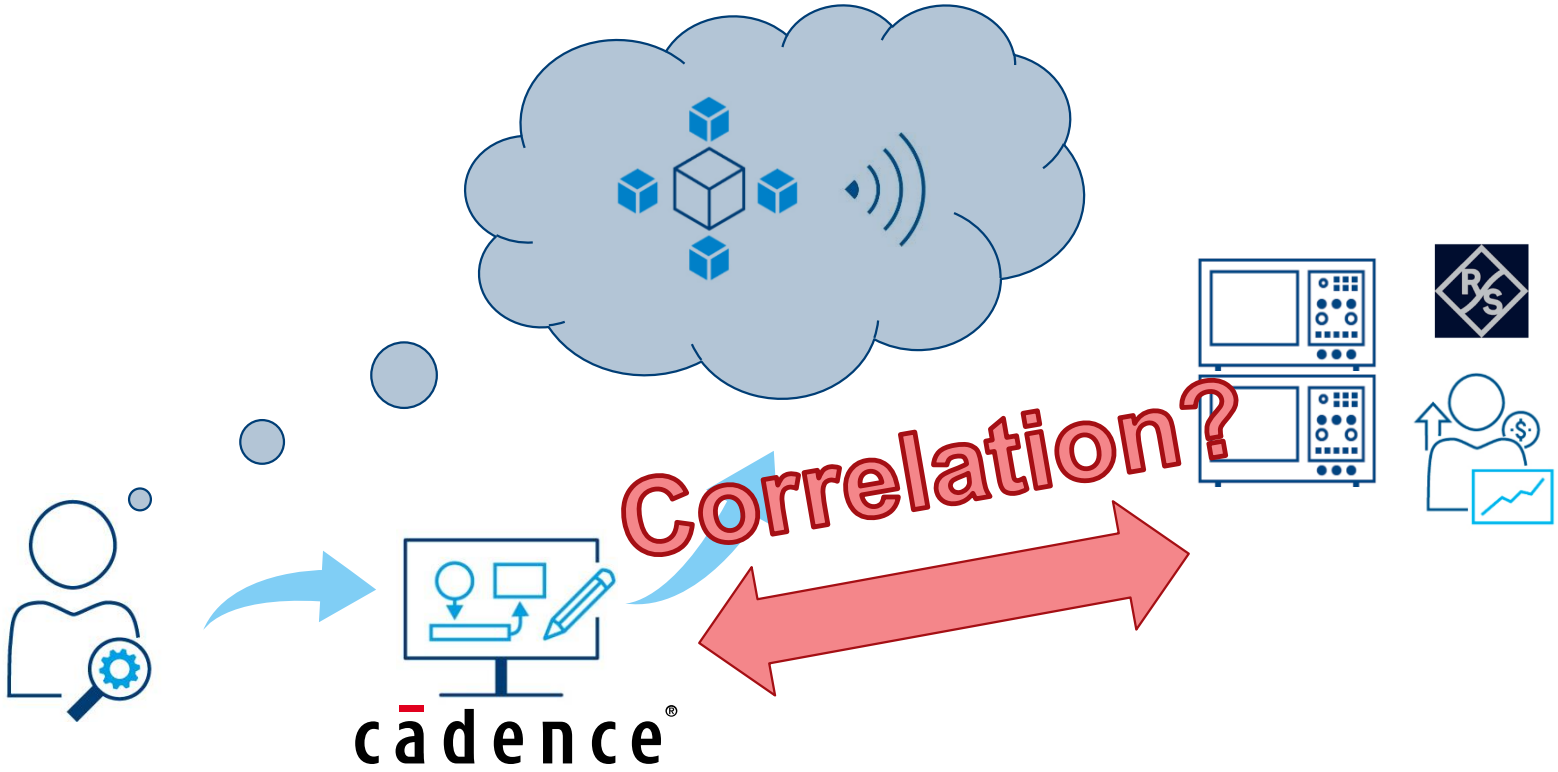
AGENDA

- Introduction
- New joint solution from R&S and Cadence
- Introduction to the Cadence AWR Design Environment® platform
- Live demonstration of joint solution – I

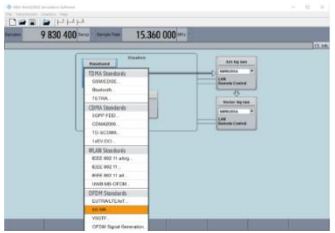
- Combination of Cadence VSS EDA with Direct DPD by Rohde & Schwarz
- Live demonstration of joint solution – II

- Summary

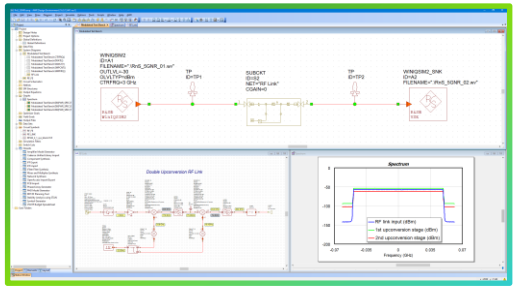
WHY COLLABORATION?



JOINT SOLUTION: AND cadence®

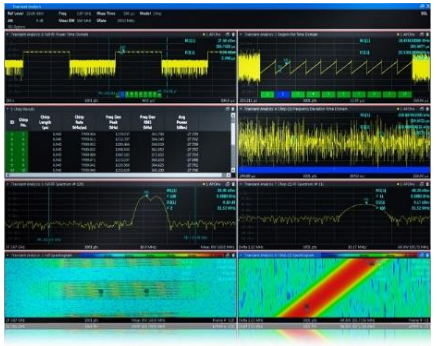


WinIQSIM2
Signal Generation

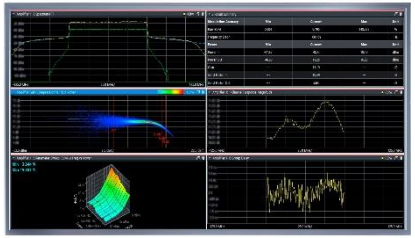


Cadence VSS
RF Design/Analysis

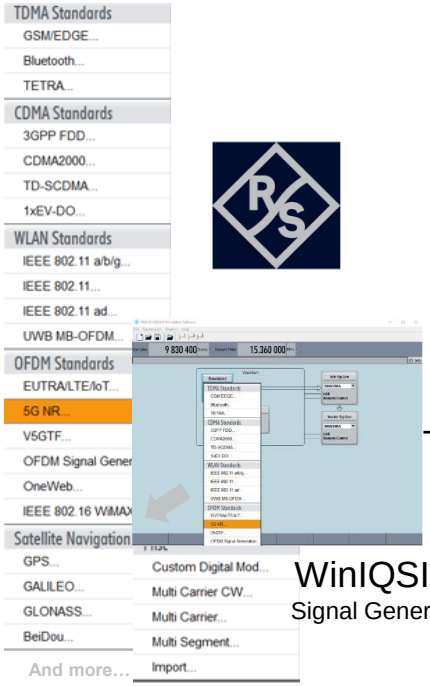
VSE
Signal Analysis



Direct DPD
Linearization

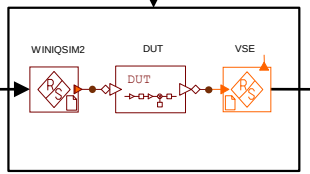


JOINT SOLUTION: AND cadence®



WinIQSIM2
Signal Generation

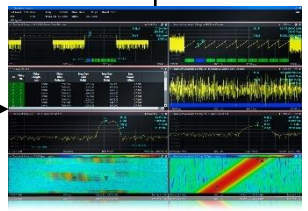
Encrypted
IQ files



VSS*
Visual System Simulator

Encrypted
IQ file

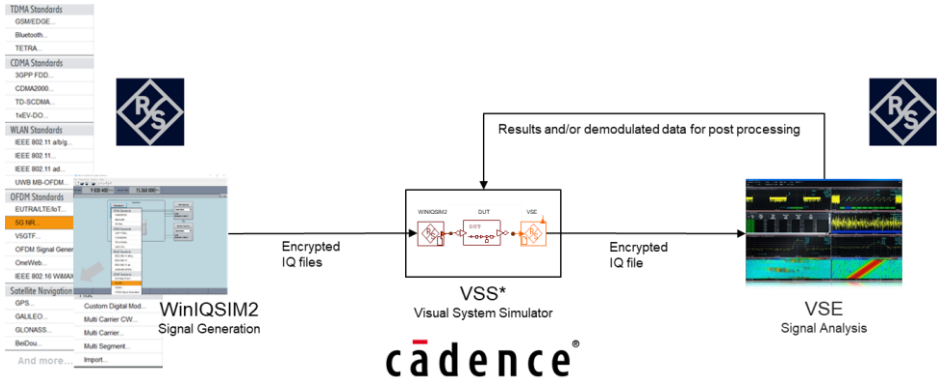
Results and/or demodulated data for post processing



VSE
Signal Analysis

cadence®

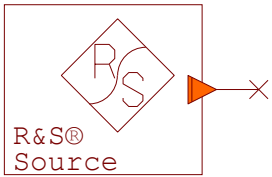
JOINT SOLUTION: AND cadence



JOINT SOLUTION: AND cadence

- **New software product: R&S VSESIM-VSS**
  - VSE included
  - Plug-in for VSE and WinIQSIM2 included in VSE installer
  - WinIQSIM2 license included – separate installer

RS_SRC
ID=A3
FILENAME=""
OUTLVL=0
OLVLTYP=dBm
CTRFRQ=1 GHz



Replay encrypted wv files in VSS

RS_SNK
ID=A4
FILENAME=""

Capture VSS signals and save into encrypted wv files

JOINT SOLUTION: AND cadence®

- Focus on components like power amplifier all the way to complex RF systems as in base station radios, radar systems or satellite links

- **Goal: Enabling first pass design**
  - Complex new communication systems support high bandwidth and complex scenarios
  - Interaction between components in RF system amplified with modern wideband systems
  - Use of real signals in EDA system simulation to verify resulting FOM of EVM
  - Maximize correlation with same signal in simulation and physical test
  - Investigate linearization (DPD) already in simulation
  - Streamlined process from design to implementation

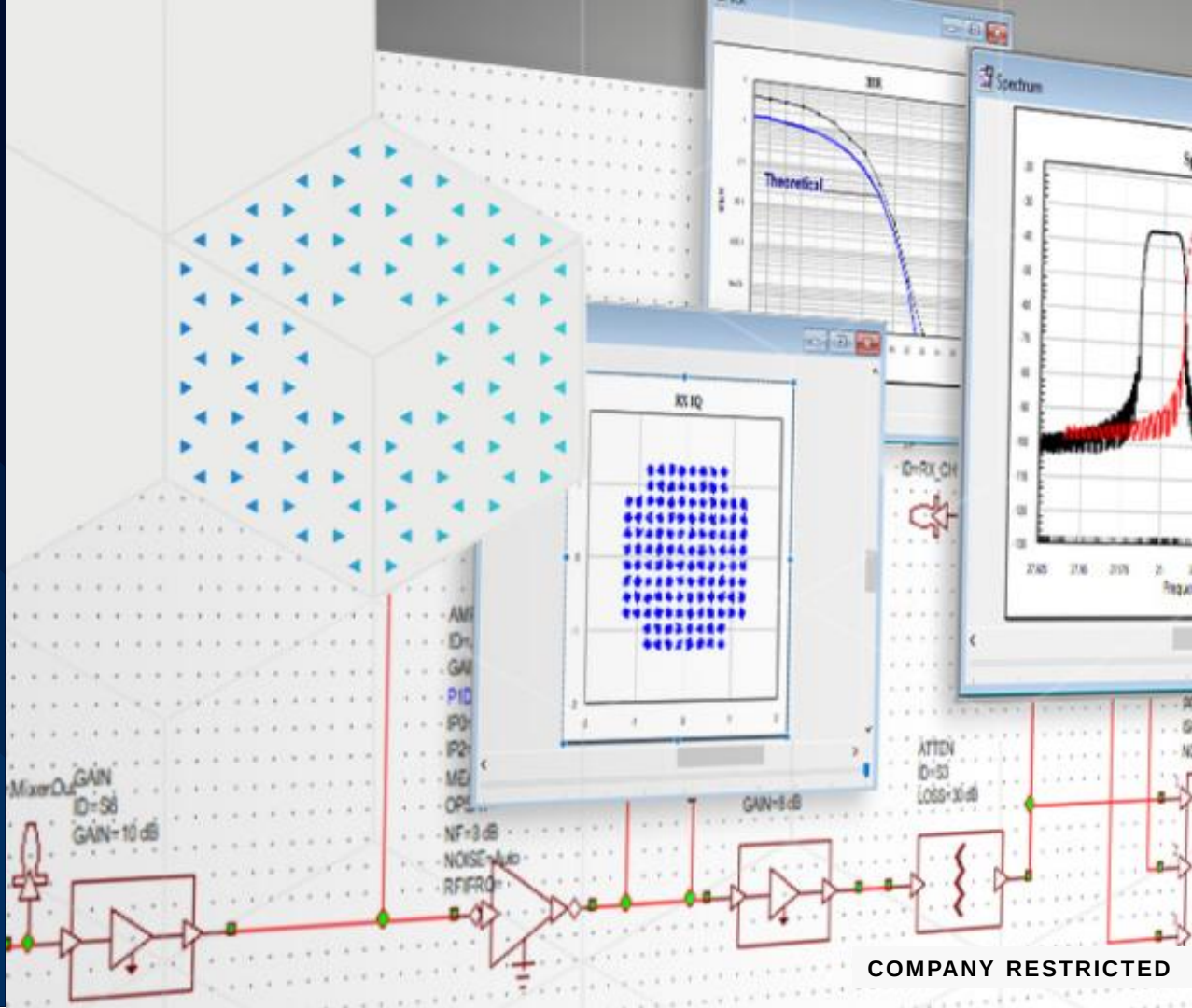
COOPERATION: AND cadence® GETS YOU FURTHER

- What to do when having half the system ready?
  - VSE sink can be placed anywhere in the VSS chain and get the IQ data to plug into SMW ARB
  - HIL scenarios

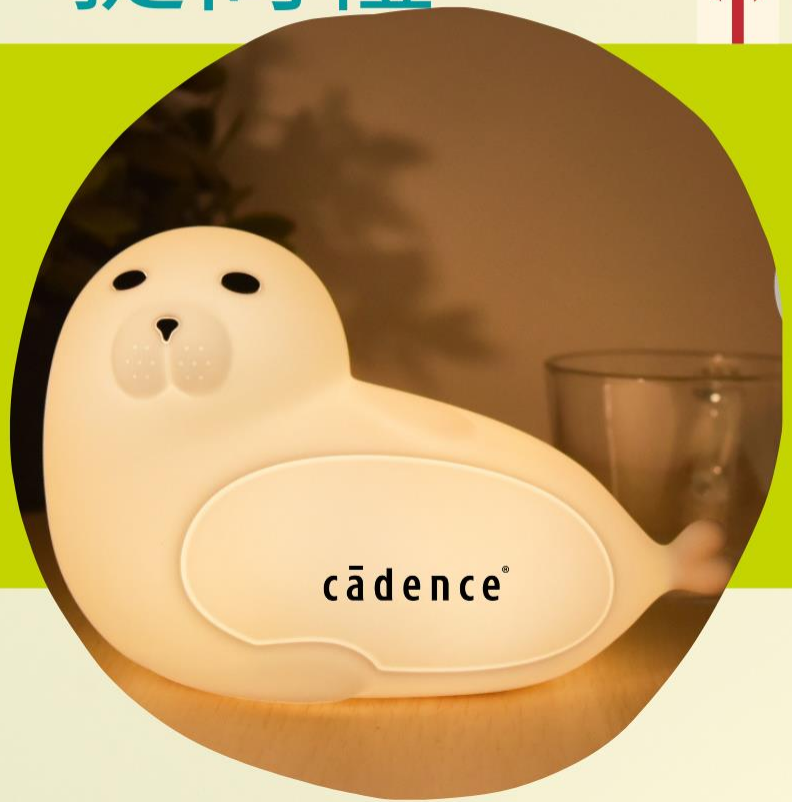
VSS*
Visual System Simulator

CADENCE INTRODUCTION

- Introduction to Cadence world and family of solutions
- Live demo



Ask Cadence
提問禮



留言提問Cadence，即有機會獲得限量好禮

「療癒拍拍海豹燈」！

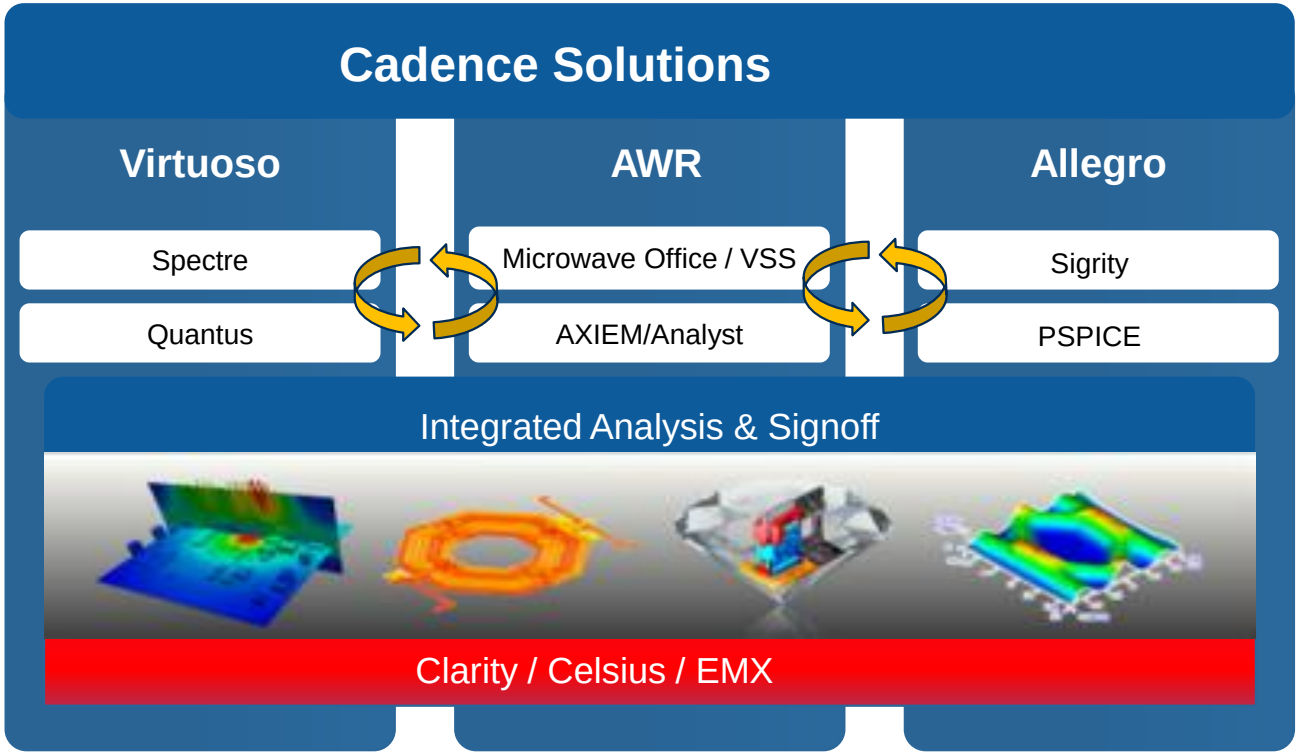
ROHDE SCHWARZ – CADENCE COLLABORATION

WinIQSim2 – VSS – VSE Product integration

Dr. Milton Lien, Sr. Principal Application Engineer, Cadence

cadence®

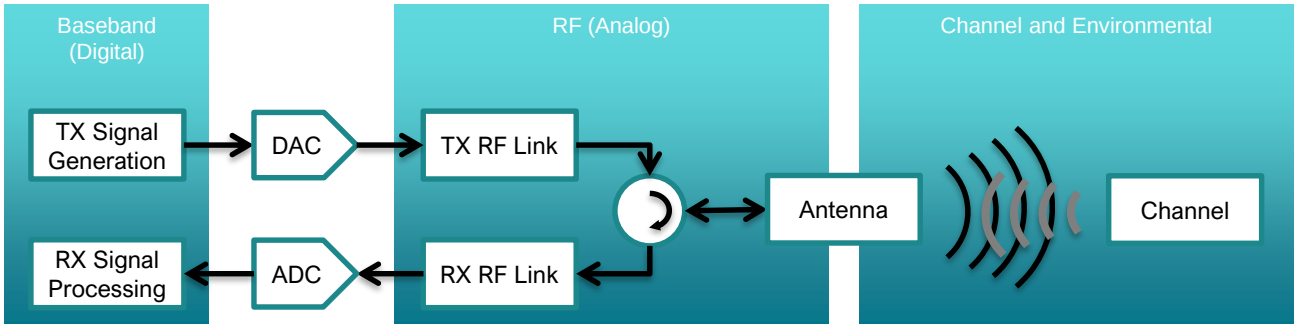
AWR RF WITHIN CADENCE



VISUAL SYSTEM SIMULATOR ™ (VSS)

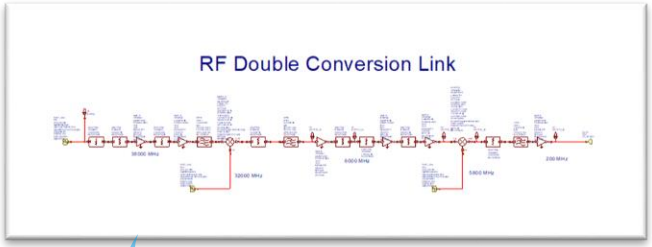
- Part of the Cadence AWR Design Environment® platform
- Design and analyze anything from simple RF links to complete comm systems
  - RF budget analysis, RF spur heritage
  - Modeling and time-domain simulation of complete communication links
  - Phased array design, standard communication libraries, etc.

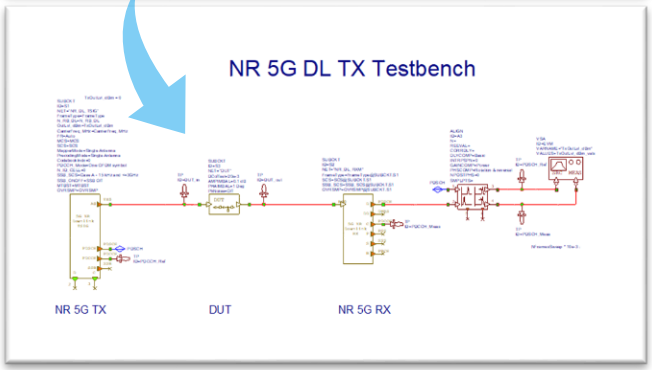
VSS includes models for every component in such systems!



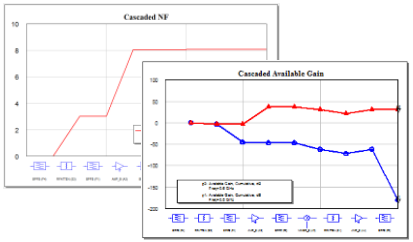
RF SYSTEM DESIGN AND ANALYSIS FLOW

- Construct and analyze RF link

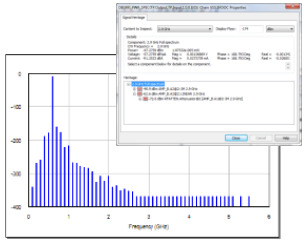




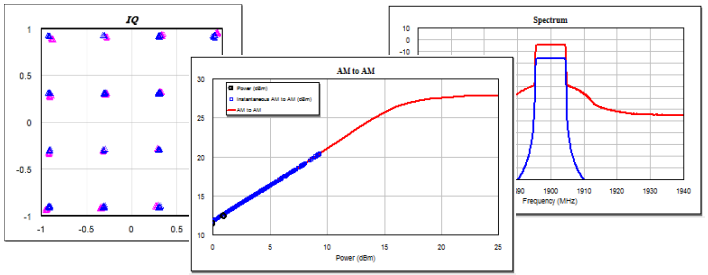
RF Budget Analysis



Spur Identification



Time Domain Simulations



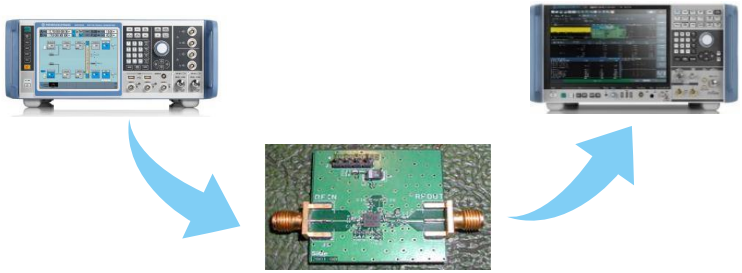
- Include in communication system/test bench

The same RF link is used by RF budget, spur analysis and time domain simulators!

VSS CUSTOMER BASE

- RF Component and Circuit Designers
- RF System/Sub-System Designers
- Baseband System Designers

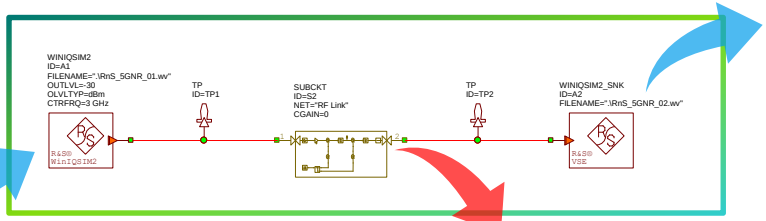
Design often leads to prototyping and measurements in lab

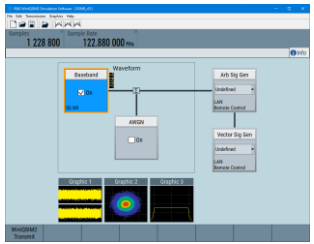


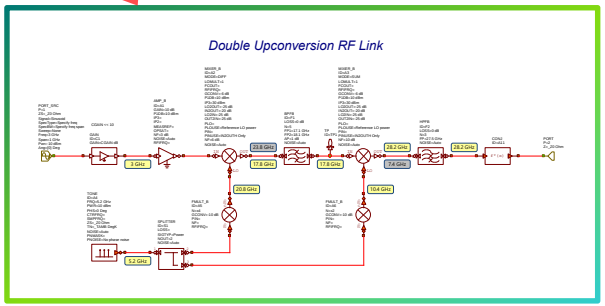
Need for instrumentation and fully spec-compliant signals!

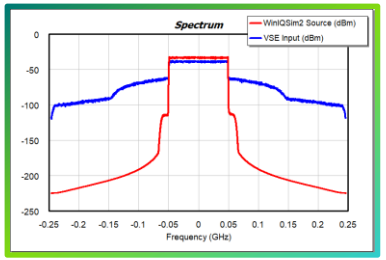
R&S – CADENCE INTEGRATED DESIGN FLOW

- Signal generation: WinIQSim2
- DUT modeling/analysis: VSS
- Signal analysis: VSE





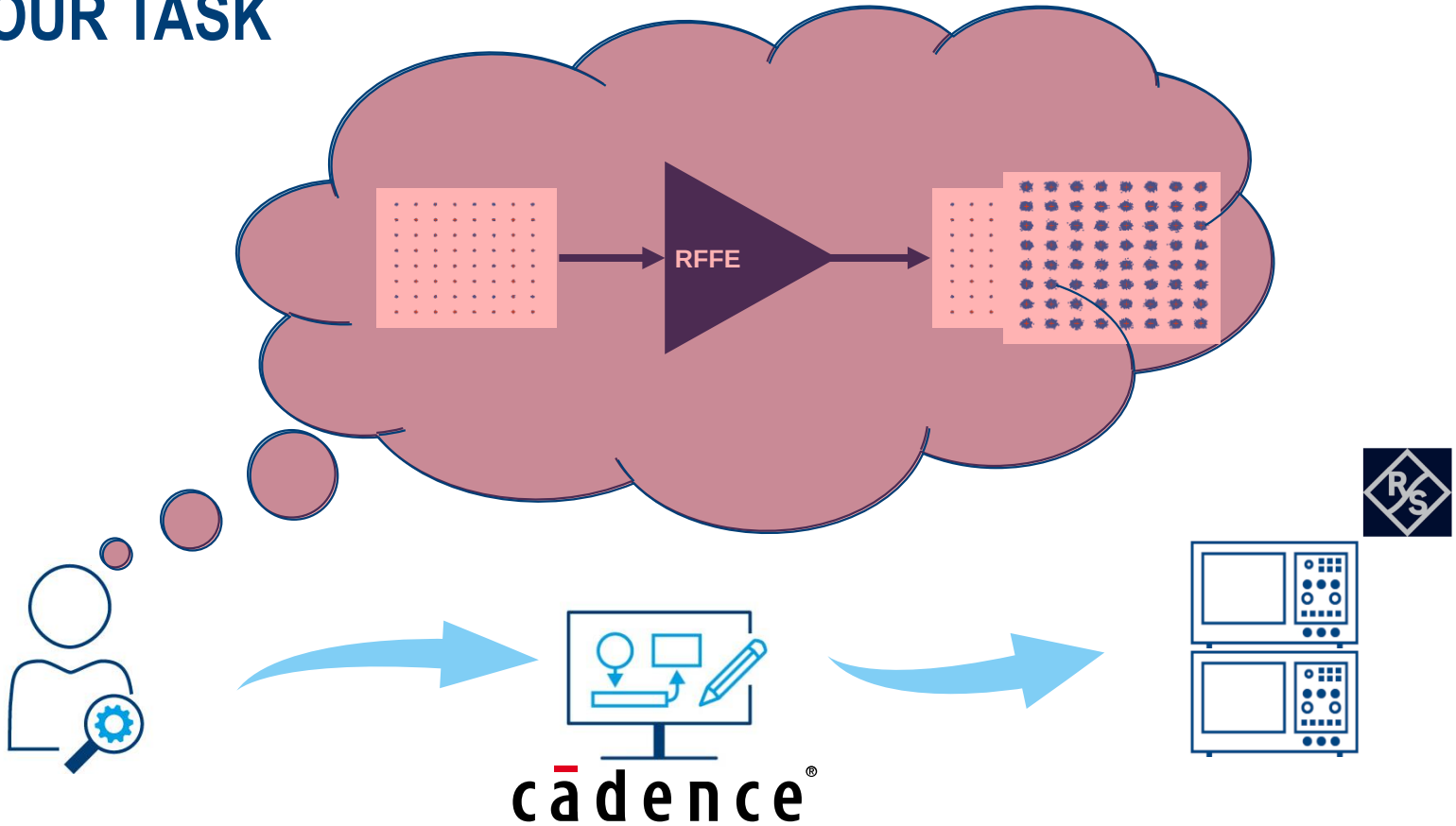




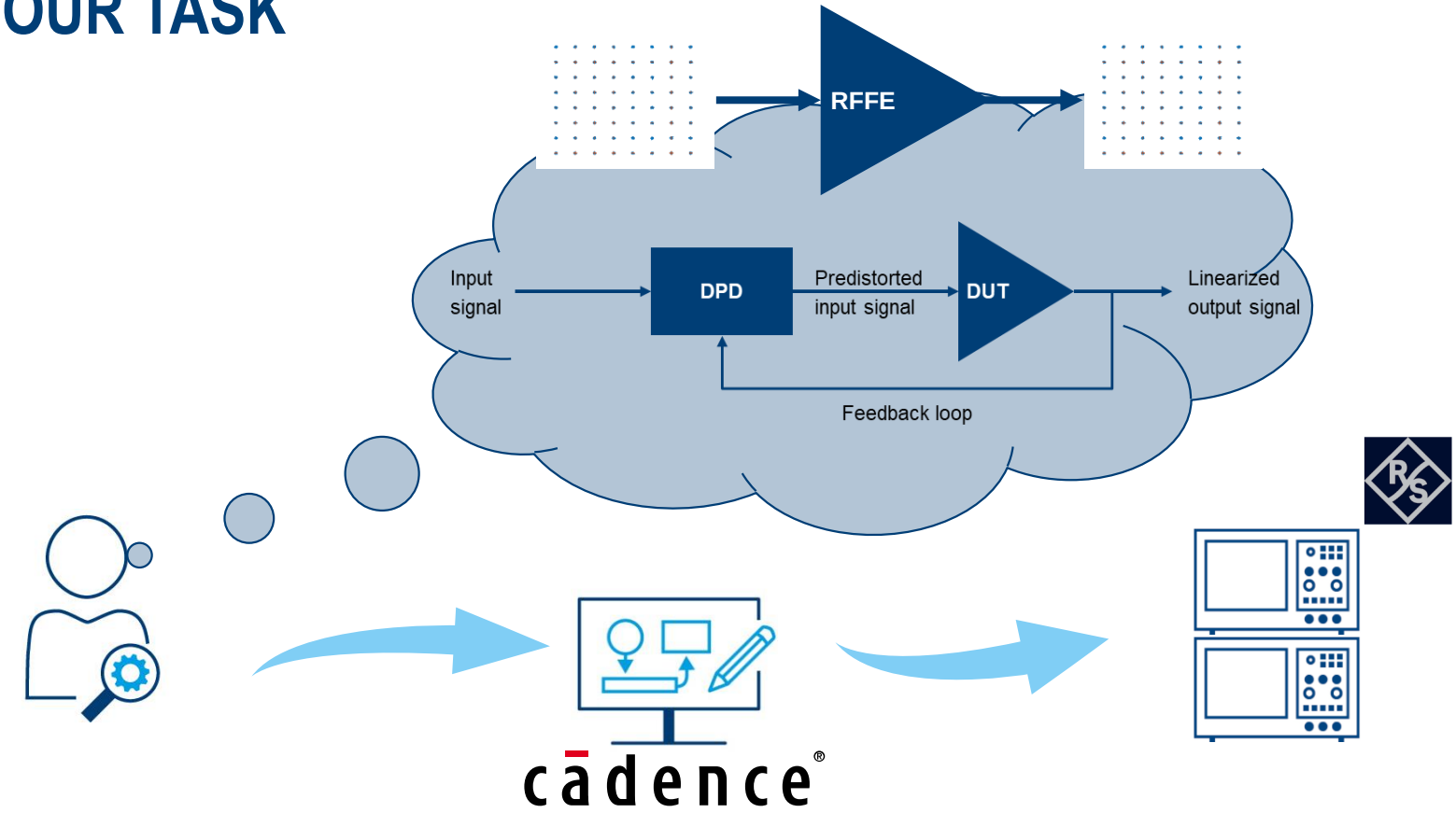
DEMO OF WINIQSIM2 – VSS – VSE CO-SIMULATION

LINEARIZATION FOR RF POWER AMPLIFIER

YOUR TASK



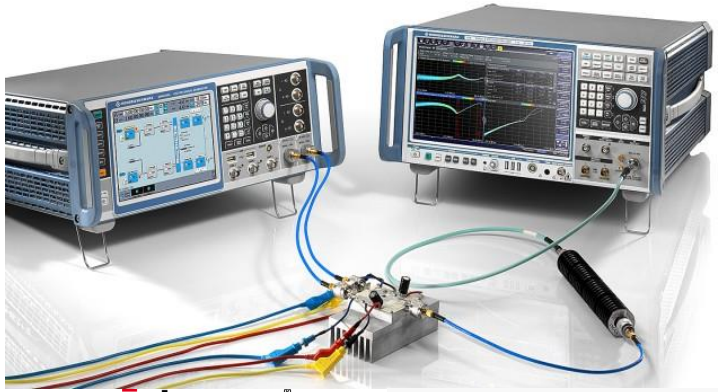
YOUR TASK


RFFE
Input signal
DPD
Predistorted input signal
DUT
Linearized output signal
Feedback loop
cadence®

WHY LINEARIZATION?

- Challenging RF signals on RF frontends
  - 5G in mmWave and RF, mMIMO, beamforming, increasing bandwidth, higher order modulations, digital payloads, wideband Electronic Warfare (EW)
- Significant power consumption is in the RF Front-End (RFFE)
  - Operating close to saturation offers best energy efficiency
  - Technologies such as GaN absolutely require digital predistortion for linear operation
- Various PA topologies studied
  - Doherty, Load Modulated Balanced Amplifier (LMBA), Outphasing, …
- PA gains in efficiency but is highly non-linear

  → Linearization is a _*MUST*_



LINEARIZATION / DPD

- PAs often driven close to saturation for max power efficiency, but in non-linear operation: compression & memory effect
- Linearization for compensation
- Understand system level performance with ideal predistortion needed

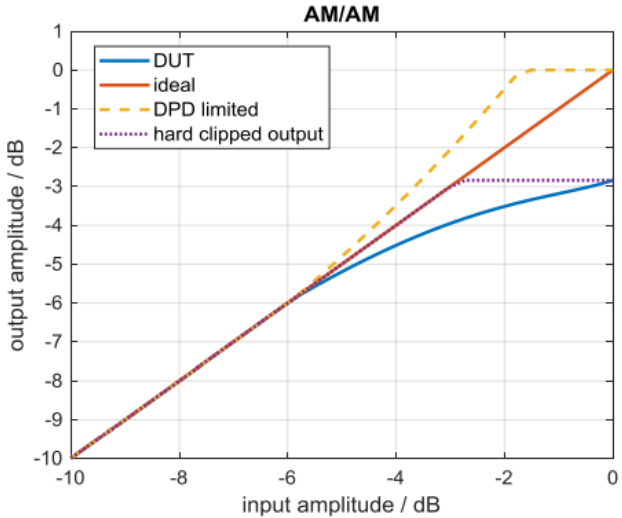
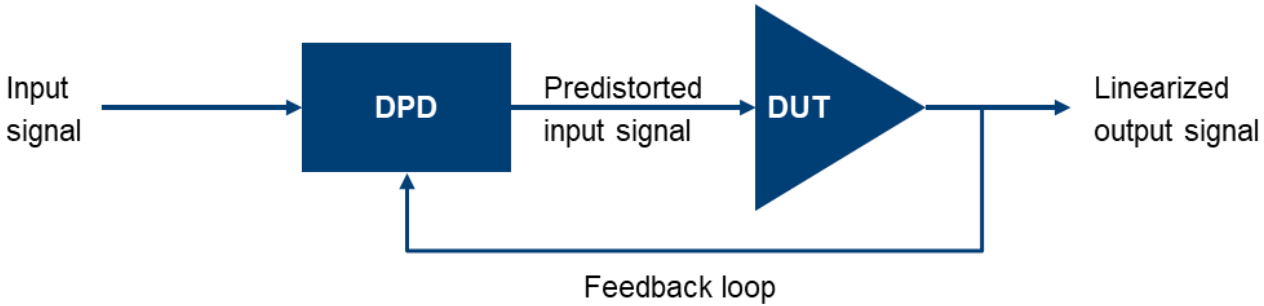
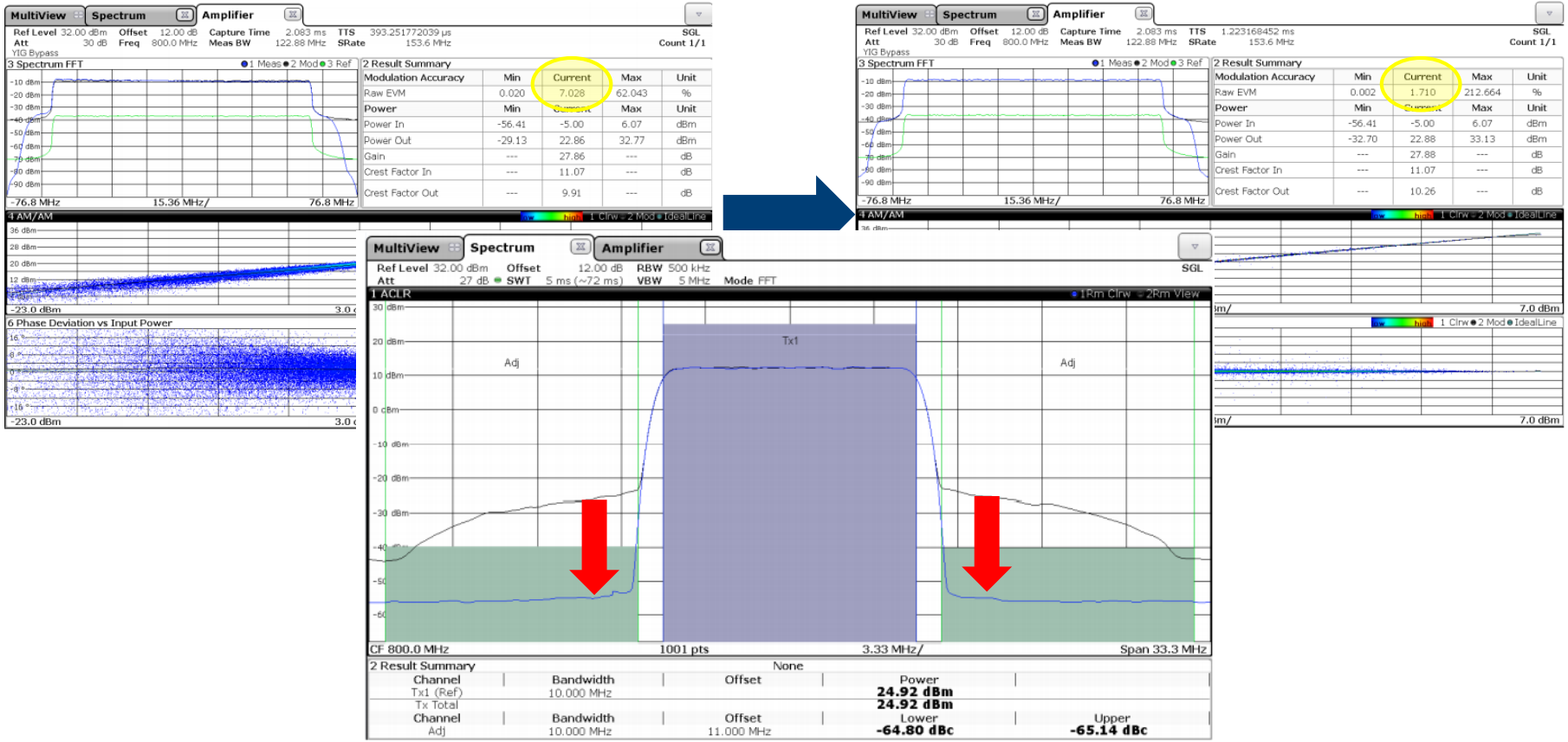


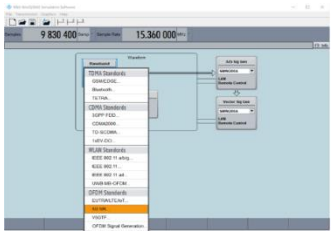
Figure 4 Overview plot: measured AM/AM, ideal output, pre-distorted input signal, and target output signal (hard clipped)



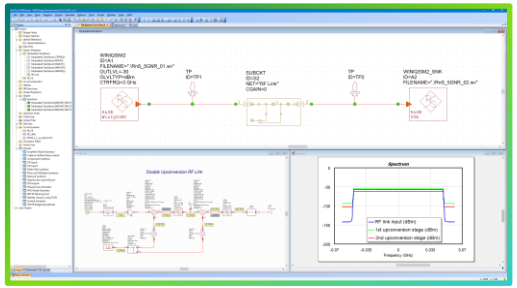
DIGITAL PREDISTORTION: BEFORE AND AFTER



JOINT SOLUTION: AND cadence®

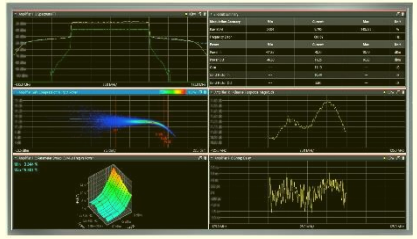


WinIQSIM2
Signal Generation



Cadence VSS
RF Design/Analysis

VSE
Signal Analysis



Direct DPD
Linearization

VSS BRIEF INTRODUCTION

RF System Design and Analysis

Dr. Milton Lien, Sr. Principal Application Engineer, Cadence

cadence®

VISUAL SYSTEM SIMULATOR ™ (VSS)

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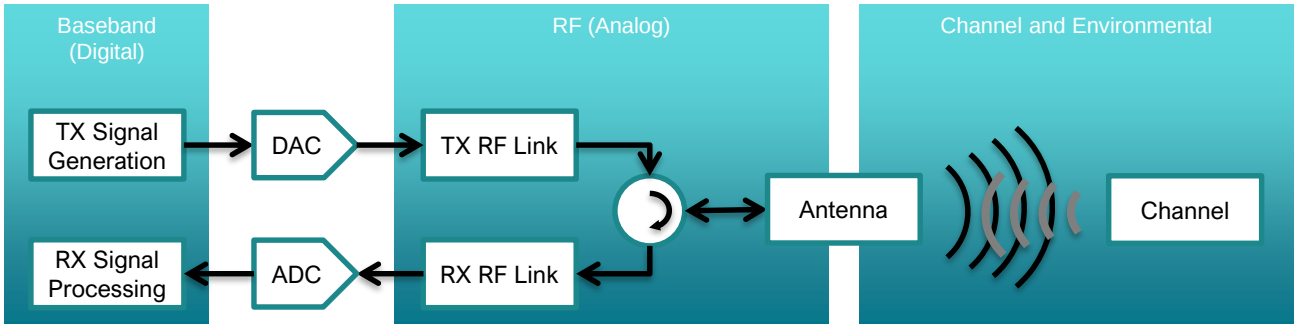
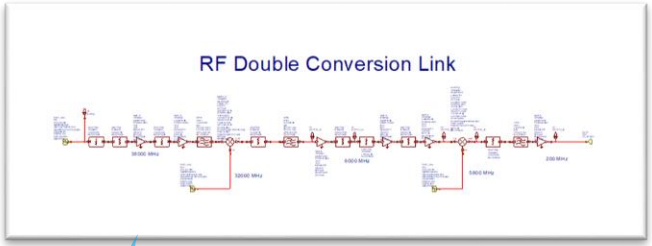
VSS includes models for every component in such systems!

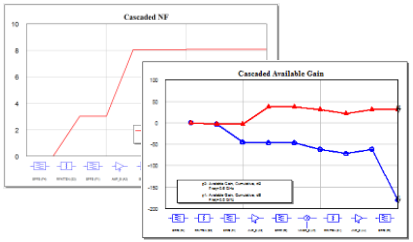


RF SYSTEM DESIGN AND ANALYSIS FLOW IN VSS

- Construct and analyze RF link



RF Budget Analysis



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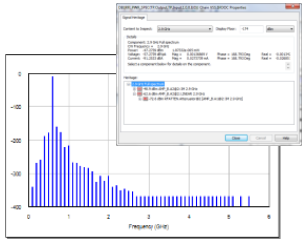
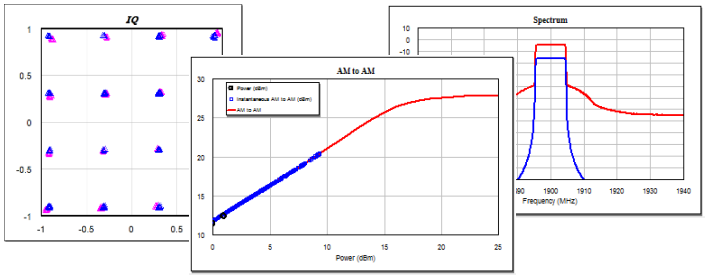


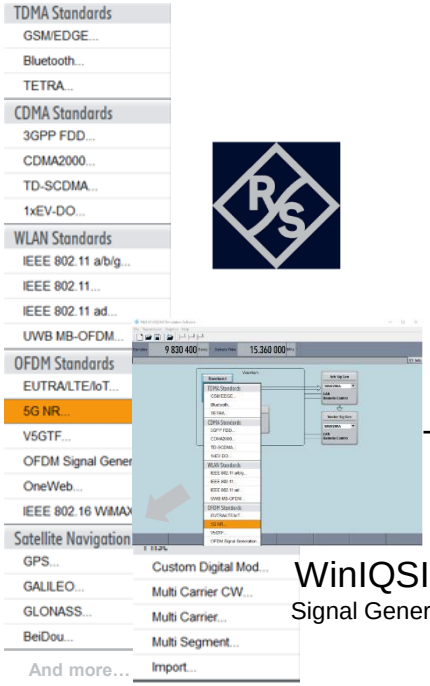
Time Domain Simulations



- Include in co

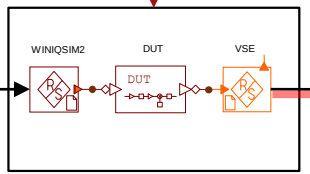
The same RF link is used by RF budget, spur analysis and time domain simulators!

JOINT SOLUTION: AND cadence®



WinIQSIM2
Signal Generation

Encrypted
IQ files

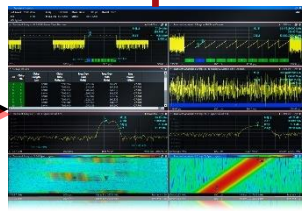


VSS*
Visual System Simulator

Feedback loop for DPD

Behavior
after DPD

Encrypted
IQ file



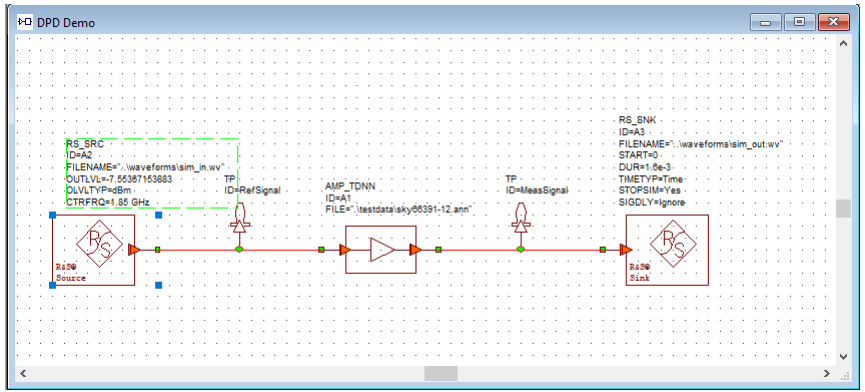
VSE
Signal Analysis

cadence®

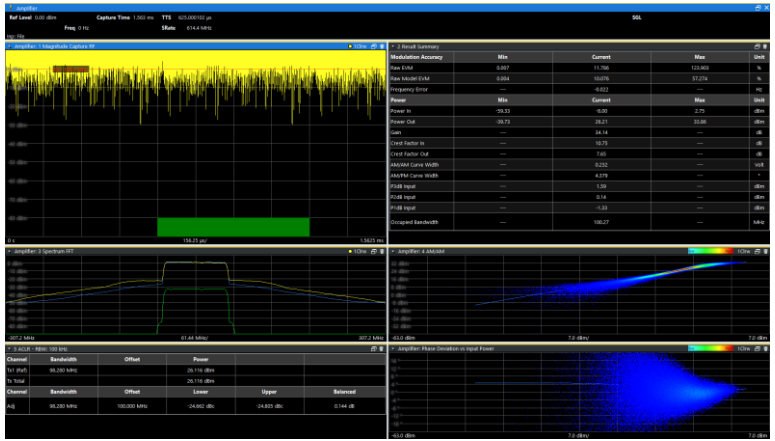
PRE-DISTORTING AN RF-AMPLIFIER PURELY IN SIMULATION

Script controlling both
software packages:
Cadence VSS and R&S VSE

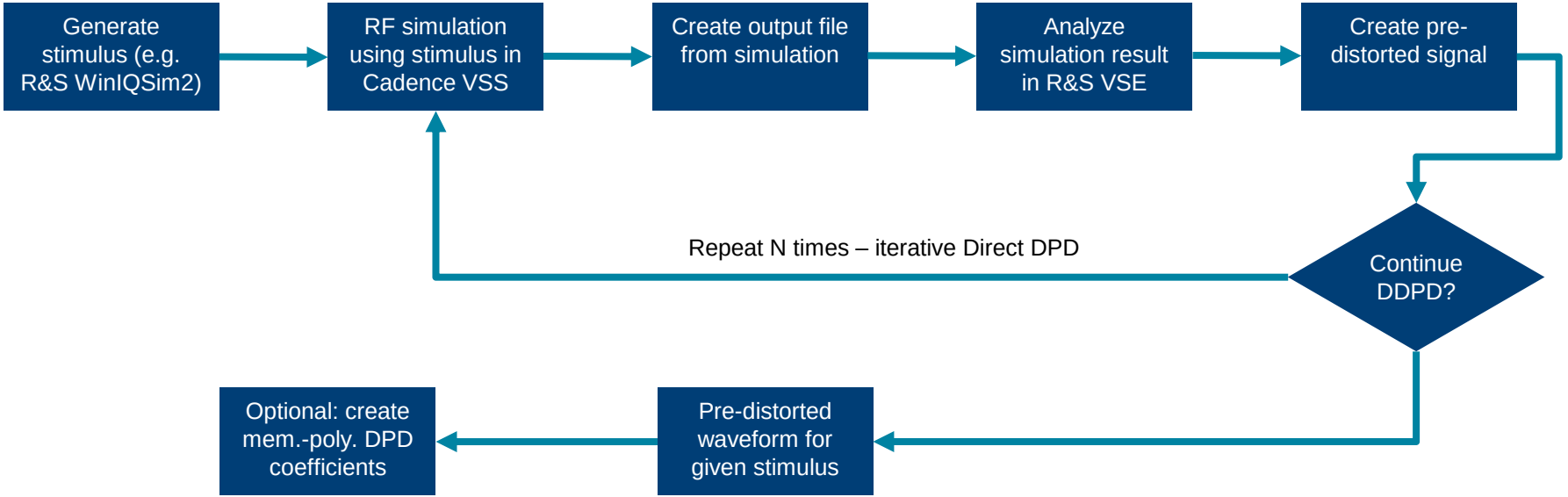
RF simulation of PA in Cadence VSS



Iterative Direct DPD in R&S VSE

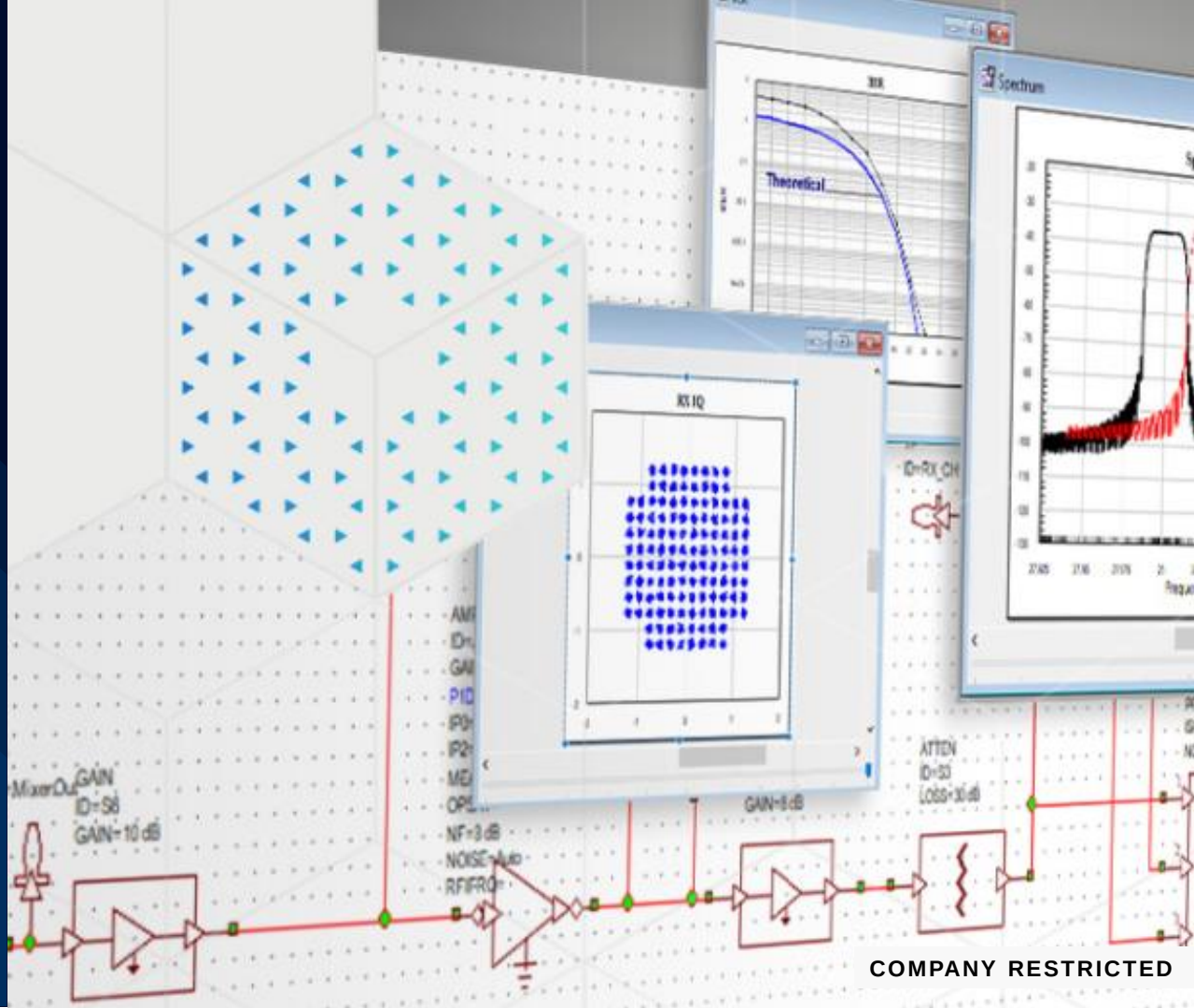


SCHEMATIC FOR PRE-DISTORTION IN RF SIMULATION CADENCE VSS – R&S VSE

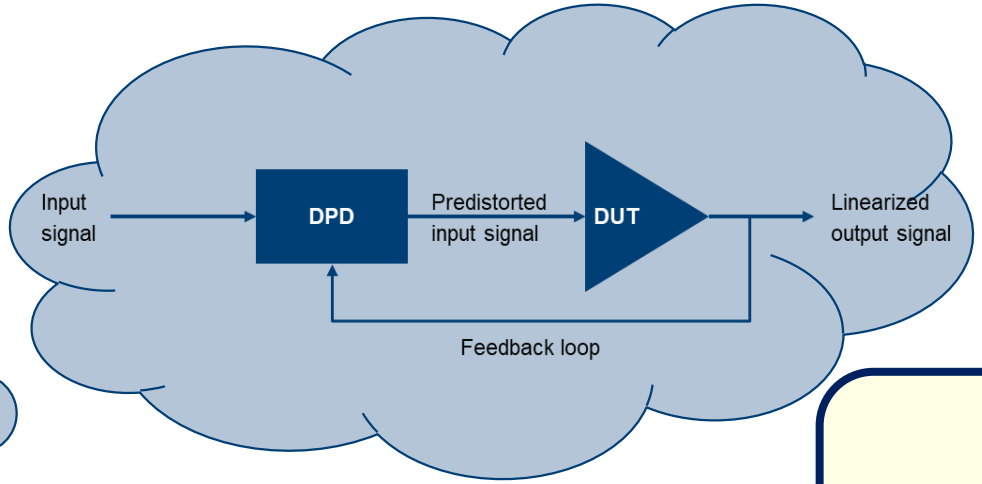


DPD IN RF SIMULATION

- Live demo of the joint solution
- Linearization in Cadence VSS using R&S VSE toolset

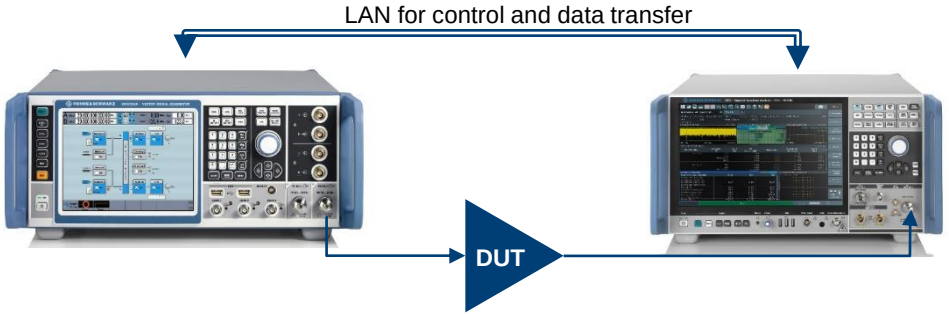


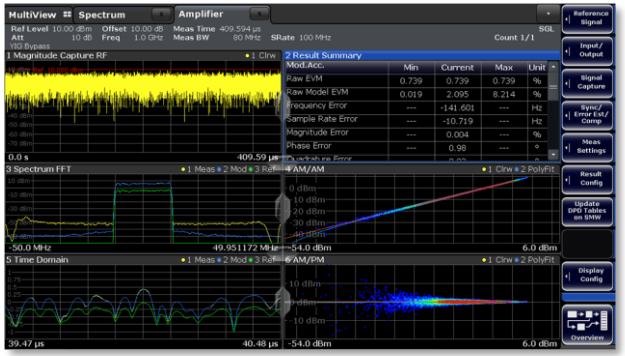
YOUR TASK



cadence®

COLLECTING DATA ON A REAL POWER AMPLIFIER



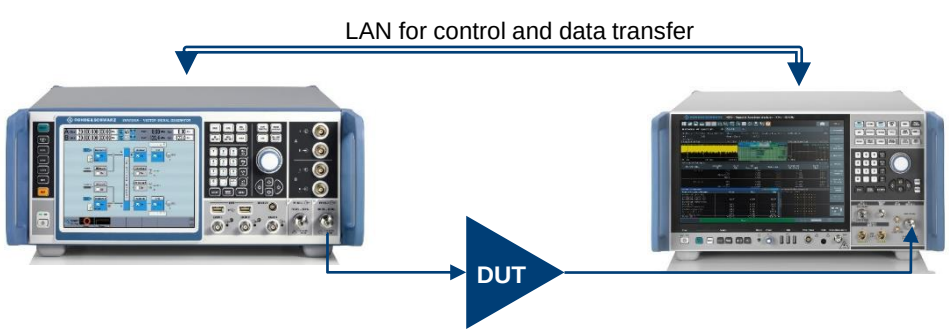


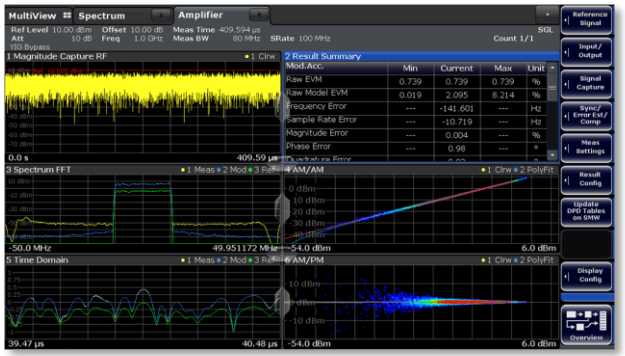
R&S®FSW-K18D Direct DPD

- Iterative approach
- Compensates for memory effects
- Excellent performance especially for amplifiers with memory effects

- Reference for best possible
  - Suppliers typically do not have access to DPD algorithms used by system integrators

CREATING THE MEMORY POLYNOMIAL DPD IN FSW





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R&S®FSW-K18M memory polynomial

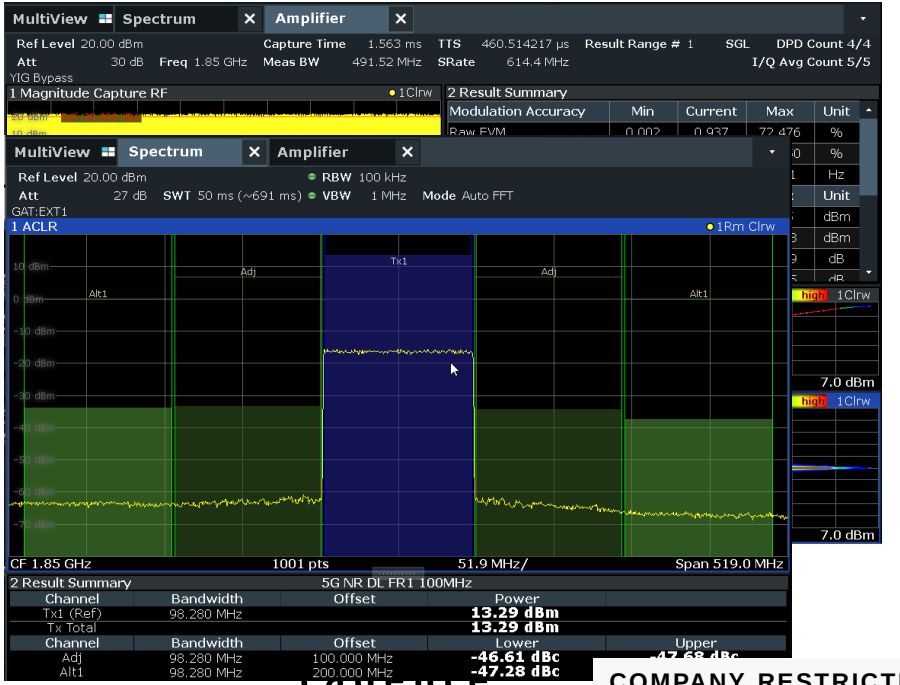
- Memory polynomial model based on Direct DPD result
- Modeling can be adopted in order and memory depth
- Model verification on DUT

- Proves easy linearization of RFFE solution

COMPARISON
SIMULATION VS. MEASUREMENT

Measurement and pre-distortion all PC-based (RF simulation + signal analysis)

Measurement and pre-distortion on physical device



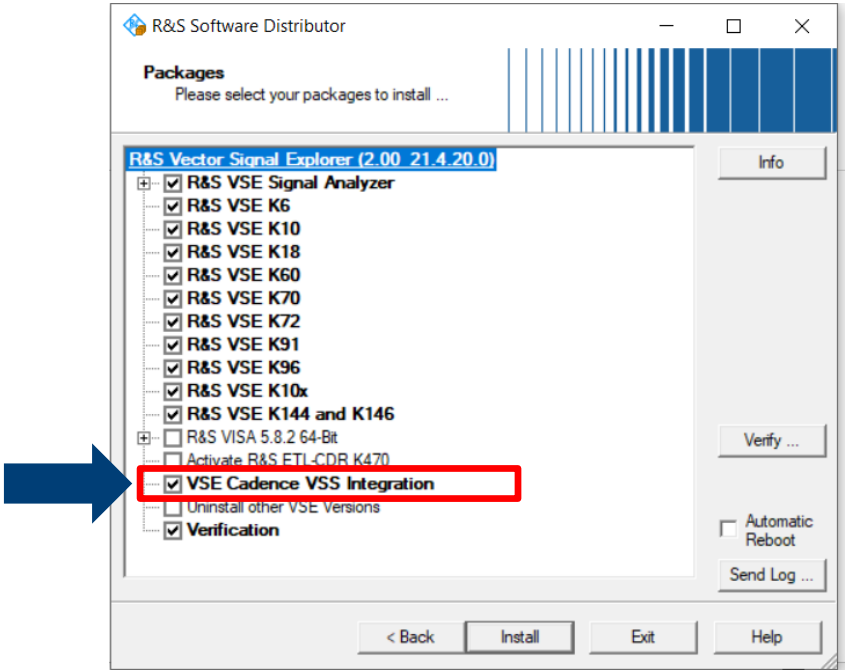
SUMMARY AND CALL FOR ACTION

HOW TO GET IT

- **R&S VSESIM-VSS**, sold by R&S
- Latest version V17 of Cadence AWR VSS, sold by Cadence

- New R&S software product
  - 12 month license
  - All future updates, extensions and standards included

- 1 license VSESIM-VSS enables all WinIQSIM2 and VSE standards and features
- USB dongle or new software license for license server (in line with Cadence approach)



SUMMARY

- First pass design through real target application signals
- Direct DPD to verify linearization possibilities already in simulation
- Streamlined process from design to implementation
- Correlation is given from simulation to real world test by applying same signals and demodulation
- Hardware in the loop to verify subset implementation complemented by simulation for system level verification
- Link to further Cadence tools through VSS

… more than 1 + 1: cadence® & 

Find out more

www.rohde-schwarz.com

Thank you!

ROHDE&SCHWARZ

Make ideas real