R&S 5G FR1 Power Amplifier Seminar

5G Doherty PA Design and Measurement

Clement POTIER – Staff MMIC Designer

29/06/2023

Outline

- **Introduction**
  - New challenges in PA design
  - iCana's profile
- **Different PA topologies for complex telecom signals**
  - Review on amplification classes
  - Efficiency VS linearity
  - AB class PAs, LMBA, Outphasing, Doherty,…
- **Basics of Doherty**
  - Load modulation
  - Matching and lambda/4
  - Importance of phase distribution
  - sizing
- **Doherty design examples**
  - Ideal structures and product variants
  - Design tips
- **Back in the lab**
  - iCana's setup in today's booth
- **Doherty PA FR1 catalog of iCana**
- **Conclusion**

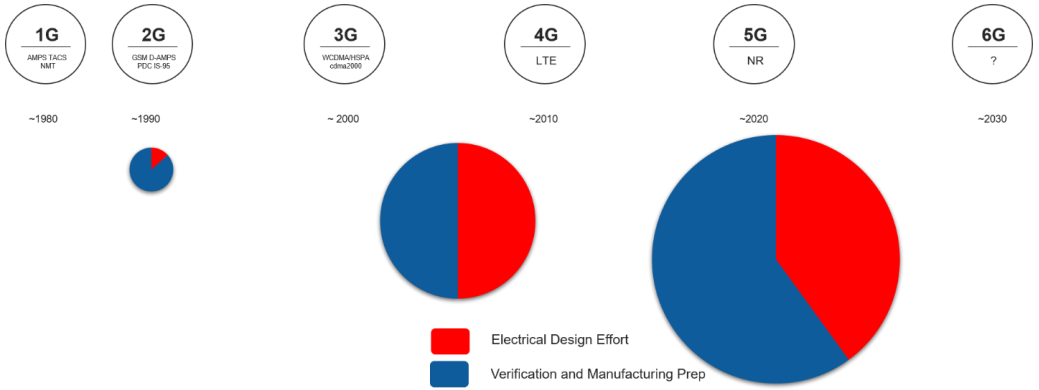
A World of Data

- IOT, augmented reality, connected cars, … => Need for more bandwidth, higher data rate, higher output power, higher integration, better efficiency… **But always with the best linearity!**
- 5G Radio Access Network (RAN): a new architecture enabling us to achieve these goals, but chips' architecture also need to re-invent themselves while staying cost competitive
- PA designers will be able to play with different leverages:
  - Active components semiconductor process
  - Biasing techniques
  - Exotic amplification classes
  - Load modulation
  - Packaging co integration

$$\text{Nyquist Bit Rate} = 2 \times BW \times \log_2 L$$

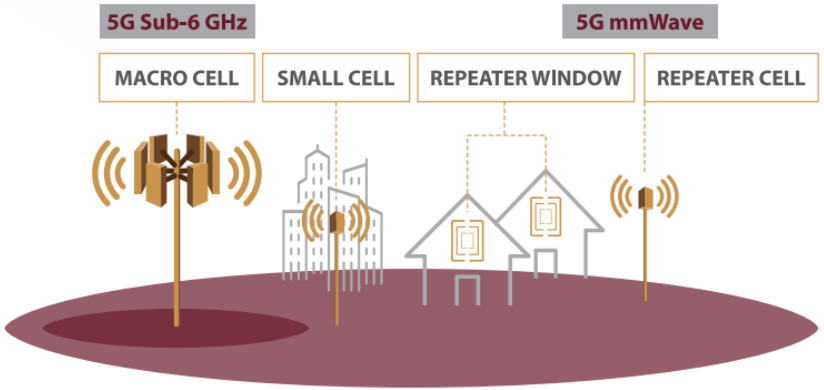
BW = Bandwidth

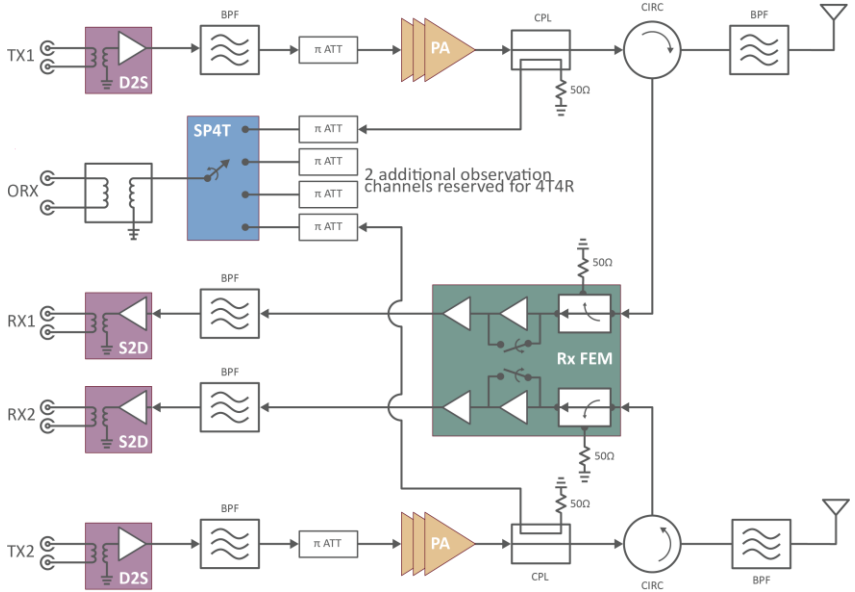
L = Signal Levels or Bits per Symbol



iCana's Profile

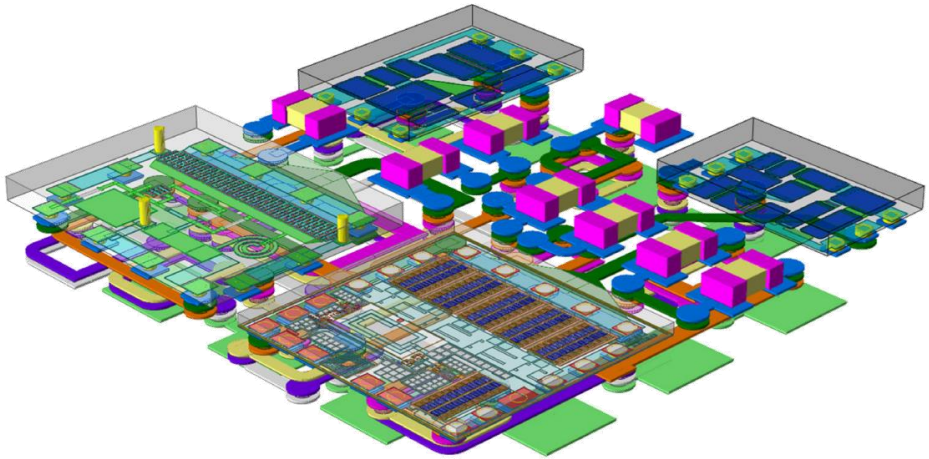
- iCana is a fabless semiconductor component supplier specializing in design and manufacturing of RF components for wireless communication. Our primary markets are 5G NR FR1 and FR2 infrastructure together with automotive connectivity





PA Design Must Comply With New Standards And Modulations Signals

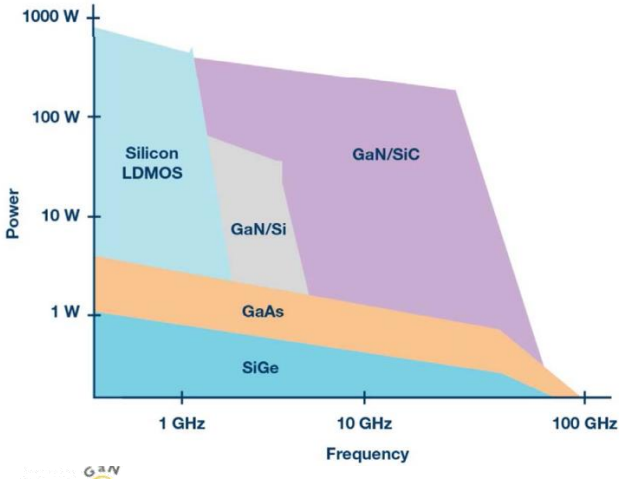
- **CAD design tools to help achieve best performances and multi-chip integration**
  - Small signal
  - High power
  - Linearity
  - Multi technology
  - Packaging
  - 3D EM
  - LVS / DRC
  - Sensitivity / Montecarlo

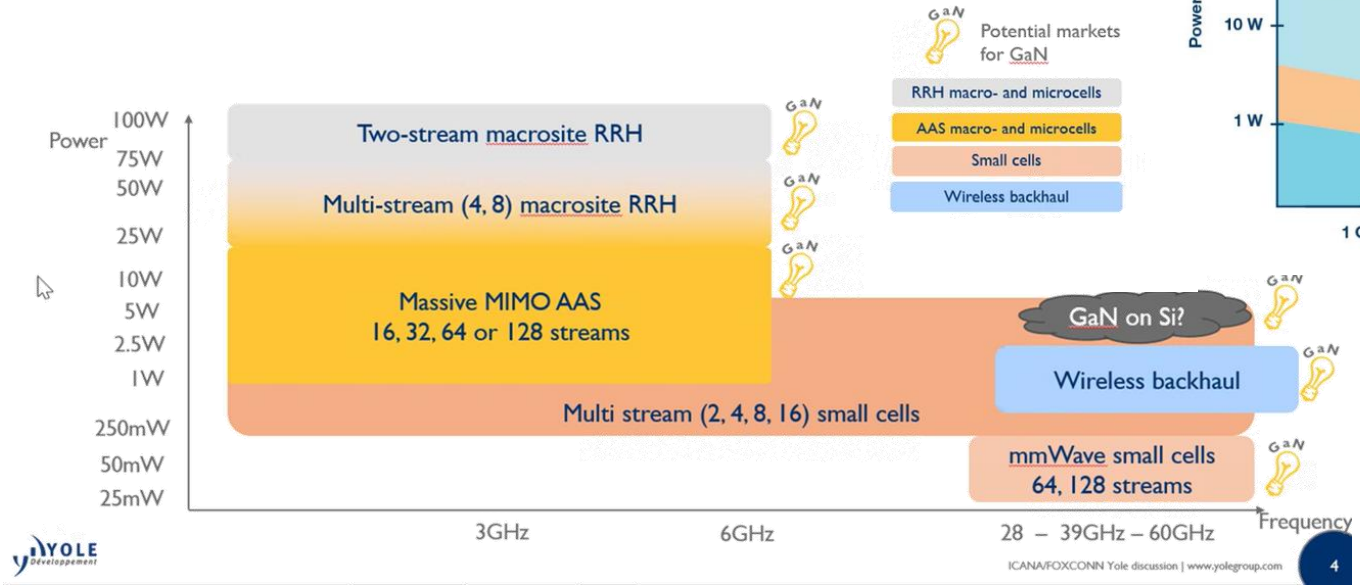


- **Higher order modulation**
  - ➔ 802.11be supports up to 4096-QAM! (WiFi 5 “only” 256-QAM”)
  - Circuit envelope simulator
- **Higher Peek to Average Ratio (PAR)**
  - Design for higher Psat
  - Design for higher backoff efficiency
  - Harmonic balance / Intermod
- **Higher bandwidth but avoid signal coexistence and spectrum sharing**
  - Strong gain flatness
  - Sharp gain profile
  - Harmonics rejection and dedicated filtering

Designers' Choice – Technology / Process

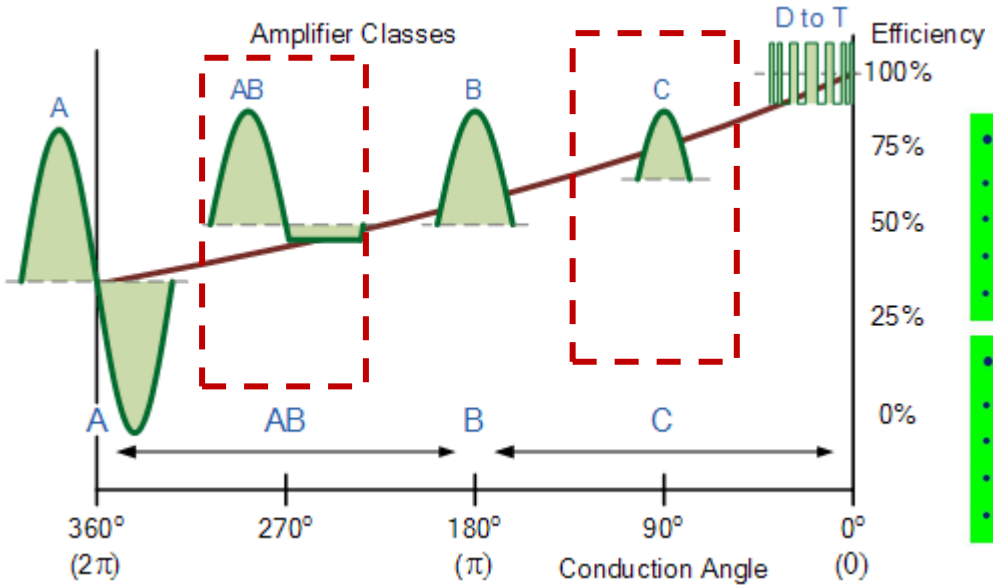
- Depending on the targeted power, voltage biasing availability, integration and cost several options can be picked
- ***GaN/Si a game changer?***





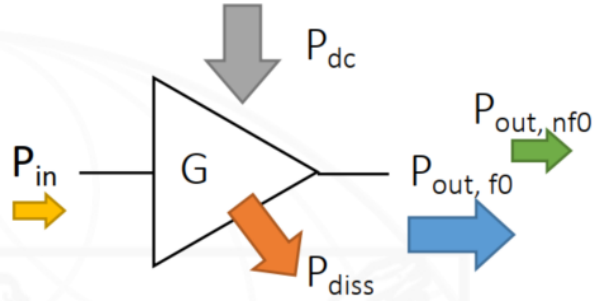
Designers' Choice – Amplification Class

- "Conventional" classes or high efficiency classes using harmonics and waveform shaping (Class F, F^{-1},..), switching devices (D, E), compensation network (J)



- **Class A**
  - Ultra Linear Amplifier
  - Extremely High Power Gain
  - Low Efficiency (50% max)
  - Conduction Angle 360°
- **Class B**
  - Non-Linear Amplifier
  - Low Power Gain
  - High Efficiency (78.5%)
  - Conduction Angle 180°
- **Class AB**
  - Linear Amplifier
  - High Power Gain
  - Medium Efficiency (50-78.5%)
  - Conduction Angle 180-360°
- **Class C**
  - Extremely Non-Linear Amplifier
  - Extremely Low Power Gain
  - Extremely High Efficiency (90%)
  - Conduction Angle <180°

By The Way How To Define Efficiency ?



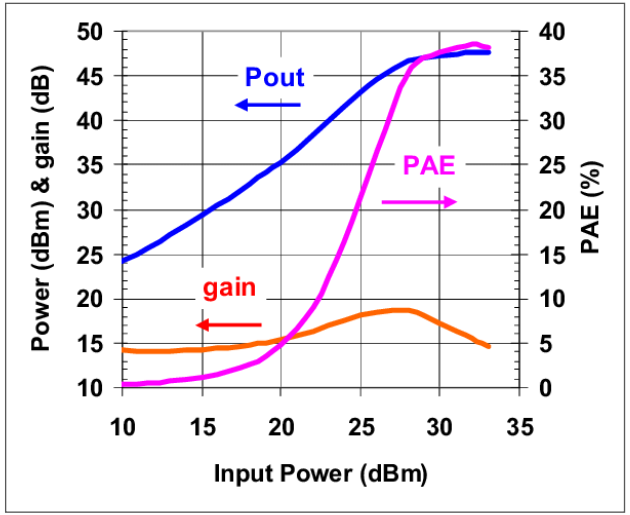
$$P_{dc} = P_{diss} + P_{out,f} + \sum_{n=2}^{\infty} P_{out,nf}$$

$$\eta = \frac{P_{out,f}}{P_{dc}} = \frac{P_{out,f}}{P_{diss} + P_{out,f} + \sum_{n=2}^{\infty} P_{out,nf}}$$

No overlap between voltage and current

No power delivered at harmonics

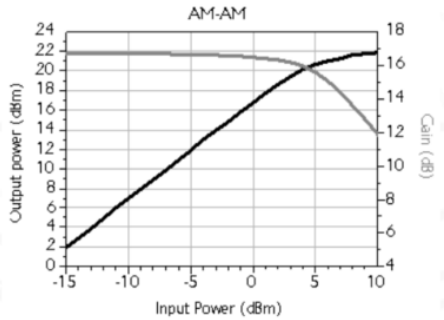
$$PAE(\%) = \left(\frac{P_{out} - P_{in}}{P_{DC}}\right) \times 100$$

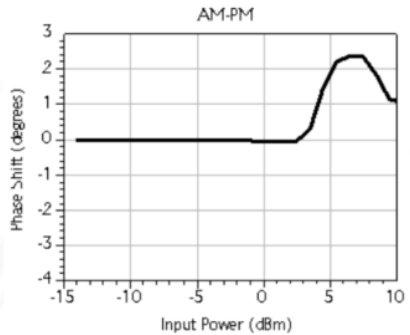


… And Linearity ?

- Biasing, physical effects in the semiconductor, gain compression, intermodulation,… are sources of linearities

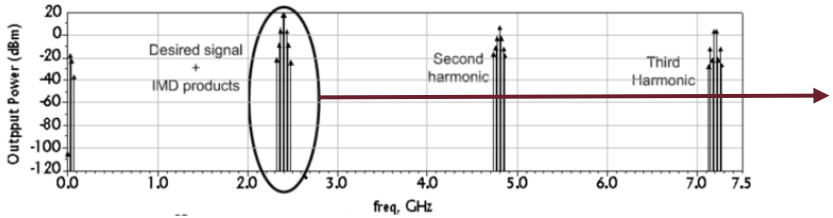
- In band distortion
  - Gain compression
  - Trapping effects
    - ➔ EVM, OP1dB, AM/AM, AM/PM

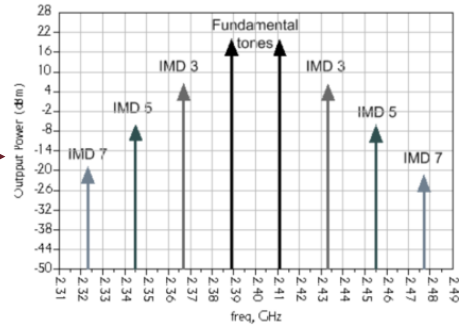




- Out of band distortion
  - Harmonics
  - Intermodulation
    - ➔ OIP3, ACLR

Example of 2 tones response





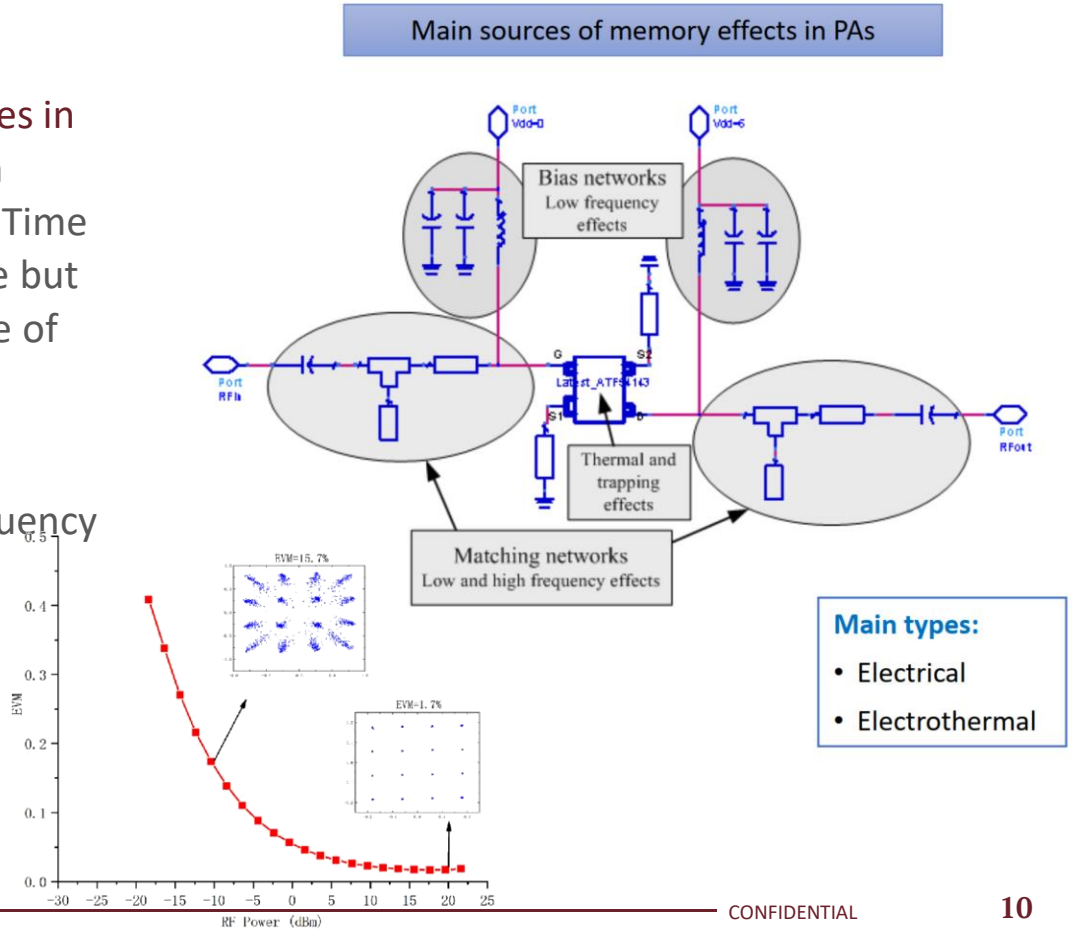
Nonlinear Behaviour Caused By Memory Effects

Description

The memory effects are defined as changes in the amplitude and phase of the distortion components, due to the previous signals. Time responses are not instantaneous anymore but will be convolved by the impulse response of the system

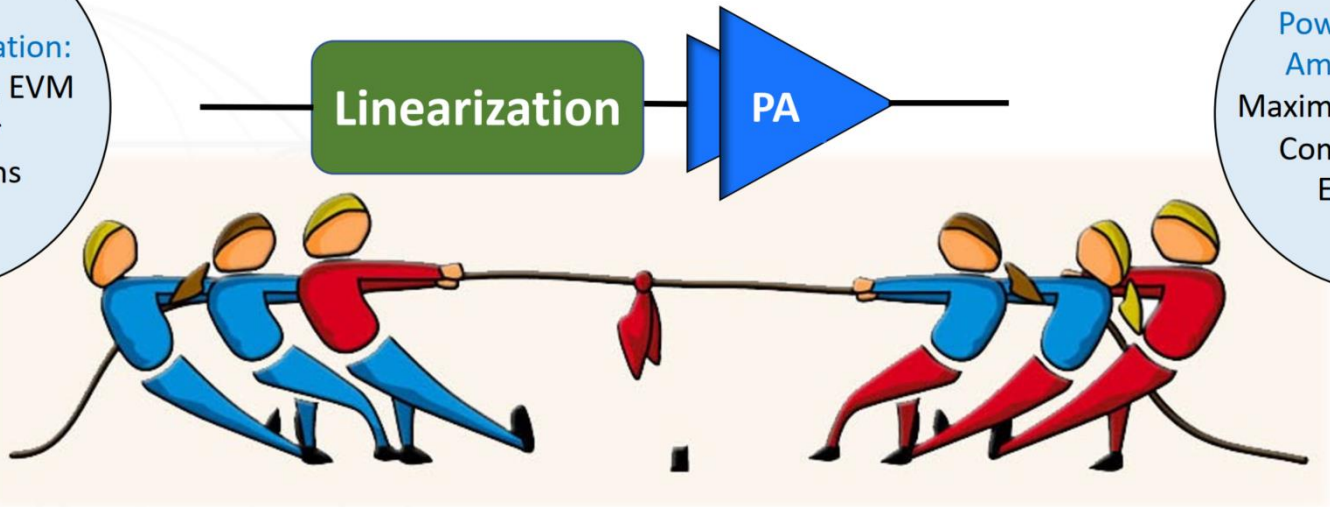
They appear as:

- Asymmetries in the IMD products (frequency domain)
- Dispersion in the decision points of the constellation (time domain)



Efficiency vs. Linearity

Linear Amplification: Meet the ACPR, EVM and Power specifications



Power Efficient Amplification: Maximize Power and Computational Efficiency

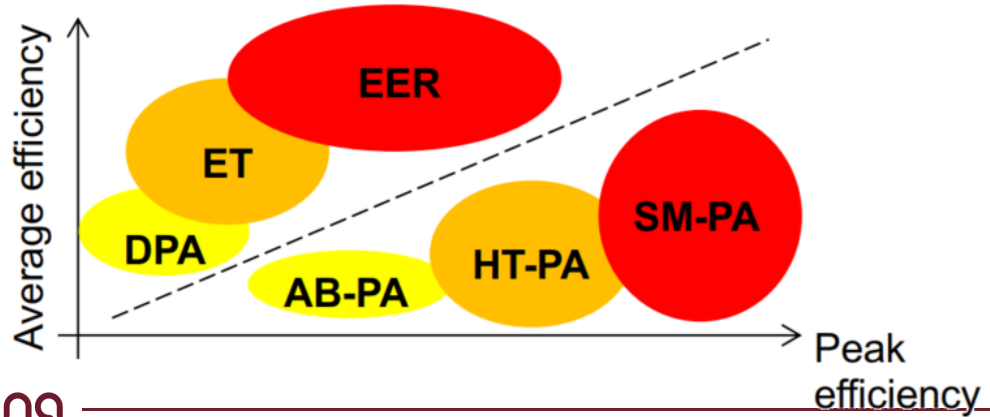
We want:
High data rates everywhere/everytime

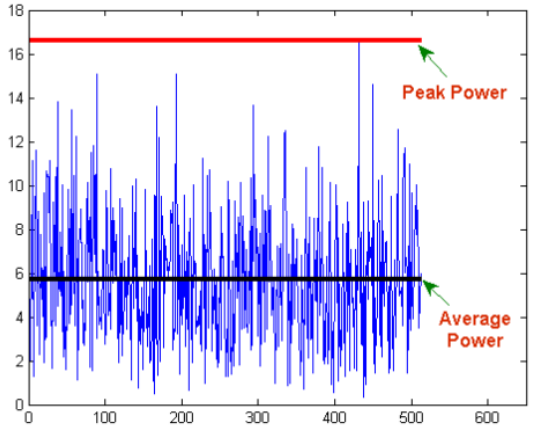
We need:
High SNR Tx. → Linear amplification of spectrally efficient modulation schemes

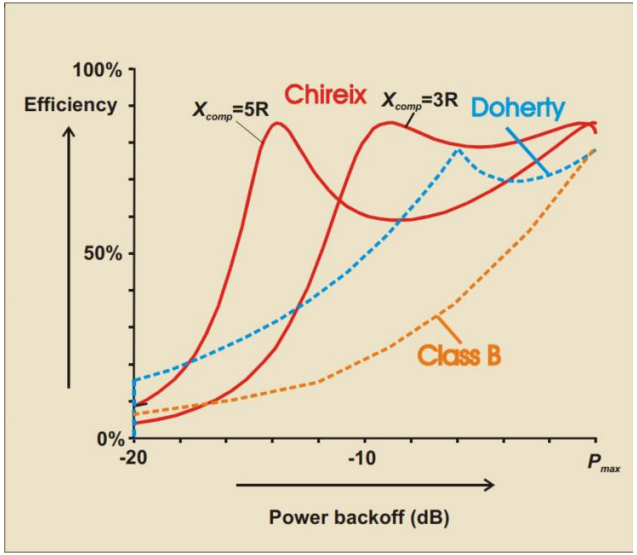
We have to cope with:
- Wide bandwidth signals
- High PAPR signals (OFDM-based)
- Concurrent multi-band and MIMO Tx.

Designers' Choice – PA Topology

- 5G modulated signals present non constant envelope with high PAPR ratios
  - ➔ We need good efficiency at high power and backoff
- Several PA topologies were investigated since several years to address these trade-offs
  - Load Modulated (Doherty, Chireix, Balanced,…), Envelope Tracking, Harmonic Tuning, Switch mode, …
  - Trade-off between performances and PA complexity

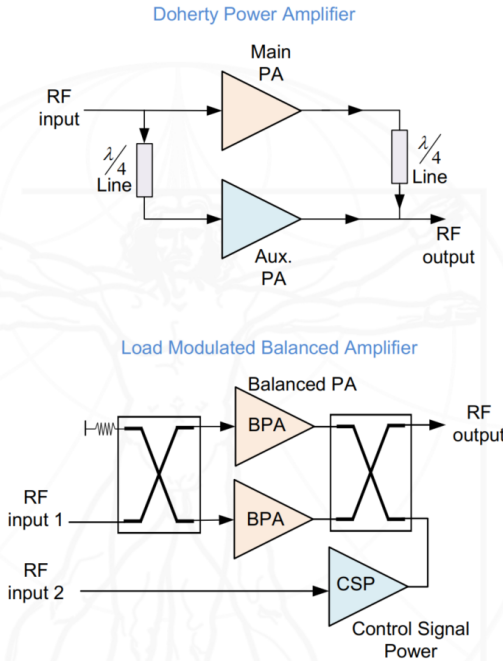


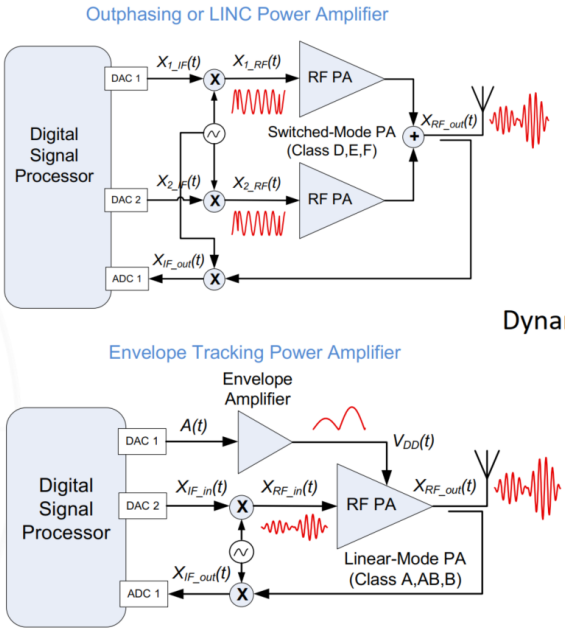




Designers' Choice – PA Topology

- Several PA topologies were investigated since several years to address these trade-offs
  - Load Modulated (Doherty, Chiriex, Balanced,…), Envelope Tracking, Harmonic Tuning, Switch mode, …
  - Trade-off between performances and PA complexity





High Efficient Amplification Architectures

Dynamic { ▪ Load ▪ Supply } Modulation

- Linearization techniques
- CFR techniques

How To Choose? With The Specs!

- Standards define the appropriate levels
  - 3GPP, small cells consortiums, ..
  - Define the modulated schemes and signals
  - Define the required linearity and output power for each frequency bands
- Market
  - System line-ups
  - Overall costs, footprint, design time
  - Regions specificities

Doherty Seems Interesting, Let's Have A Look!

- Invented by W. H. Doherty at the Bell Labs in 1936
- The Doherty architectures propose to use 2 parallel power cells, to try to maintain a constant saturation level of the total PA, thus a high efficiency

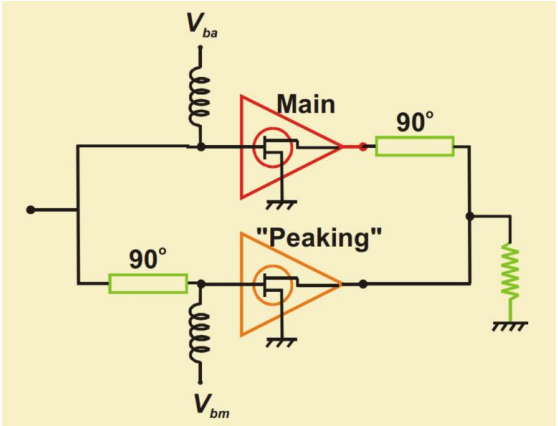
  This can be achieved by several key parameters :

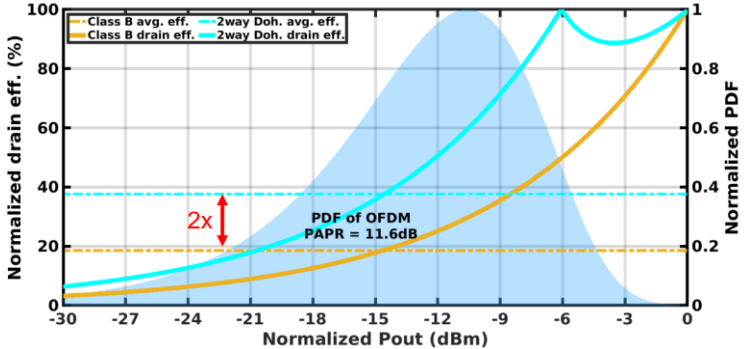
  - One power cell (Carrier / Main) acts as normal PA with high efficiency at saturation, then needs to see a different load with the increasing Pin/Pout

  ➔ Use another amplifier like in active load pull

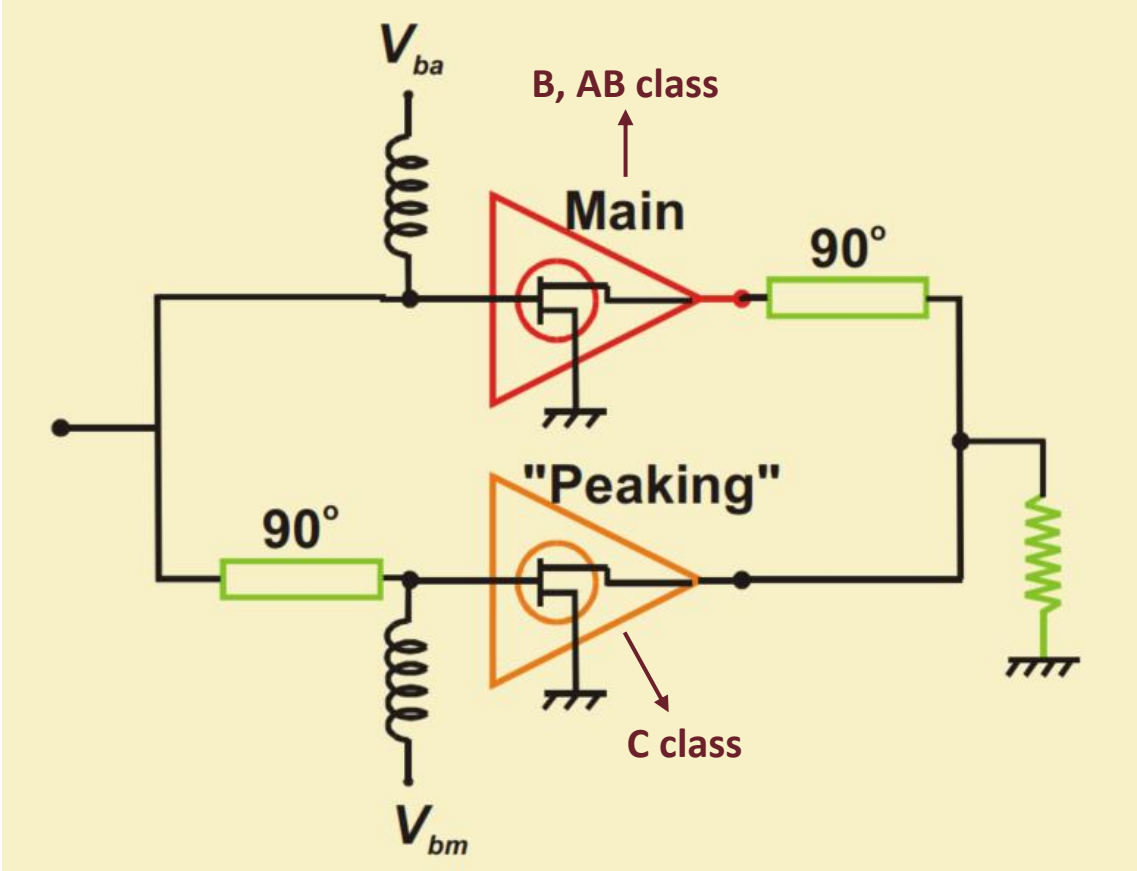
  - The other power cell (peaking / auxiliary) will not be "active" at low power ➔ Class C
  - Keep voltage swing constant to keep efficiency constant

  ➔ Impedance Inverter Network in between



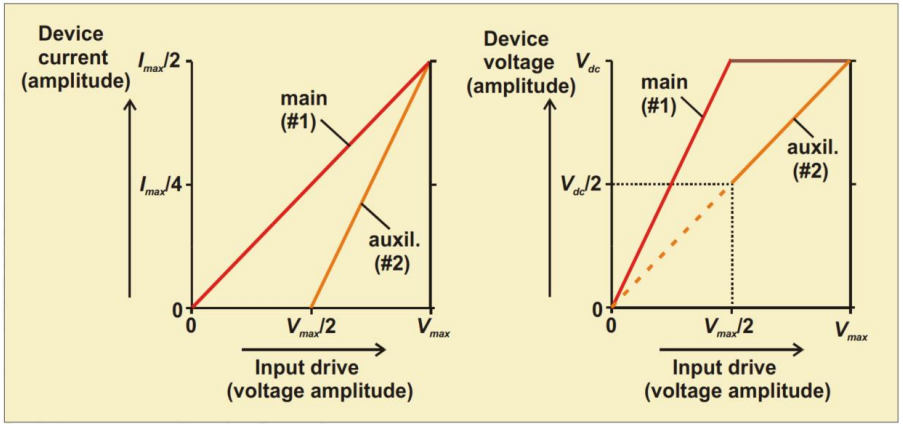


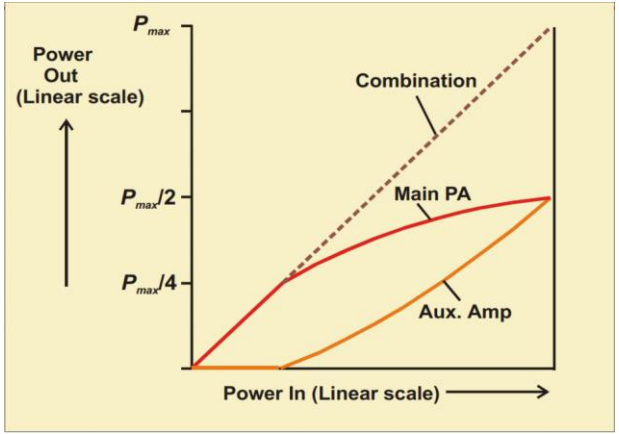
The Doherty Amplifier Basics (1/7)



The Doherty Amplifier Basics (2/7) – Keep Constant $Vout_M$

- If we consider a class B amplifier for the Main, $Vout_{Max}$ = Vdd – Vk
- Thus efficiency is $\eta = \frac{\pi}{4} \cdot \frac{Vout}{Vdd}$, if the load is constant, efficiency will change as collector Voltage will change with current increase
- If we can modulate the load such as Vout stays constant and only Ic increases with Pin/Pout then the efficiency shall remain constant

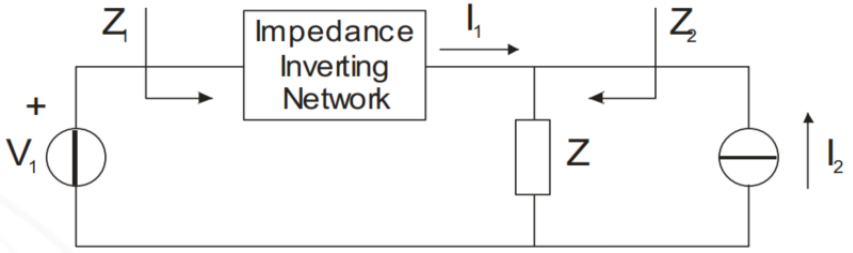


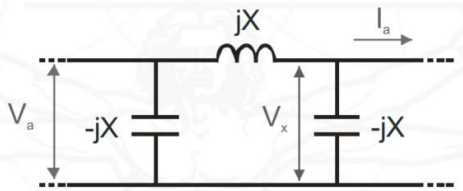


The Doherty Amplifier Basics (3/7) – Lambda/4 Section

- But then the 2 power cell must operate with independent voltage swings!

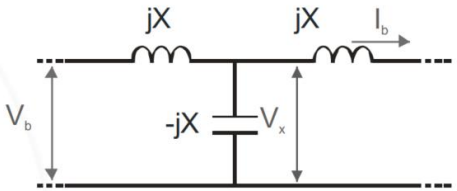
➔ Need to design an Impedance Inverter Network to isolate both of them





$$I_a = \frac{V_a - V_x}{jX} - \frac{V_x}{-jX} = \frac{V_a}{jX}$$

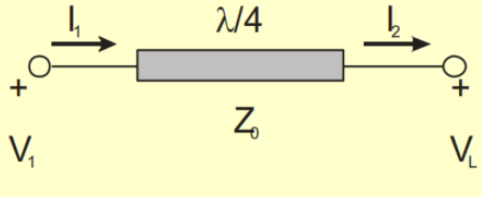
$$R_a = \left[R // (-jX) + jX\right] // -jX = \frac{X^2}{R}$$



$$I_b = \frac{V_b - V_x}{jX} - \frac{V_x}{-jX} = \frac{V_b}{jX}$$

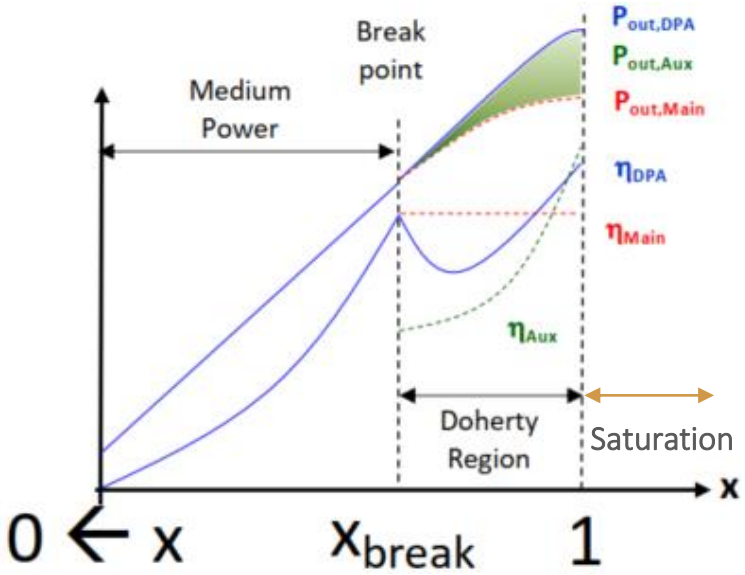
$$R_b = (jX + R) // (-jX) + jX = \frac{X^2}{R}$$

- One of the bandwidth limitation…



$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} 0 & j \cdot Z_0 \\ \dfrac{j}{Z_0} & 0 \end{pmatrix} \cdot \begin{pmatrix} V_L \\ I_2 \end{pmatrix}$$

The Doherty Amplifier Basics (4/7) – OBO Definition



$$OBO = 10 \cdot log_{10}\left(\frac{P_{out,Main}\big|_{x=x_{break}}}{P_{out,Main}\big|_{x=1} + P_{out,Aux}\big|_{x=1}}\right)$$

- We define :

$$\alpha = \frac{P_{out,Main}\big|_{x=x_{break}}}{P_{out,Main}\big|_{x=1}} = \frac{I_{1,Main}\big|_{x=x_{break}}}{I_{1,Main}\big|_{x=1}} \qquad \alpha = 10^{-\frac{OBO}{20}}$$

$$P_{out,DPA}\big|_{x=1} = \frac{1}{\alpha} \cdot P_{out,Main}\big|_{x=1}$$

$$I_{1,Aux}\big|_{x=1} = \frac{1-\alpha}{\alpha} \cdot I_{1,Main}\big|_{x=1}$$

- If OBO increases:
  - ➔ Aux power cell size increases vs. Main size
  - ➔ Aux bias point shift from deep class C towards class B

The Doherty Amplifier Basics (5/7) – Power Cells Sizing

- Starting from the required DPA output power $P_{out,DPA}$, and OBO, the Main device can be sized

$$\alpha = 10^{-\frac{OBO}{20}}$$

$$P_{out,Main}\Big|_{x=1} = \alpha \cdot P_{out,DPA}\Big|_{sat}$$

Selecting normalized bias point ξ (designer parameter)

$$\xi = \frac{I_{DC,Main}}{I_{Max,Main}}$$

$$I_{1,Main}\Big|_{x=1} = \frac{P_{out,DPA}\big|_{sat}}{\frac{1}{\alpha}\frac{1}{2}(V_{DD}-V_k)} = \frac{I_{Max,Main}}{2\pi} \cdot \frac{\theta_{AB} - sin(\theta_{AB})}{1 - cos\left(\frac{\theta_{AB}}{2}\right)}$$

$$\theta_{AB} = 2 \cdot acos\left(\frac{\xi}{\xi - 1}\right)$$

- The parameter identifying the Doherty region x_{break} can be inferred by solving the equation

$$x_{break}[\theta_{break} - sin(\theta_{break})] = \alpha[\theta_{AB} - sin(\theta_{AB})]$$

By using ➔ $cos\left(\frac{\theta_{AB}}{2}\right) = x_{break} \cdot cos\left(\frac{\theta_{break}}{2}\right)$

$$\theta_C = 2 \cdot acos(x_{break})$$

- The Aux device can be sized $I_{Max,Aux} = I_{Max,Main} \cdot \frac{1-\alpha}{\alpha} \frac{1 - cos(\theta_C)}{\theta_C - sin(\theta_C)} \cdot \frac{\theta_{AB} - sin(\theta_{AB})}{1 - cos(\theta_{AB})}$

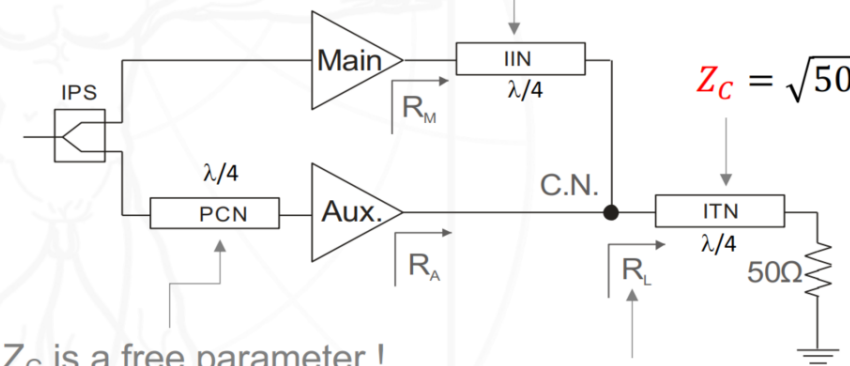
- The "virtual" bias point for the Aux device can be estimated $I_{DC,Aux} = -I_{Max,Aux} \cdot \frac{x_{break}}{1 - x_{break}}$

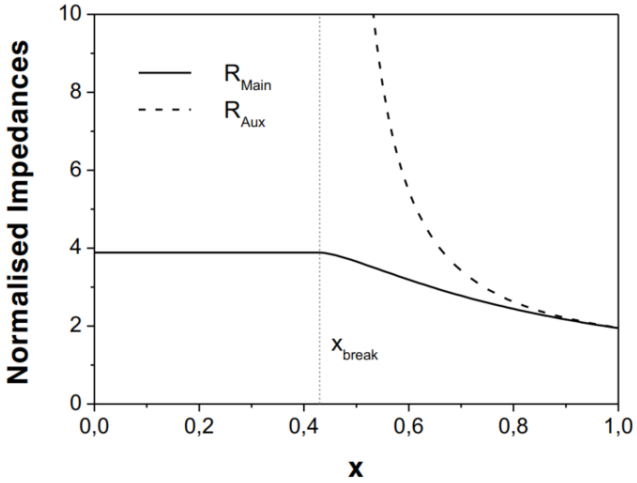
The Doherty Amplifier Basics (6/7) – Defining The Loads

- The DPA output design parameter can be inferred

$$R_{M,sat} = \frac{V_{DD} - V_k}{I_{1,Main}\big|_{x=1}} \qquad R_{M,break} = \frac{1}{\alpha} R_{M,sat}$$

$$R_{A,sat} = \frac{V_{DD} - V_k}{I_{1,Aux}\big|_{x=1}}$$





The Doherty Amplifier Basics (7/7) – Trade-Offs

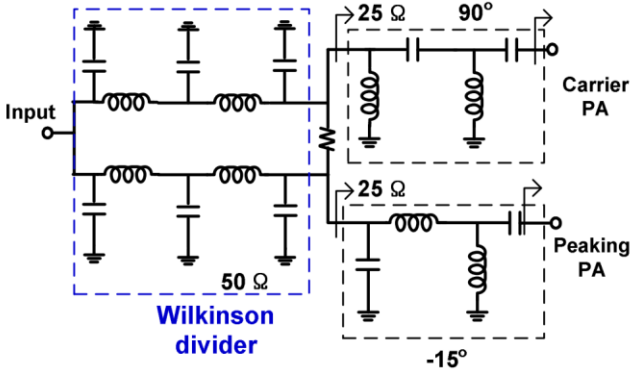
< 6 GHz

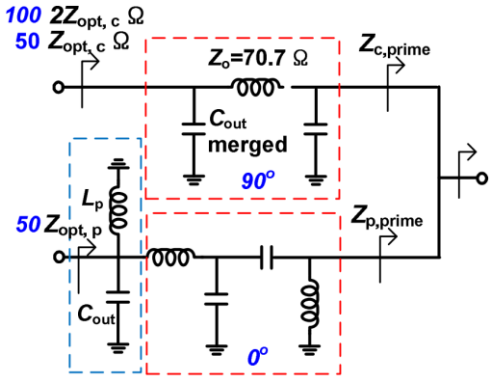
- Parallel combination of transistor fingers (power bars)
  - Negligible de-phasing
- Series combination of transistors (stacking)
  - Little interstage matching needed
  - Stability
- Combination at PA level
  - Off-chip
  - On-chip

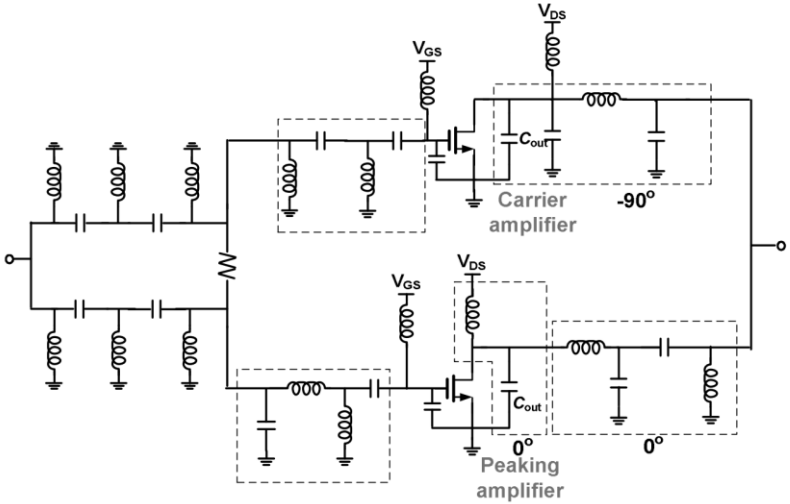
> 6 GHz

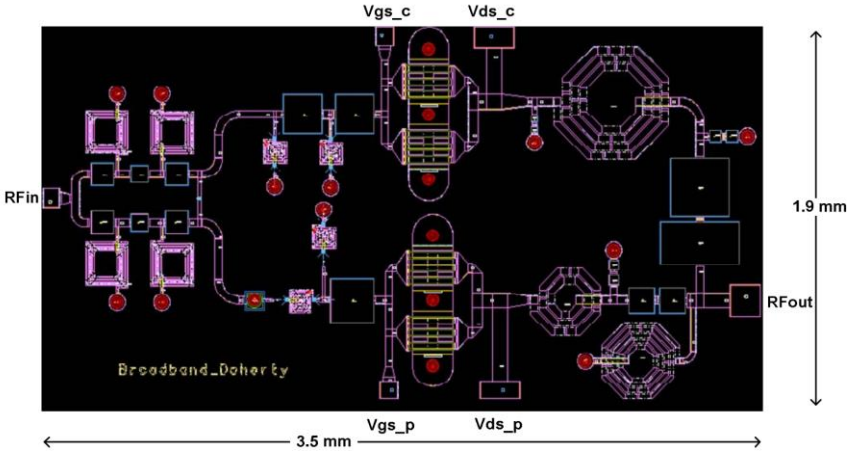
- Parallel combination of transistor fingers (power bars)
  - Significant de-phasing
- Series combination of transistors (stacking)
  - Complex interstage matching needed
  - Stability
- Combination at PA level
  - Off-chip
  - On-chip

The Doherty Amplifier – Ideal Example

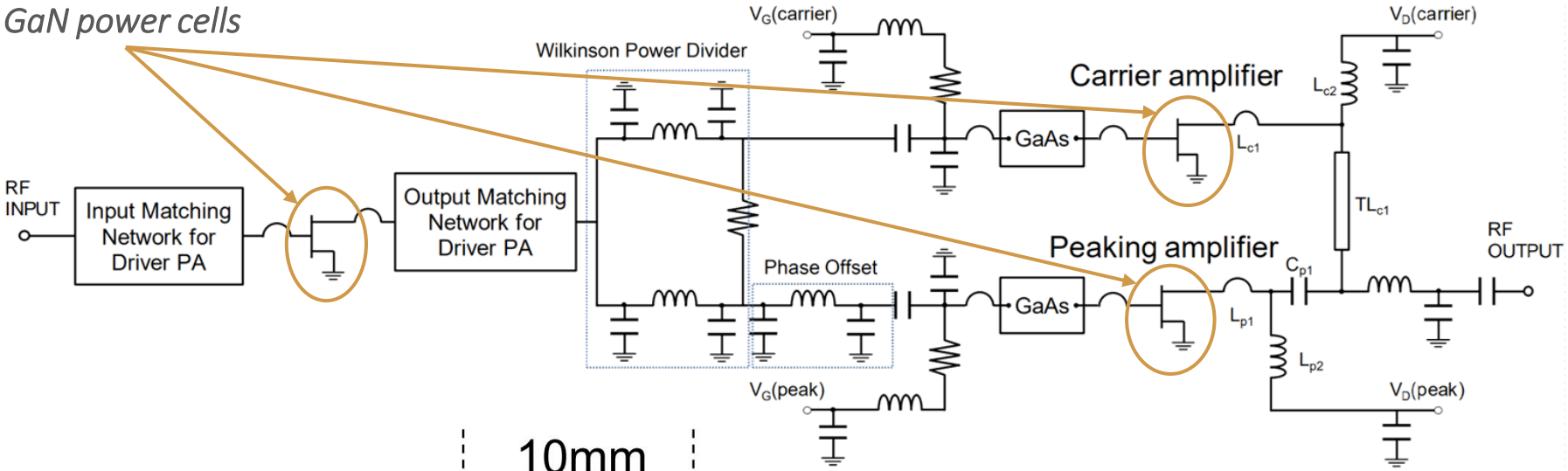


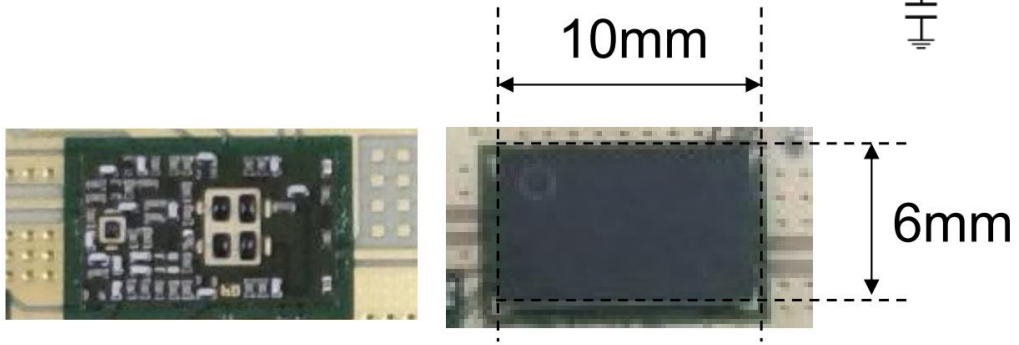




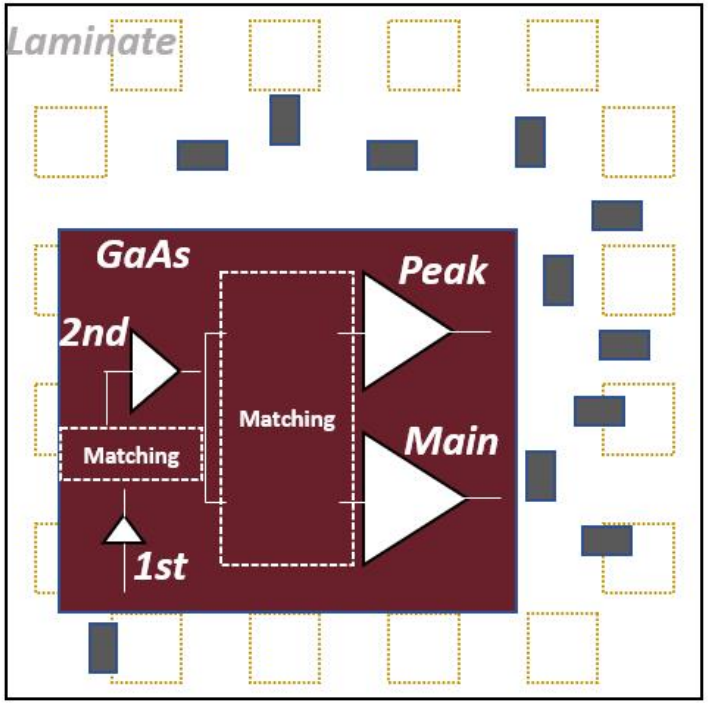


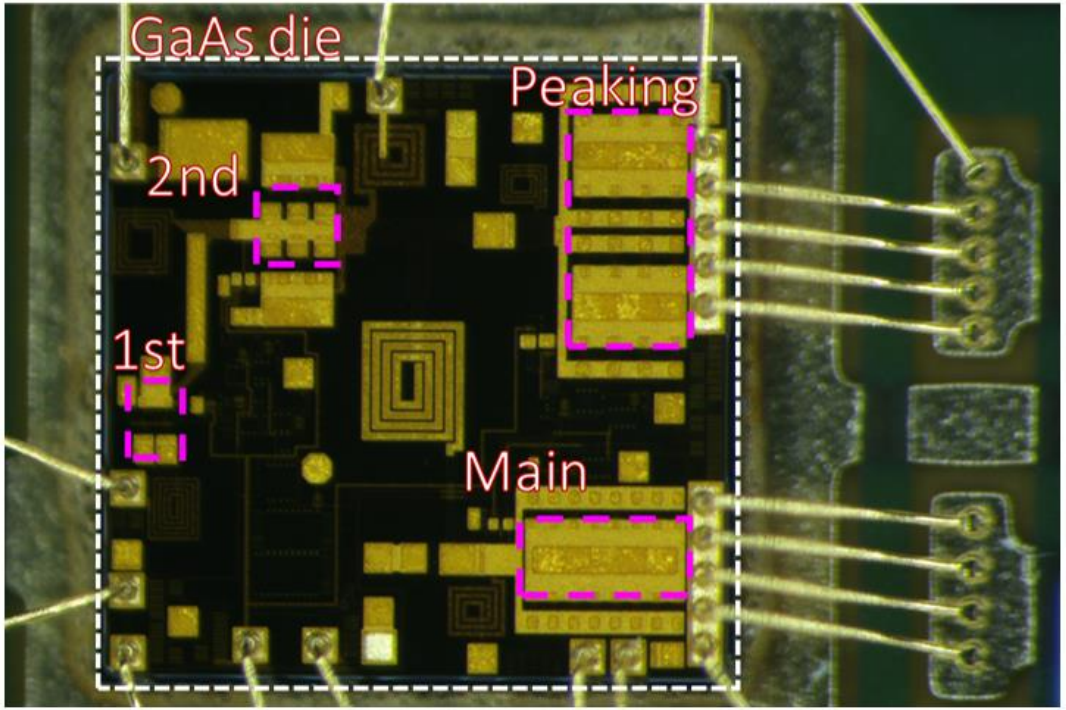
The Doherty Amplifier – Ideal Example Driver And Hybrid





The Doherty Amplifier – Ideal Example Driver And Hybrid

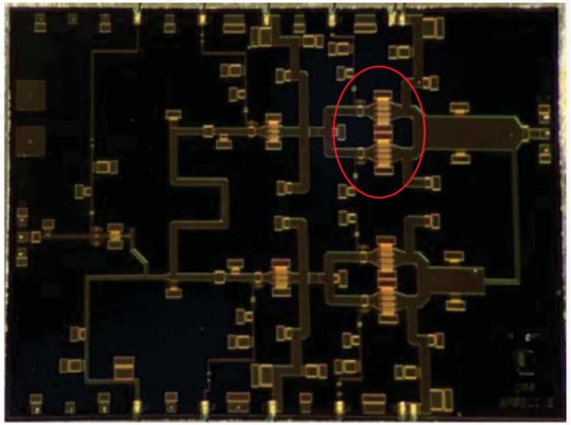




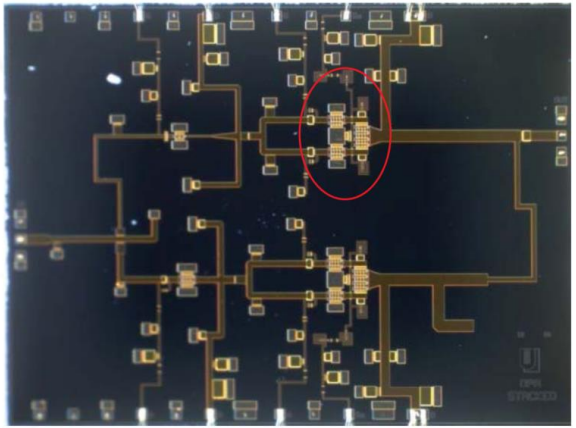
MMIC Solutions For Higher Frequencies

17.3-20.3 GHz

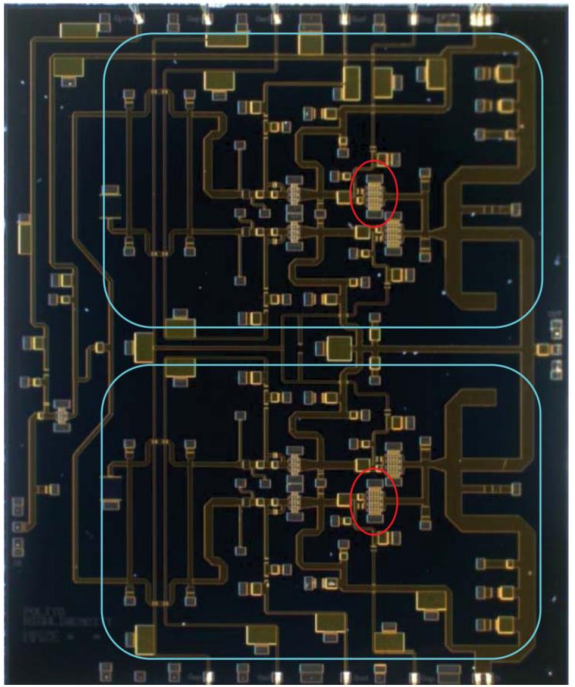
ESA ITT AO/1-9088/17/NL/HK
Single Chip Ka-Band Doherty Amplifier



transistors
in parallel



transistors
in series



DPA cells
in parallel

The Doherty Amplifier – Design For Real 5G FR1 Product

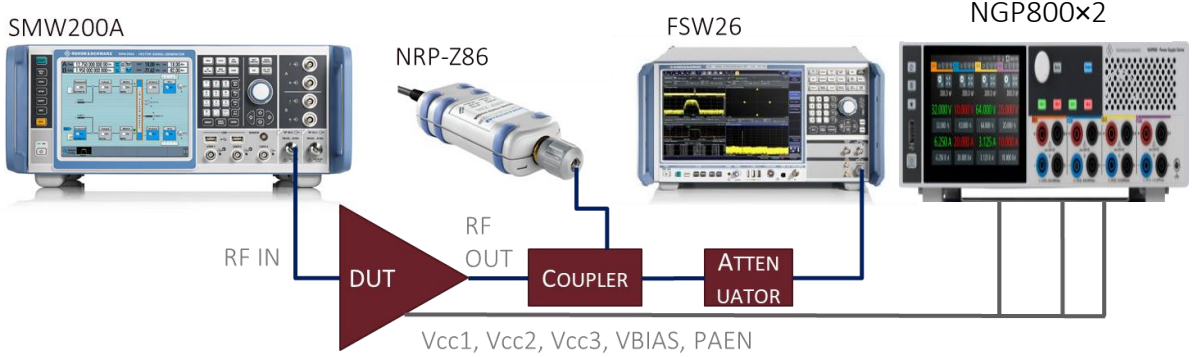
- The PA must be cost competitive so hybrid solutions in over-molded packages are the best approach
- Several topologies with one driver followed by one splitter or one splitter followed on each branch by a driver then the Doherty power cell, uneven divider, uneven power cells, die bar + matching, pre-matched cells,…
- Variants of Doherty, inverted, multi-way
- All the parasitic must be taken in account as the phase is critical ➔ need for complex simulation benches and cosimulations with packages and different process in one module
- Bond wires need to be included
- Electro thermal simulations and accurate thermal / trapping models are needed

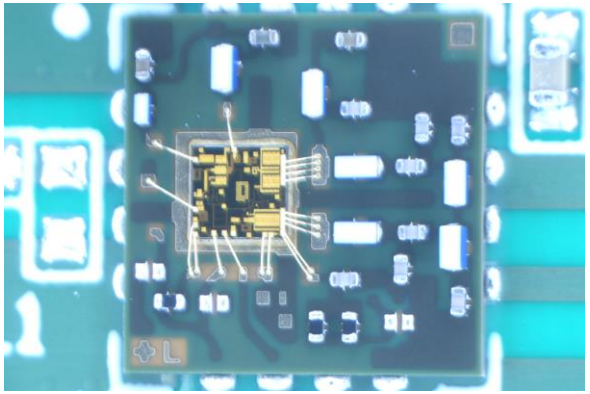
The Doherty Amplifier – Design For Real 5G FR1 Product

- Active biasing technics aligned with process variations are mandatory, especially for HBTs
- IMD3 simulations with different tone spacings
- Envelope simulations with 3gpp standard input signals
- Raw ACLR < -35dB to achieve -50dB after DPD
- All of that to … tune in the lab after manufacturing!

Back In The Lab – iCana's Booth Setup

- Large Signal Test Setup Diagram and non-overmolded DUT
- Modulated Signal: 5G NR, FDD, TM3.1, scs = 30kHz, Bandwidth = 1 × 100 MHz, PAR = 8.5 dB
- Frequencies: 3.45, 3.55, 3.65 GHz
- $V_{cc1} = V_{cc2} = V_{cc3} = V_{BIAS} = 5.0$ V, $V_{PAEN} = 2.0$ V



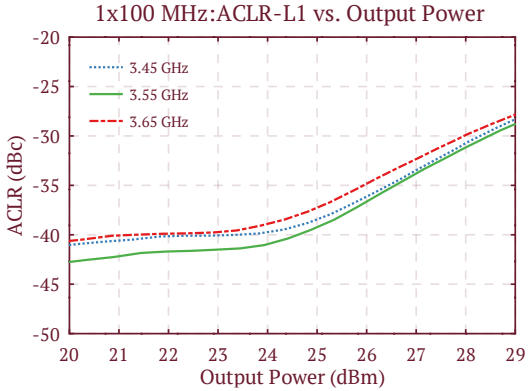


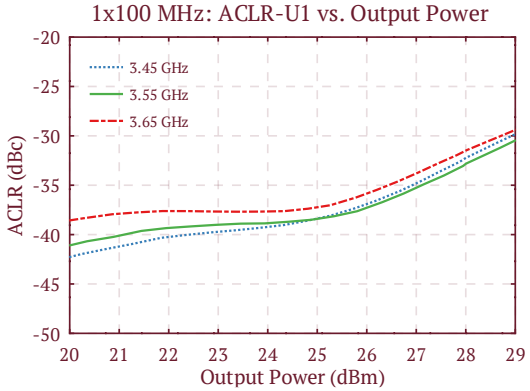
Back In The Lab – Measured Result

Back In The Lab – Measured Result

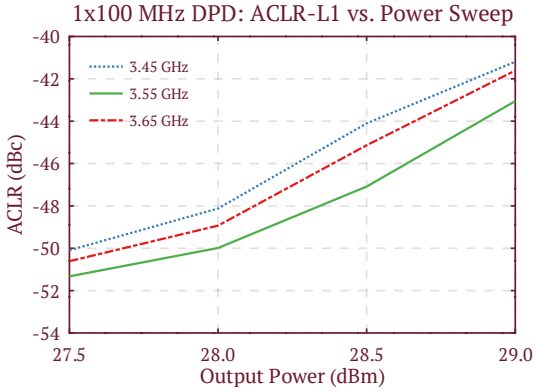
- ACLR-L1 & ACLR-U1 vs. Output Power with / without DPD

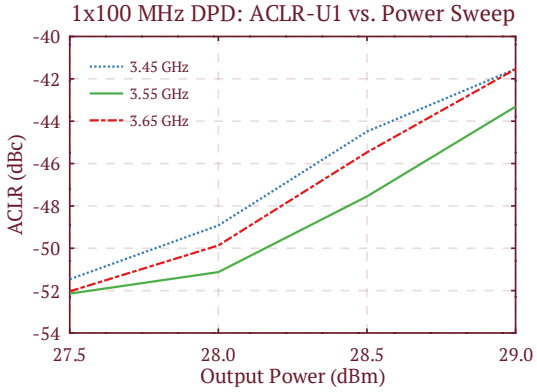
Raw ACLR





ACLR after DPD





iCana's Doherty PA Portfolio For 5G FR1

4 W High-Efficiency Power Amplifiers

Part Number	Frequency Range (GHz)
ARQSP1819-4	1.8 – 1.9
ARQSP2122-4	2.1 – 2.2
ARQSP2324-4	2.3 – 2.4
ARQSP2527-4	2.5 – 2.7
ARQSP3336-4	3.3 - 3.6
ARQSP3437-4	3.4 – 3.7
ARQSP3742-4	3.7 – 4.2
ARQSP4450-4	4.4 – 5.0

8 W High-Efficiency Power Amplifiers

Part Number	Frequency Range (GHz)
ICASP3338-8	3.3 – 3.8
ICASP3742-8	3.7 – 4.2
ICASP4450-8	4.4 – 5.0

20 W High-Efficiency Power Amplifiers

Part Number	Frequency Range (GHz)
ICASP3338-20	3.3 – 3.8
ICASP3742-20	3.7 – 4.2
ICASP4450-20	4.4 – 5.0

Conclusions

- 5G and new communications are always pushing for more power/efficiency/linearity
- There will always be trade-offs, pushing the efforts towards designers, foundries to develop innovative structures who need back strong support and innovative tools and instruments from testing and automation industry
- Doherty PAs are one of the topologies to assess these issues but as we explained as also its limits. Is Doherty the answer to future 5G/6G requirements? Variations and innovation around the DPA are flourishing thanks to the universities and industry works to push these limits.
- Meet us our booth for more discussions ☺

Sources

- The Doherty Power amplifier, Paolo Colantonio SC1 EuMIC, EuMW22
- Load Modulated RFPAs, Steve Cripps, SC1 EuMIC, EuMW22
- Linearization techniques Overview, Pere L. Gilabert, SC1 EuMIC, EuMW22
- PA Theoretical Foundation, Franco Giannini, SC1 EuMIC, EuMW22
- Doherty Power Amplifiers for Sub-6 GHz and Beyond-6 GHz: Challenges and Design Approaches, A. Piacibello, V. Camarchia, EuMC31, EuMW22
- Improving RG GaN Success, Wolfspee, Mircowave Journal ebook, March 2022
- The Doherty Power Amplifier, P. Colantonio, F. Giannini, R. Giofre, L. Piazzon, Class Chapter of University of Roma Tor Vergata, Italy
- Compact N-Way Doherty Power Combiners for mm-wave 5G Transmitter, A. K. Kumaran, H. M. Nemati, L. C. N. de Vreede, M. S. Alavi, Benelux RF conf. May 2023

www.icana-rf.com