



Cadence AWR Design Environment Empowers RF PA Design and Simulation

RF Design Solutions for High-Power Amplifiers

Dr. Chinghuei Tseng, Account Technical Director

June 2023

cadence[®]

Agenda

GaN RF Design Trends and Challenges

Cadence Solution in RF Design

Design and Simulation

RF Packaging and Thermal Analysis

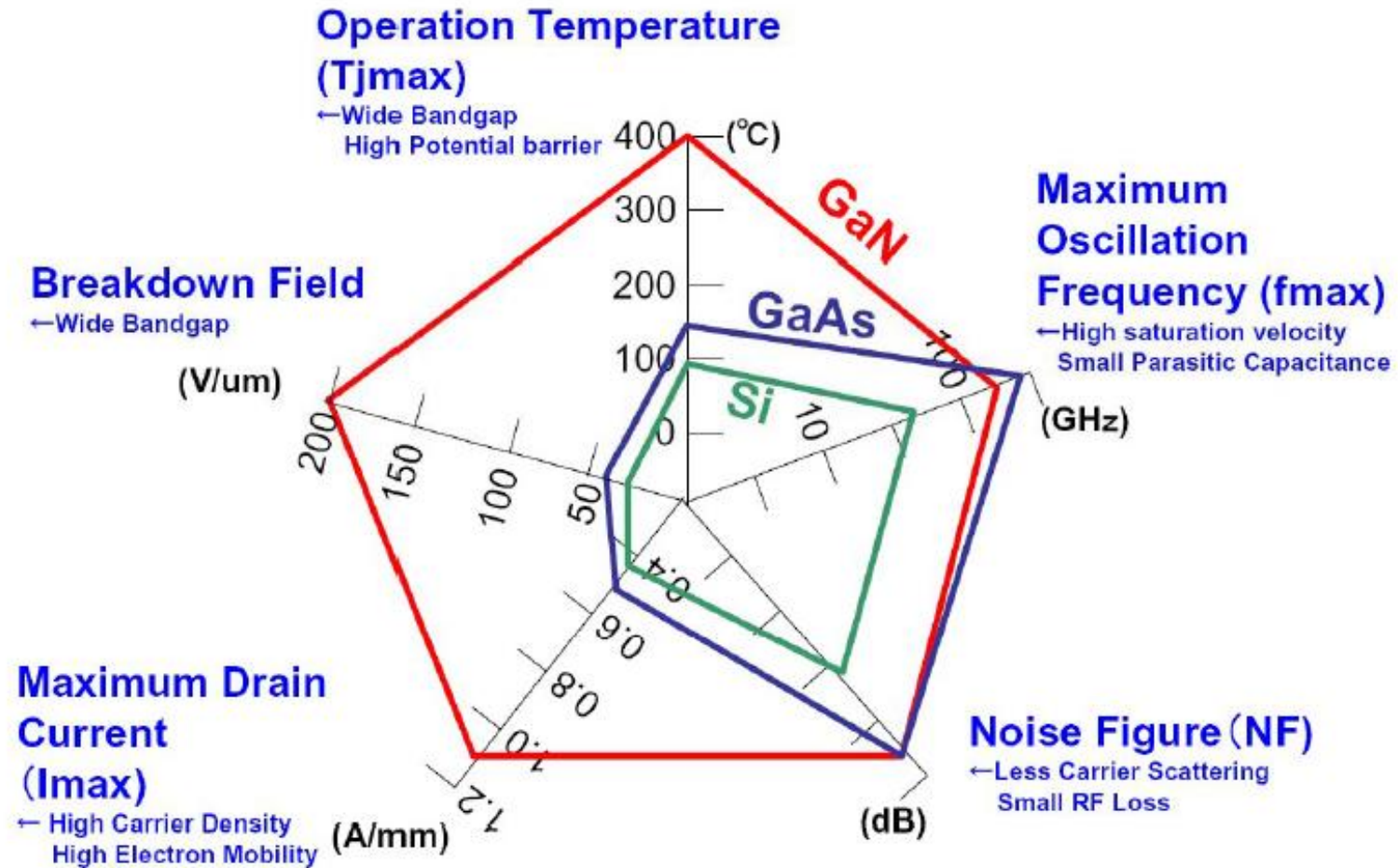
Rohde Schwarz – Cadence Collaboration

Summary



GaN RF Design Trends and Challenges

Benefits of GaN for RF Applications



Panasonic

Tanaka, Current Status of AlGaN/GaN HFETs and MMICs for RF Applications, CSICS Short Course, 2005

GaN for PA Design

Property	Si	GaAs	SiC	GaN
Energy Gap (eV)	1.11	1.43	3.2	3.4
Critical Electric Field (MV/cm)	0.6	0.5	3.0	3.5
Charge Density (# x $1 \times 10^{13}/\text{cm}^2$)	0.3	0.3	0.4	1
Thermal Conductivity (W/cm/K)	1.5	0.5	4.9	1.5
Mobility ($\text{cm}^2/\text{V}/\text{s}$)	1300	6000	600	1500
Saturation Velocity ($\times 10^7$ cm/s)	1	1.3	2	2.7



High Voltage



High Current Density



High Frequency



High Power Amp

- GaN Is Natural Fit For High Power Applications



Simulation and Design Tools Needed for an Effective Design Process


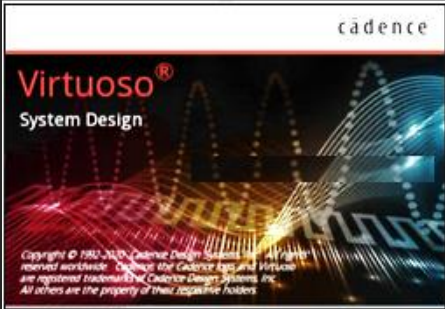
- Load pull analysis built into the design framework
 - Graphing capabilities to display load pull-based behavior in a convenient manner
- Nonlinear stability analysis tools
- Matching circuit synthesis
 - Input and Out matching circuits need to be synthesized
- Electromagnetic (EM) and circuit co-simulation



Cadence Solution in RF Design

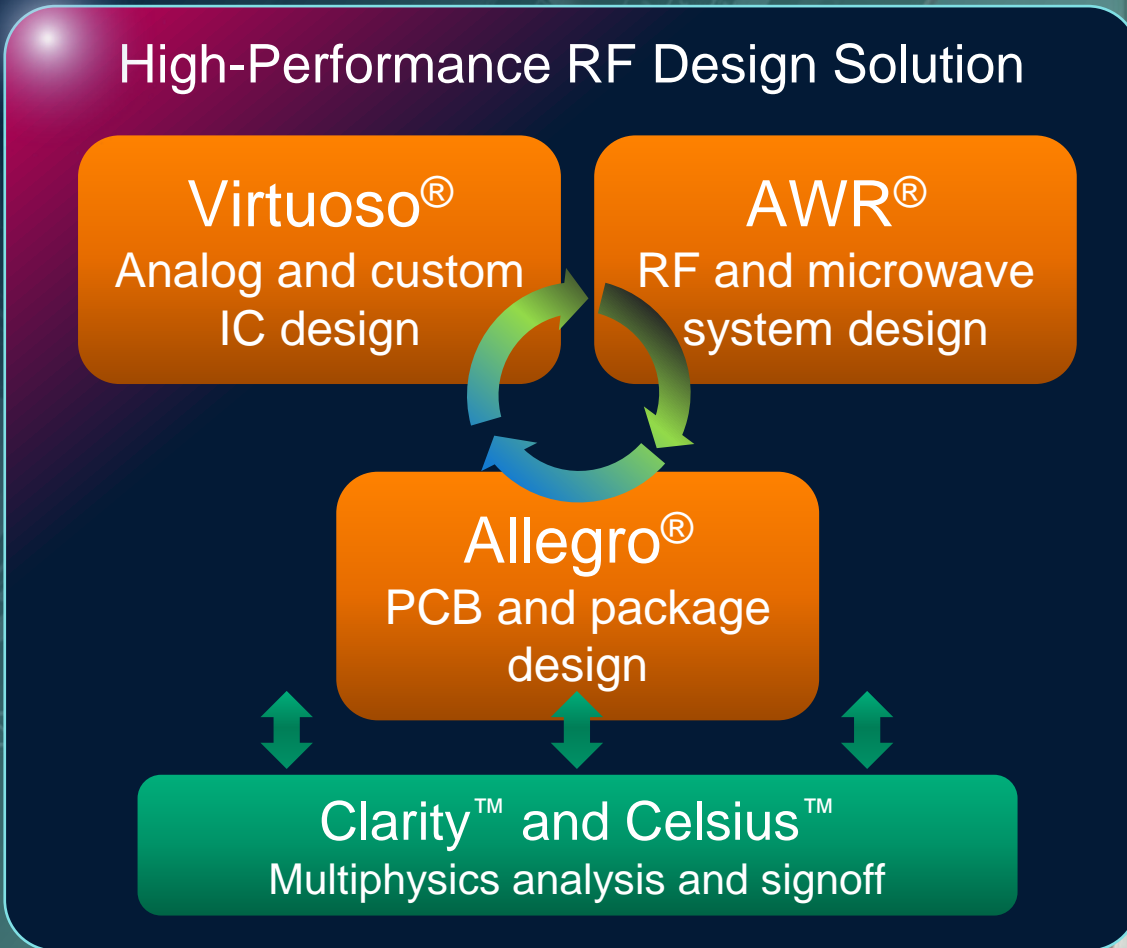
Cadence Silicon RFIC, MMIC, and SiP Solutions

Design, analyze, and implement

Platform	AWR Design Environment® 	Virtuoso® 
Technologies	<ul style="list-style-type: none"> • GaN/GaAs and Si MMIC Chips, Acoustic modules • Smaller mmW and uW Si RFIC Blocks 	<ul style="list-style-type: none"> • Si RFIC and Digital Chips • SiP and Heterogeneous Integration
Design	<ul style="list-style-type: none"> • Microwave Office® w/ APLAC • Visual System Simulator™ 	<ul style="list-style-type: none"> • Virtuoso w/ Spectre®
Analysis	<ul style="list-style-type: none"> • EMX®, AXIEM® (planar EM) • Clarity™, Analyst (3D FEM) • Celsius™ (Thermal) 	<ul style="list-style-type: none"> • EMX, AXIEM (planar EM) • Clarity, Analyst (3D FEM) • Celsius (Thermal) • Innovus™
Implementation	<ul style="list-style-type: none"> • Front-to-back for MMIC • Interoperability to Virtuoso for backend 	<ul style="list-style-type: none"> • Front-to-back for RFIC, SoC, SiP

Complete System-Level RF-Aware Design Platform

Efficient, reliable, extensible RF design and analysis from transistors to antennas



Wireless and Radar Design

- **Optimized IC, package, and PCB workflows**
- **Integrated design data exchange**
- **Seamlessly embedded multiphysics analysis**

Only with Cadence

- **Up to 5X designer productivity**
- **Eliminate point tool interoperability friction**
- **Quick turnaround system analysis**

Design, Analysis, and Implementation Solutions

RFIC

Design and Implementation

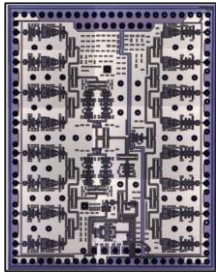
- Virtuoso®

Analysis

- Spectre®
- EMX®

Verification

- Pegasus™



III-V MMICs and Acoustics

Design and Implementation

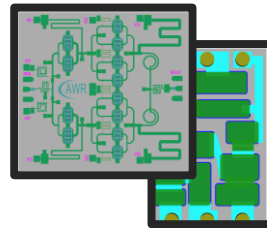
- Microwave Office®

Analysis

- APLAC®
- AXIEM®
- Clarity/ Celsius

Verification

- Microwave Office



Silicon MMICs

Design and Implementation

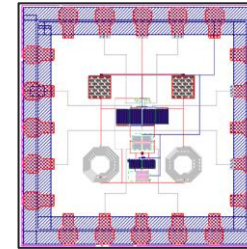
- Microwave Office

Analysis

- APLAC/Spectre
- EMX

Verification

- Pegasus



Wireless PAs

Design and Implementation

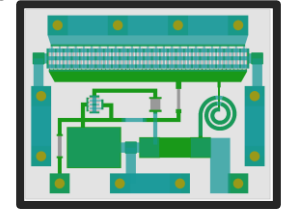
- Microwave Office

Analysis

- APLAC
- AXIEM/EMX

Implementation and Verification

- Pegasus



Packaged RFICs

Design and Implementation

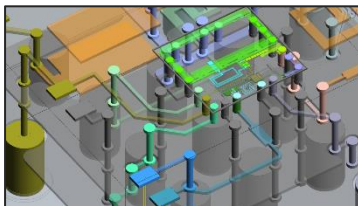
- Virtuoso RF
- Allegro® Package Designer Plus

Analysis

- Spectre
- EMX
- Clarity
- Celsius

Verification

- Virtuoso/Allegro Package Designer Plus



Packaged MMICs

Design and Implementation

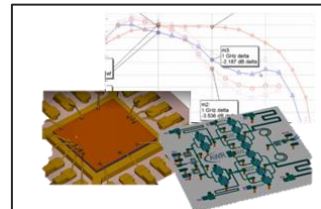
- Microwave Office
- Allegro Package Designer Plus

Analysis

- APLAC
- AXIEM
- Clarity/ Celsius

Verification

- Microwave Office/Allegro Package Designer Plus



RF Modules

Design and Implementation

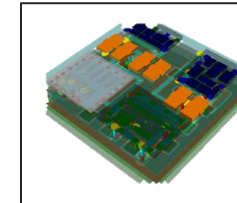
- Virtuoso RF
- Microwave Office
- Allegro Package Designer Plus

Analysis

- Spectre/APLAC
- Clarity/Celsius
- AXIEM/EMX

Verification

- Virtuoso/Allegro Package Designer Plus



RF Boards

Design and Implementation

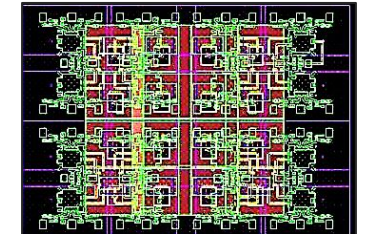
- Microwave Office
- Allegro

Analysis

- APLAC
- AXIEM
- Clarity
- Celsius

Verification

- Allegro



GaN PDK Partnerships

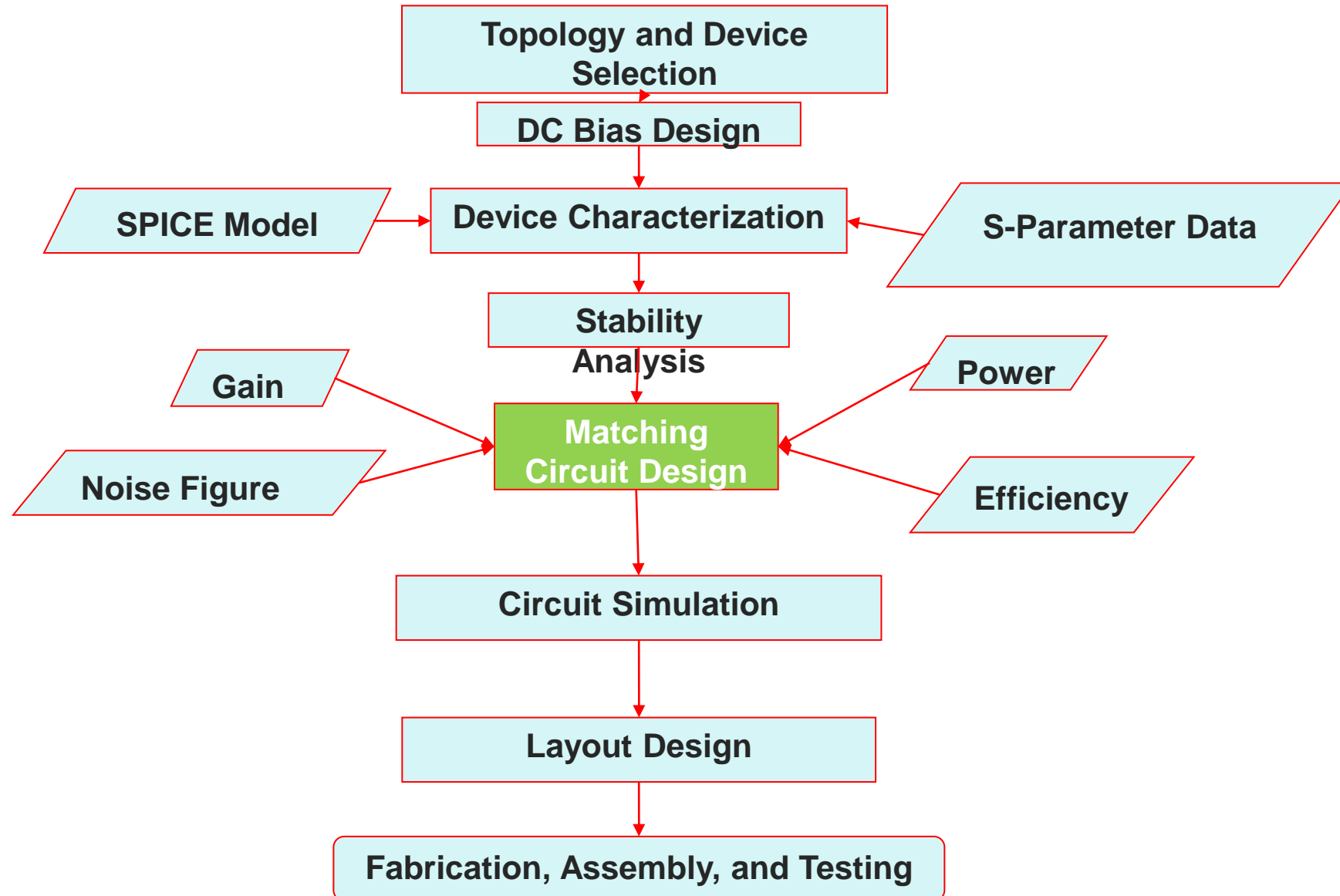
Global support of GaN foundries and integrated device manufacturers

- PDKs available from leading GaN, GaAs, SiGe, and silicon foundries
- Co-developed with foundries serving both commercial and aerospace/defense markets
- Global reach across North America, EMEA, and AP regions
- Feature-rich PDKs include:
 - Symbols and schematics
 - Fully-scalable Pcells
 - Scalable models nonlinear GaN transistor (HEMT, pHEMT) models for amplification and switching
 - Monte Carlo statistical/mismatch simulation
 - Advanced layout utilities
 - Accurate EM simulation featuring:
 - EM-enabled parameterized on-chip passives
 - Predefined substrate definitions and stack-ups with geometry simplification
 - Preconfigured simulation settings



Design and Simulation

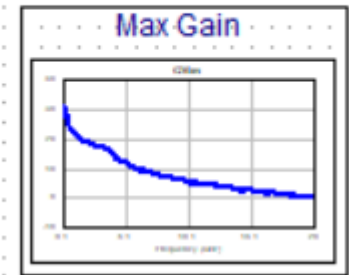
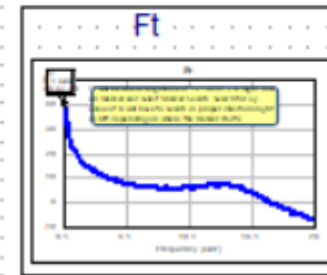
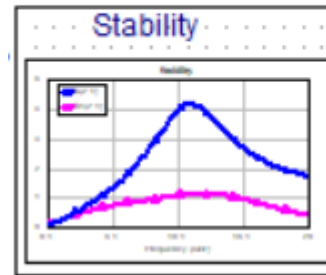
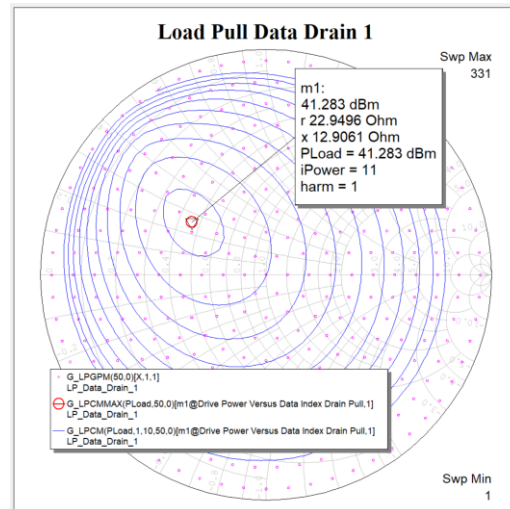
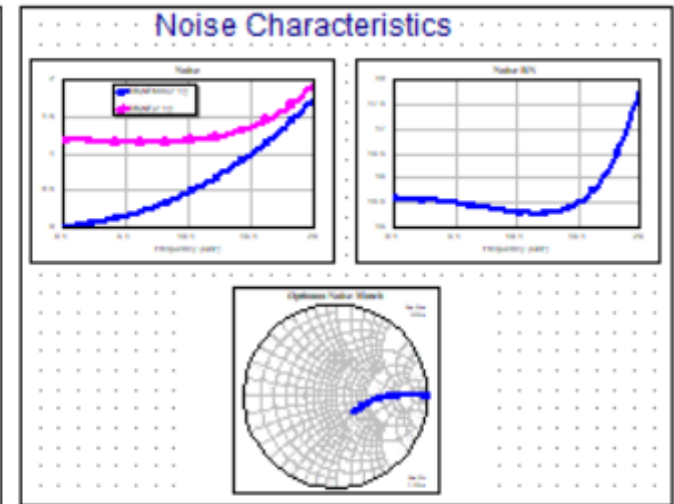
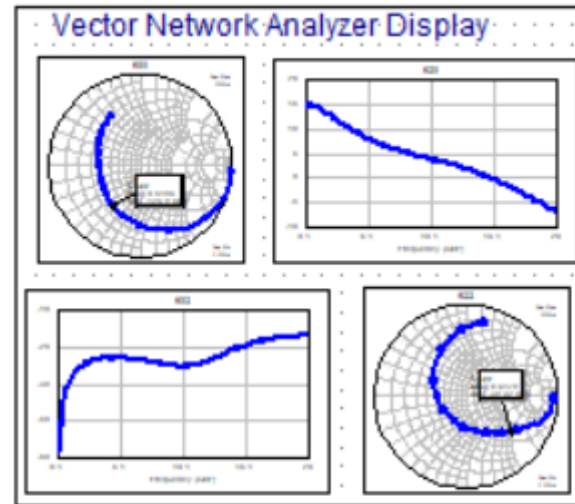
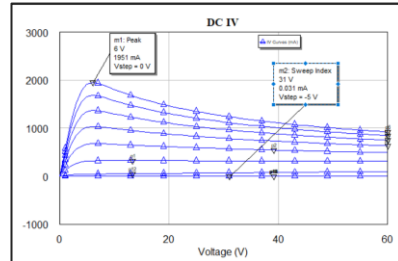
RF Power Amplifier Design Flow



Simulation and Modeling Capabilities

Analysis for all phases of RF circuit design and verification

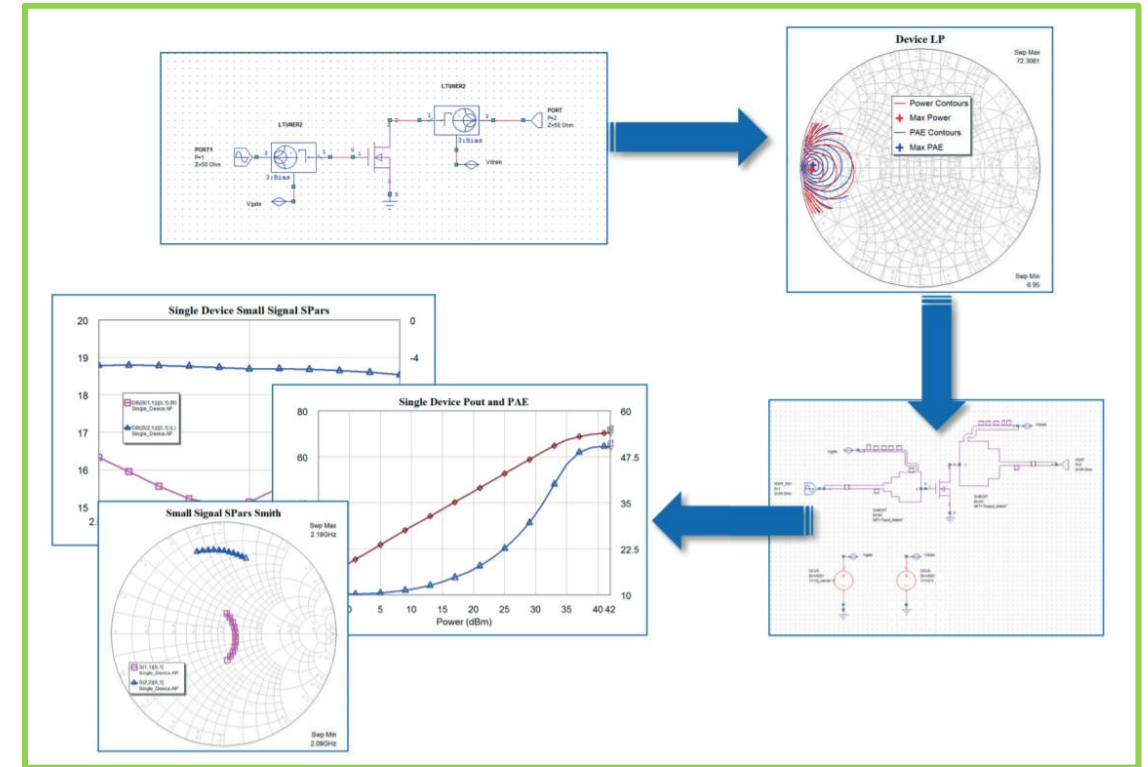
- DC IV
- Linear S-parameters
- Stability
- Harmonic balance
- Circuit envelope
- Load/source pull
- Yield
- Optimization
- EM analysis



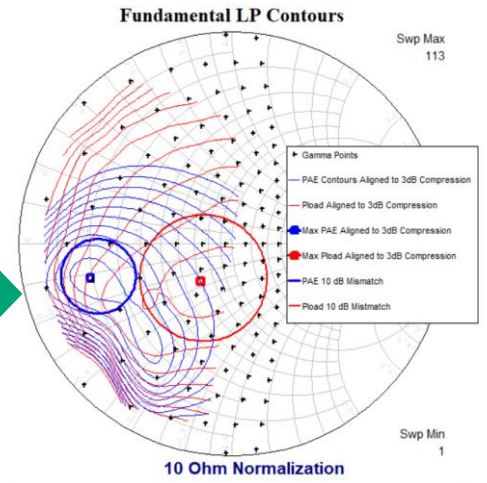
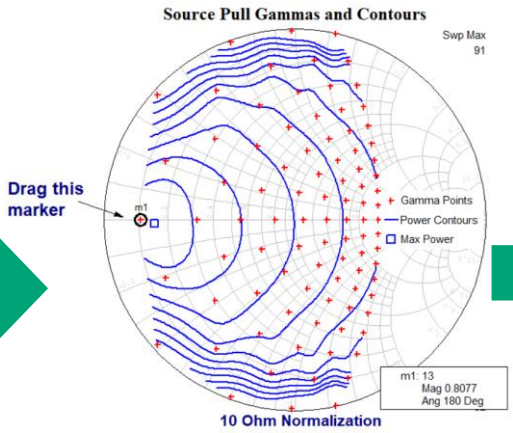
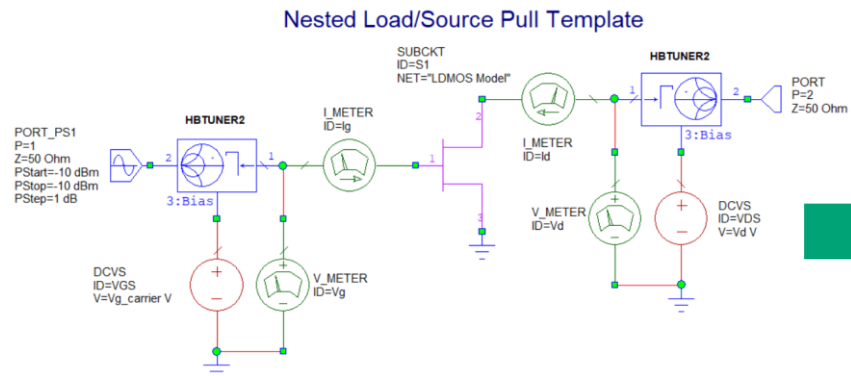
Load-Pull Analysis for Power Amplifier Design

Determine load requirements for challenging specifications

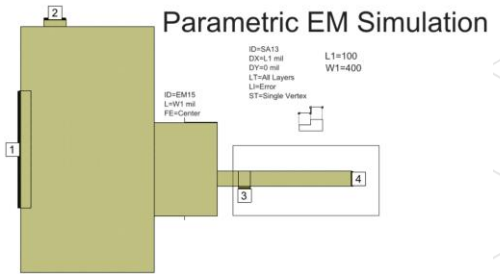
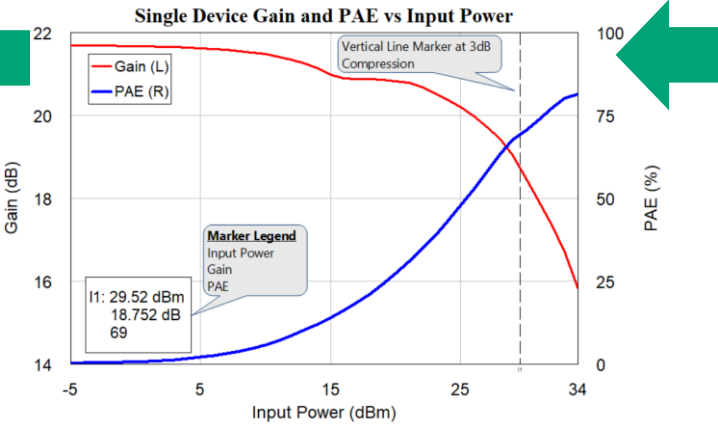
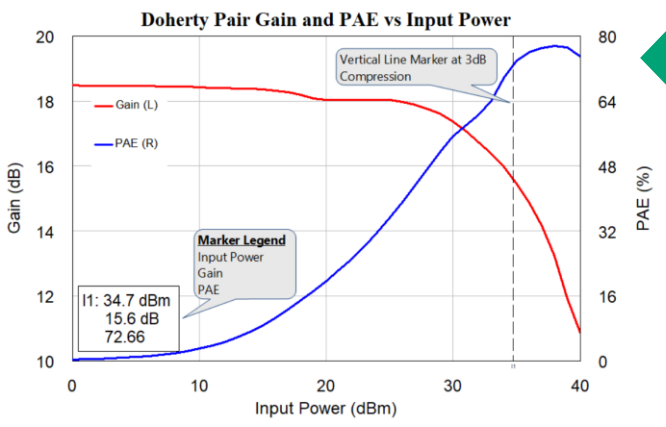
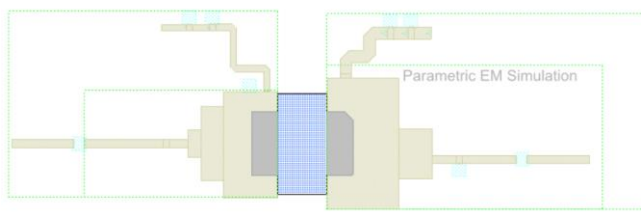
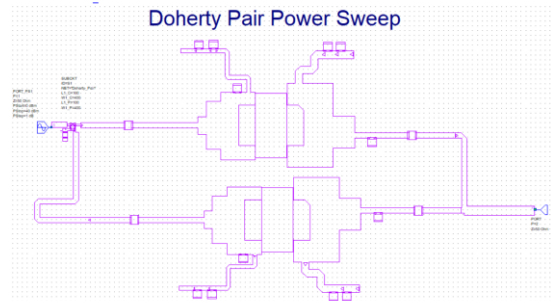
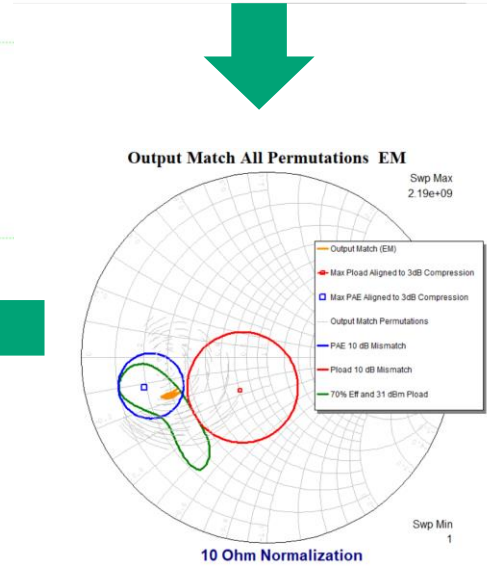
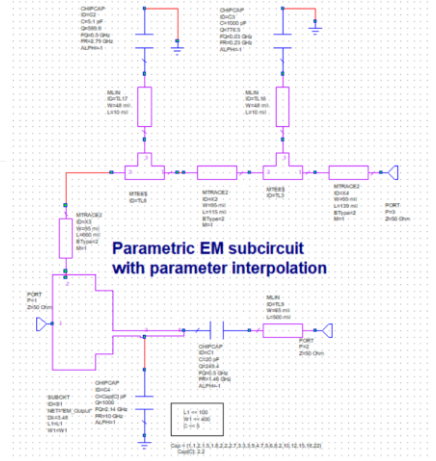
- Simulate nonlinear performance as a function of source and/or load impedance.
- Plot performance contours such as P_{out} , PAE
 - Provides key design information for matching circuit development
 - Supports nested source/load harmonic load-pull
 - Supports low-frequency (F2-F1) load-pull for two-tone excitations (new in v15)
- Can be performed over swept power, frequency, or other user-defined parameters



Load-Pull Analysis for PA

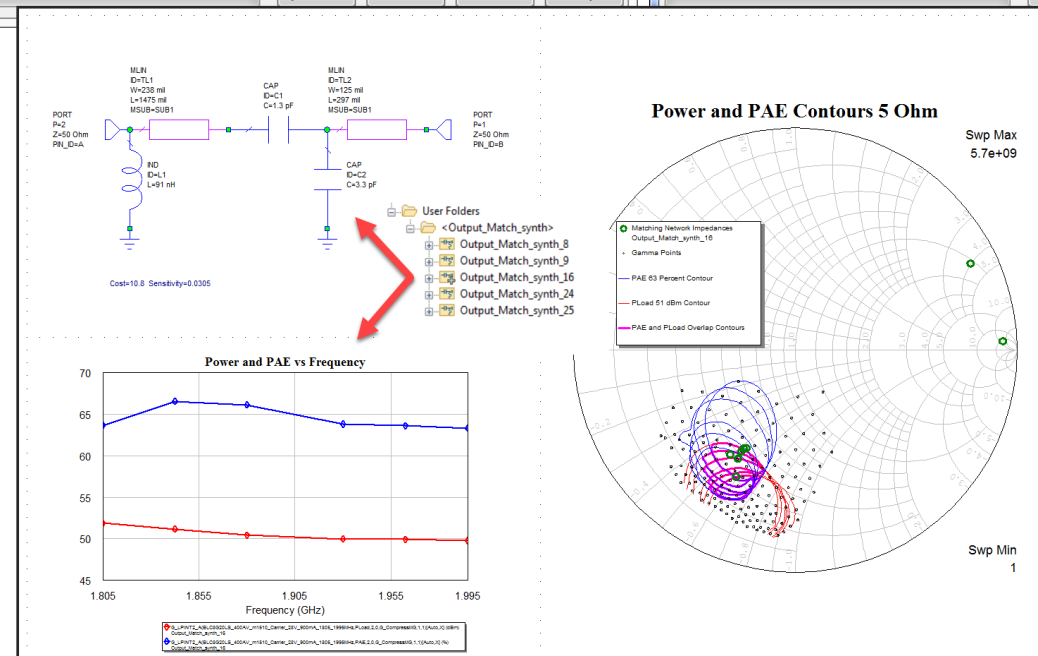
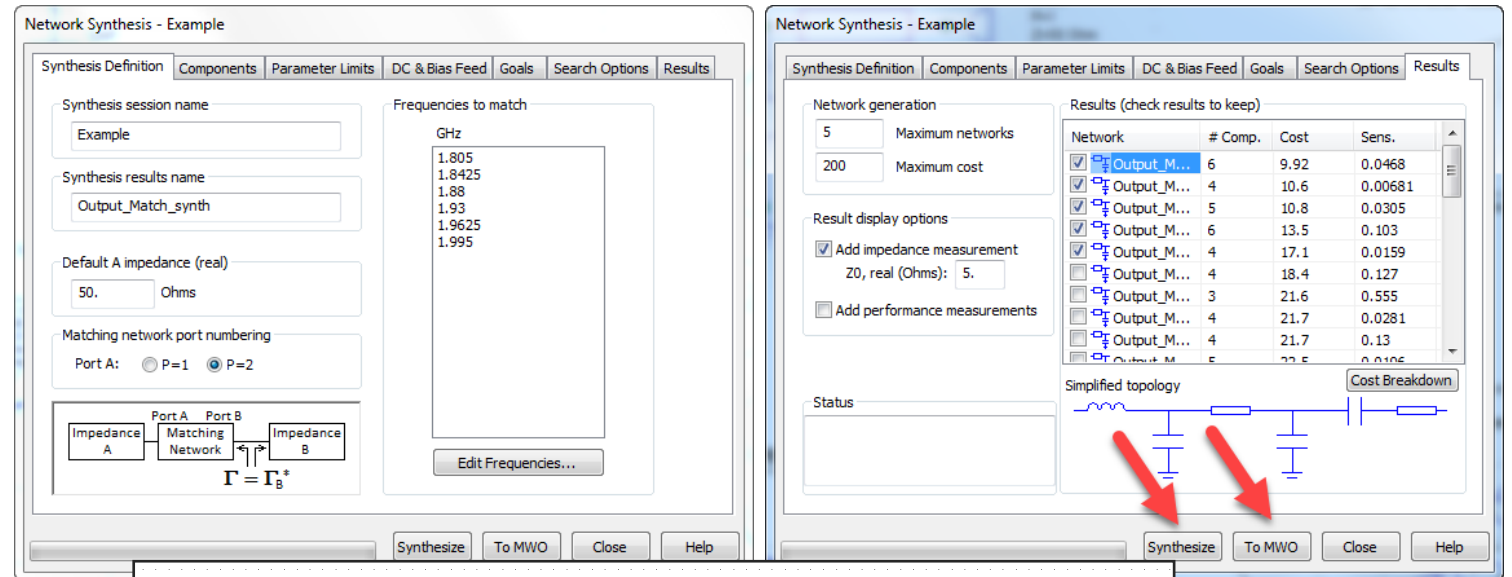


OR
Network Synthesizer Wizard



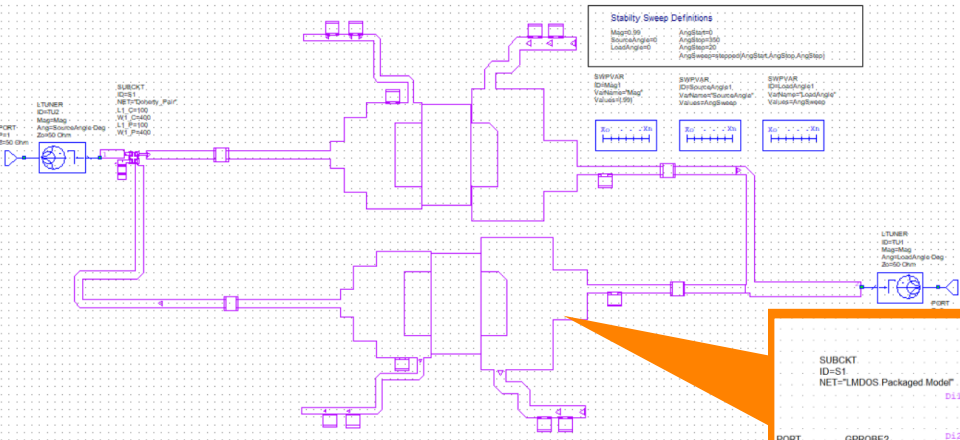
Network Synthesis Wizard

- **Synthesis Definition** - defines the "direction" of the matching network and frequency band(s) of interest
- **Components** - defines the available series and shunt components as well as first component and last component limitations
- **Parameter Limits** - defines the parameter limits, parameter rounding, component series, etc. for each component
- **DC and Bias Feed** - defines the matching network DC path constraints and the bias injection network that the wizard should consider
- **Goals** - defines the measurements and goals for the synthesis. Double-click on a Measurement or Goal to see the setup.
- **Search Options** - defines advanced search options
- **Results** - Shows Synthesis run results and controls how many networks and what additional data is sent back to Microwave Office® software



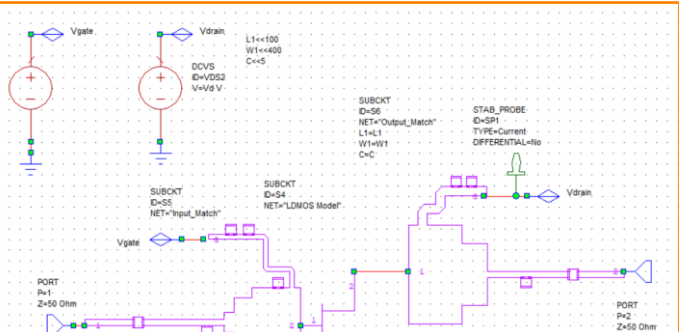
Linear and Nonlinear Stability Analysis

Linear Internal Stability Analysis



```

NLSTABILITY
ID=ST1
Fstart=1000 MHz
Fend=10000 MHz
Fsteps=10
SwpType=LINEAR
    
```



Stability Analysis Wizard: Select Circuit Schematic

This wizard guides you through the steps that are needed in analyzing the stability of the selected circuit using the STAN stability analysis. The STAN approach enables nonlinear stability analysis so the circuit stability can be studied for example as a function of swept power. Each sweep point performs an HB analysis which is followed by a set of small signal analysis over the chosen frequency band. The data gathered from each stability probe will be sent to STAN which returns the identified poles and zeros shown in MWO graphs. TVCAD with STAN and Scripting plugins is needed to analyze the data.

[Read more](#)

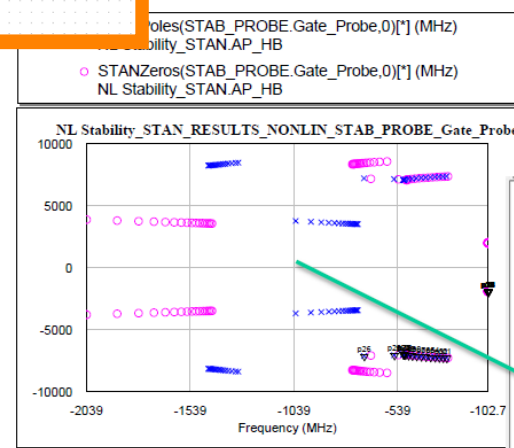
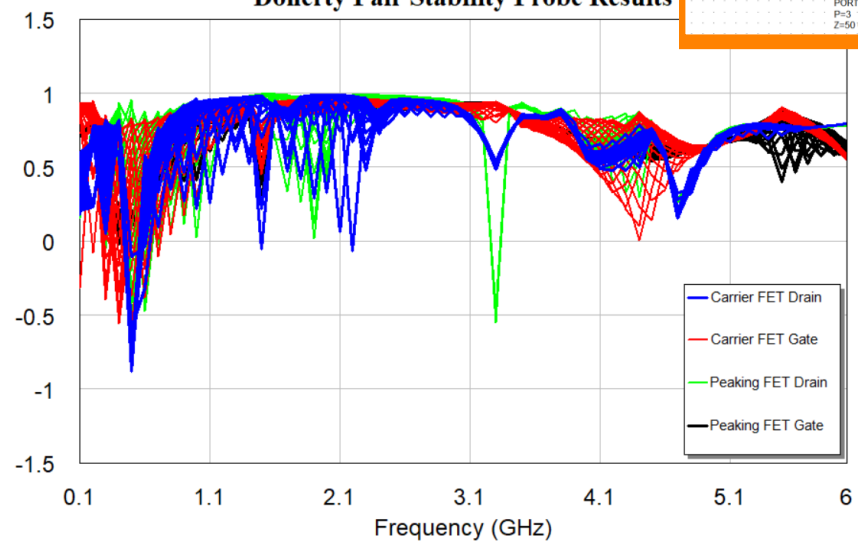
Circuit schematic

Select the circuit schematic for Stability Analysis:

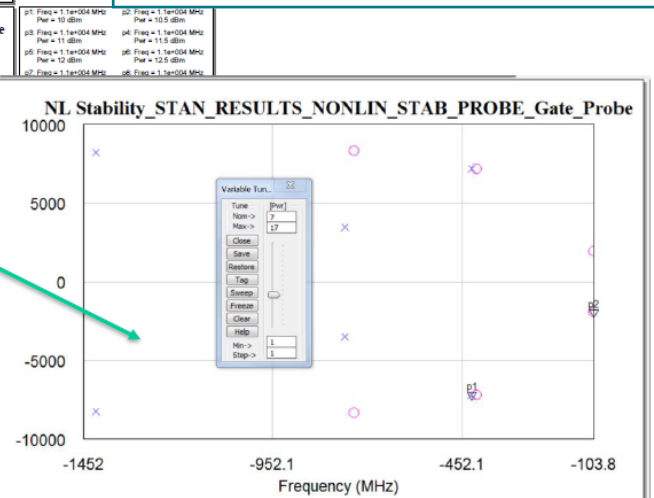
*** NO VALID SCHEMATICS FOUND ***
This wizard requires at least one unlocked Circuit Schematic with enabled port(s) and enabled named connector(s) or STAB_PROBE element(s).

Next Cancel

Doherty Pair Stability Probe Results

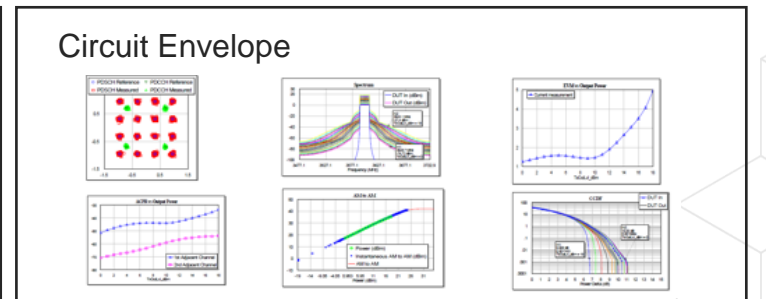
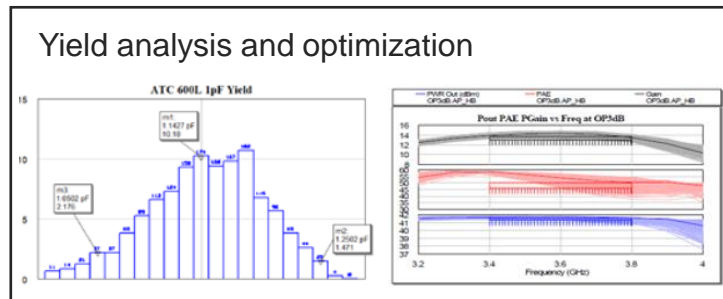
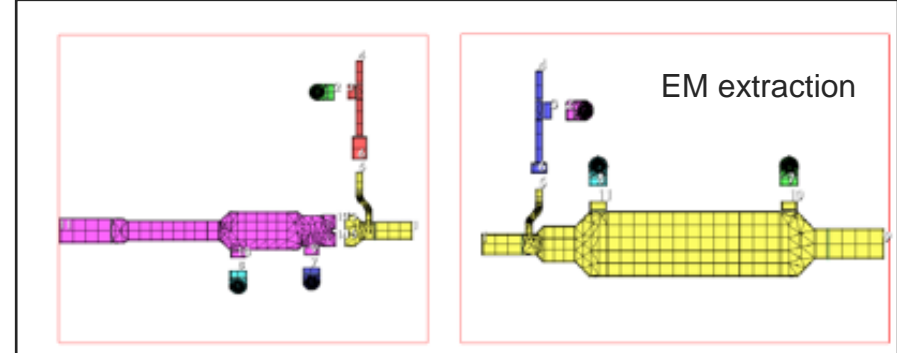
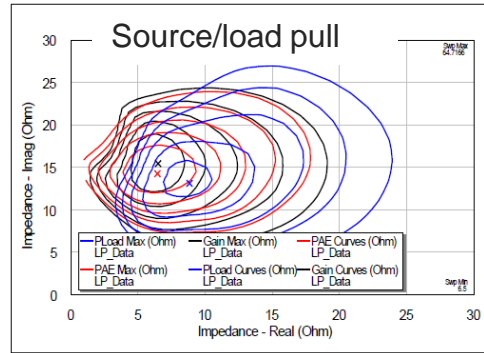
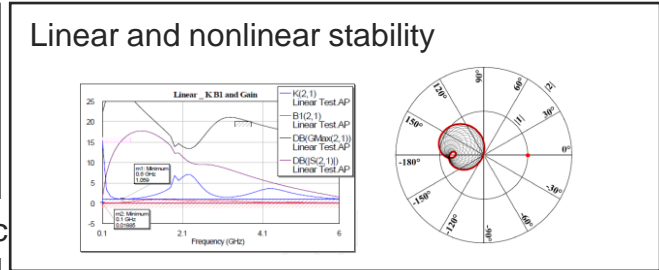
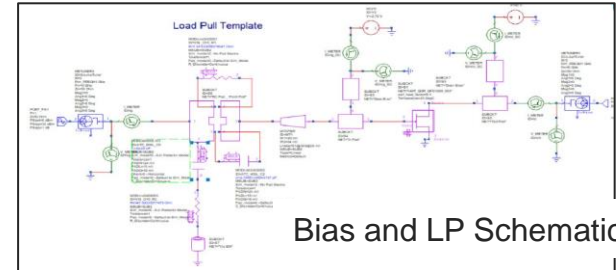


- MMIC Power Gain
- NL Stability_STAN_RESULTS_NONLIN_S3_S1_STAB_PROBE_Drain_Probe
- NL Stability_STAN_RESULTS_NONLIN_S3_S2_STAB_PROBE_Drain_Probe
- NL Stability_STAN_RESULTS_NONLIN_S3_S3_STAB_PROBE_Drain_Probe
- NL Stability_STAN_RESULTS_NONLIN_S3_S4_STAB_PROBE_Drain_Probe
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- NL Stability_STAN_RESULTS_NONLIN_S3_S7_STAB_PROBE_Drain_Probe
- NL Stability_STAN_RESULTS_NONLIN_S3_S8_STAB_PROBE_Drain_Probe
- NL Stability_STAN_RESULTS_NONLIN_STAB_PROBE_Gate_Probe



Front-to-Back RF GaN PA design

- Determine the biasing requirement
- Linear stability analysis and stabilization network (if needed)
- Impedance matching (source/load pull) and nonlinear optimization
- Physical design and EM extraction
- Optimization
- Yield Analysis
- Digital Modulation Analysis – EVM, ACPR, CCDF, Spectrum, IQ results

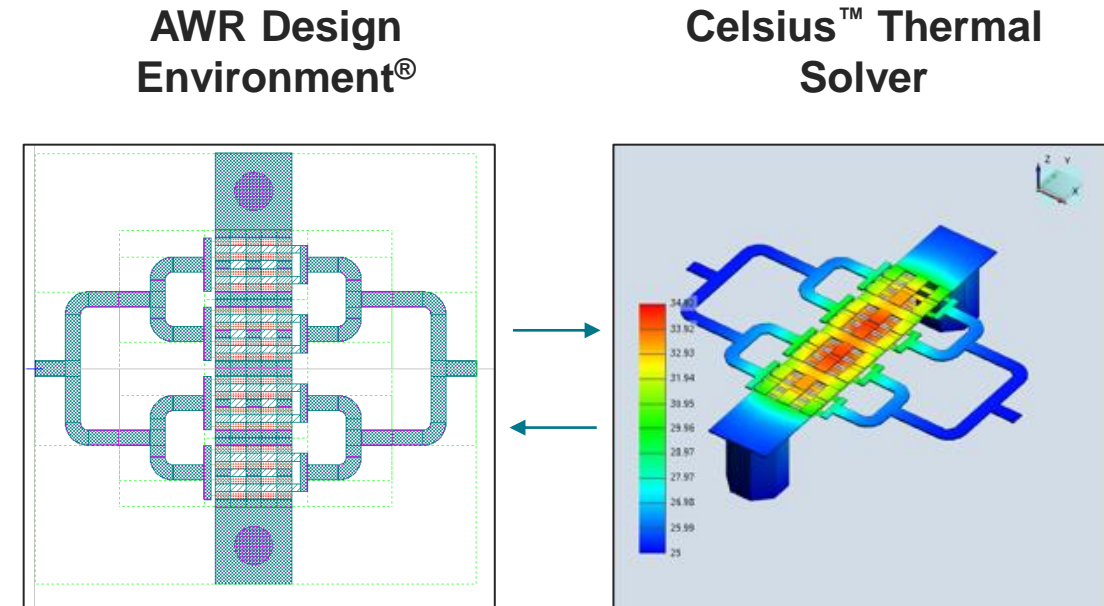




RF Packaging and Electrothermal Analysis

Why Celsius Thermal Solver in RF Design?

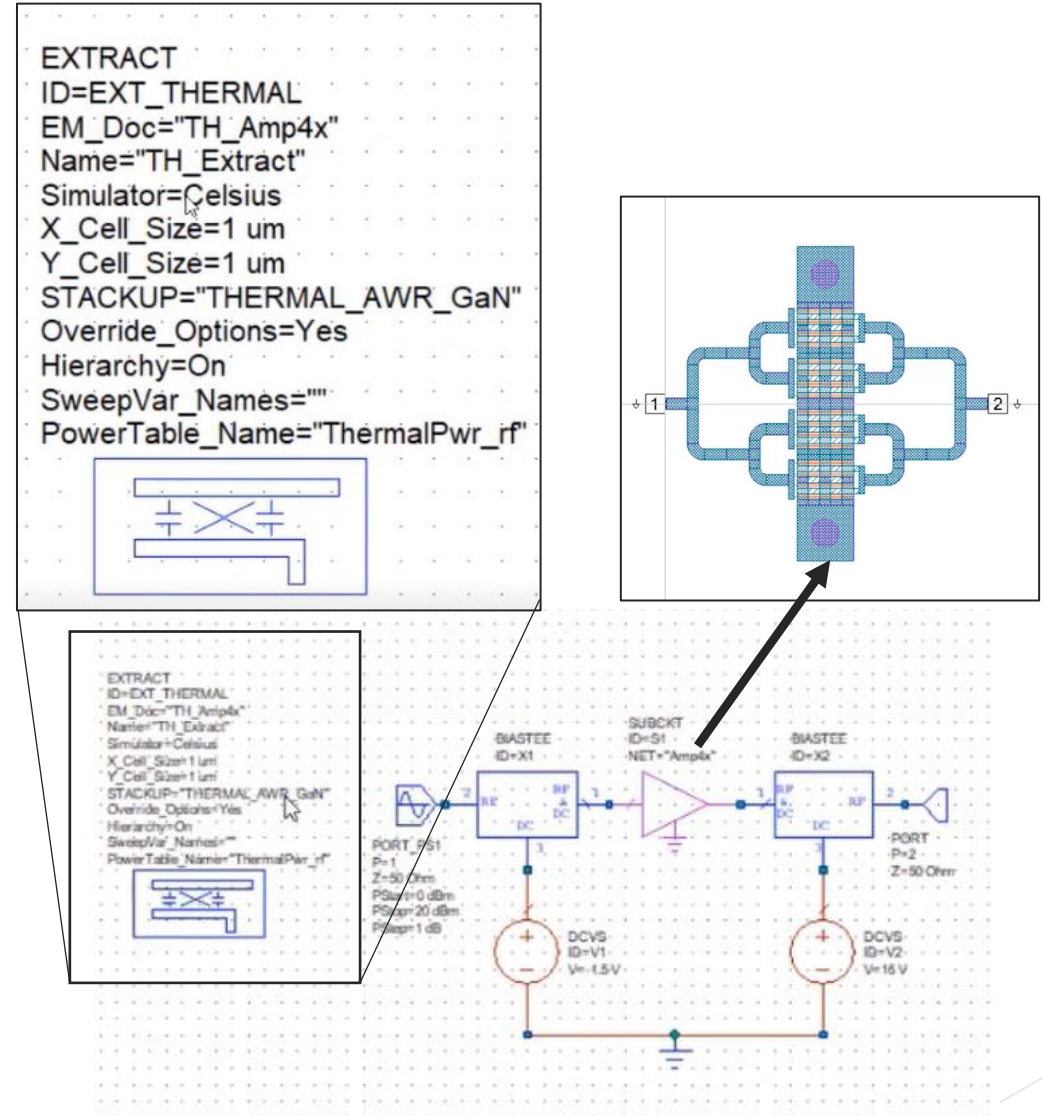
- Operating temperatures impact reliability (device lifetime) and performance
- Thermal analysis gives designers an understanding of operating temperature related to power dissipation
- Temperature information can be inserted into the electrothermal model to predict the impact on RF performance
- Heat maps can be used to help develop/optimize heatsink design
- Provide RF engineers with ready access to operating temperature data for reliability and performance studies



Celsius Thermal Solver for Thermal Analysis in Microwave Office Software

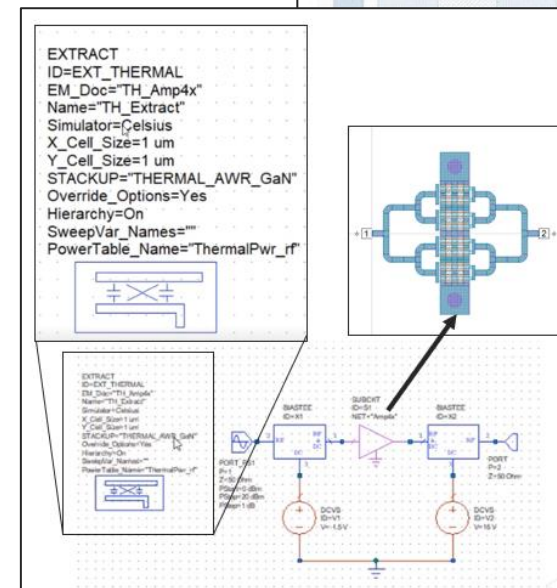
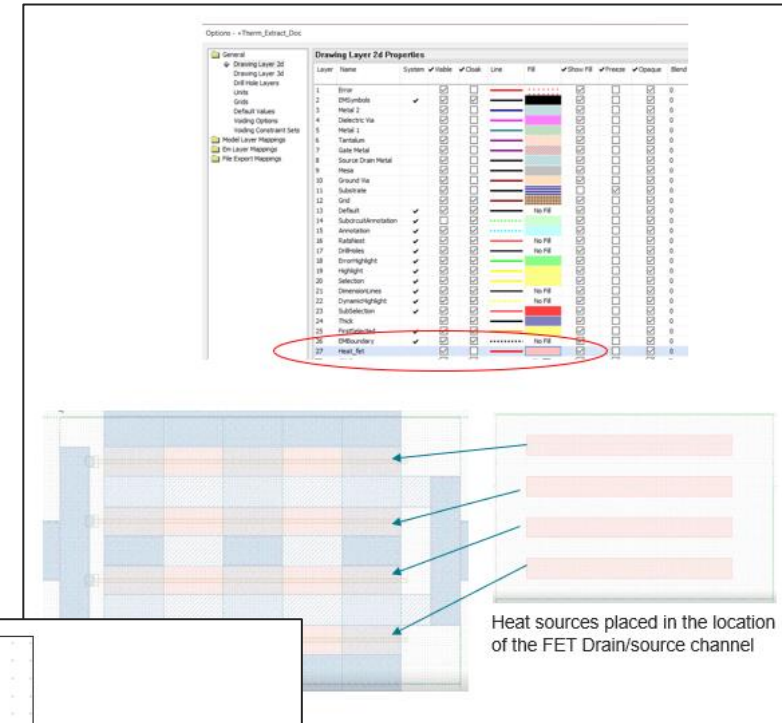
Key features and benefits

- Thermal structures are easily created using powerful Microwave Office[®] extraction block workflow
- Leverages existing structure data (geometries, materials, stack up) in Microwave Office software to define Celsius[™] Thermal Solver structure
- Obtain power dissipation information from Microwave Office analysis
- Thermal simulations launched from inside AWR[®] platform, results automatically returned
- Easy-to-use flow allows RF design engineers to perform their own thermal analysis



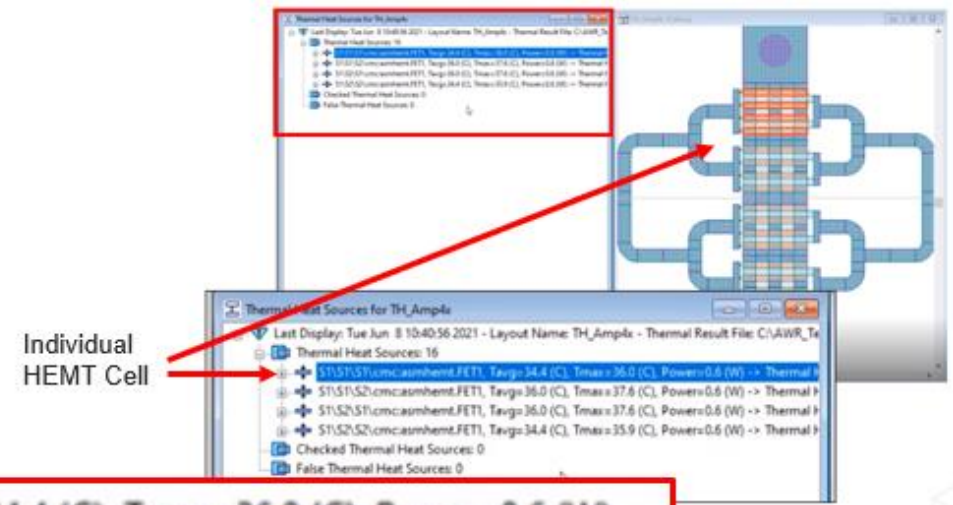
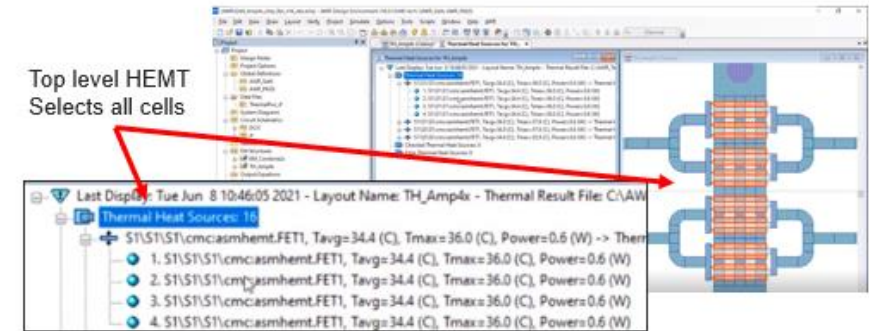
Microwave Office / Celsius Thermal Workflow

1. **Set-up** - thermal draw layers, EM layer mapping
2. Define heat source geometries in layout (or pCell)
3. **Add extraction block** to create a thermal document
4. Create **power dissipation** data file from nonlinear simulation (new measurement)
5. Associate extraction block with stackup and power dissipation data file
6. Simulate in Microwave Office[®] software or send to Celsius[™] Thermal Solver (native editor)
7. Operating temps back-annotated into Microwave Office and linked to user-defined heat sources



Thermal Analysis Results – GaN FET Example

- Test structure – GaN HEMT devices, combiner network, and source to ground vias
- Celsius™ results automatically reported listed of all defined heat sources throughout the hierarchal design layout
- Selected thermal analysis results for individual heat sources are highlighted in the layout
- Average and peak temperature across heat source area and power dissipation are reported



1. S1\S1\S1\cm:asmhemt.FET1, Tavg=34.4 (C), Tmax=36.0 (C), Power=0.6 (W)



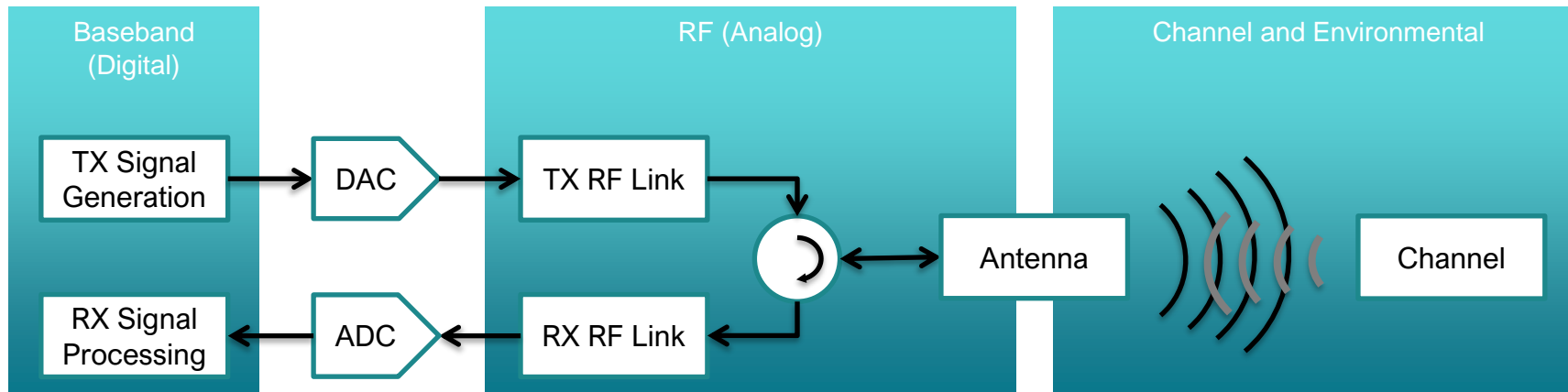
Rohde Schwarz – Cadence Collaboration

WinIQSim2 – VSS – VSE Product integration

Visual System Simulator (VSS)

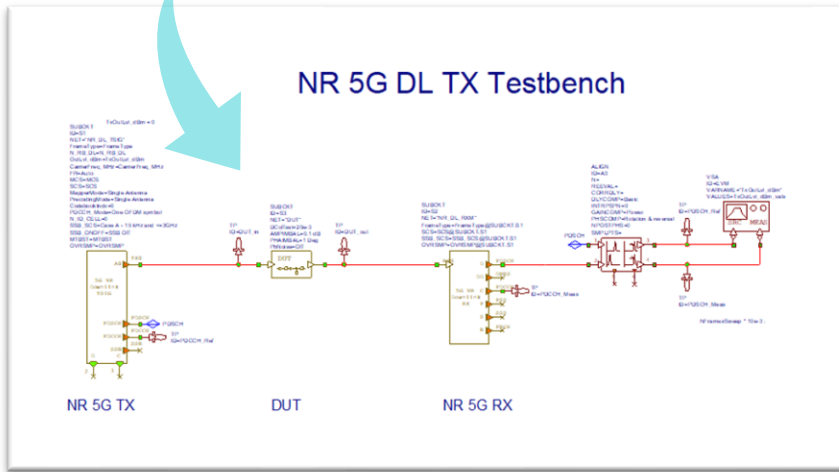
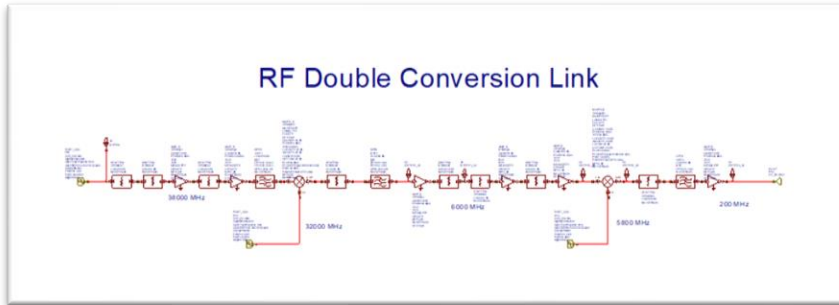
- Part of the Cadence[®] AWR Design Environment[®] platform
- Design and analyze anything from simple RF links to complete comm systems
 - RF budget analysis, RF spur heritage
 - Modeling and time-domain simulation of complete communication links
 - Phased array design, standard communication libraries, etc.

VSS includes models for every component in such systems!

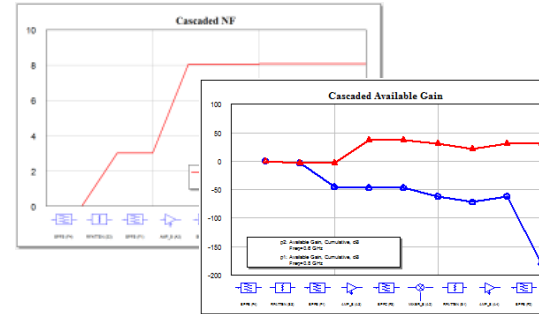


RF System Design and Analysis Flow in VSS

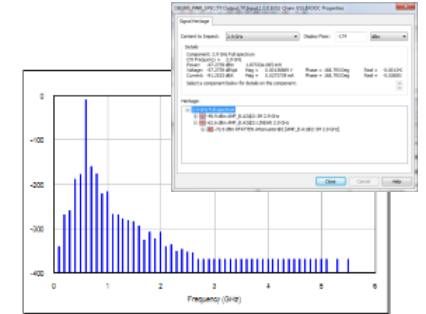
- Construct and analyze RF link



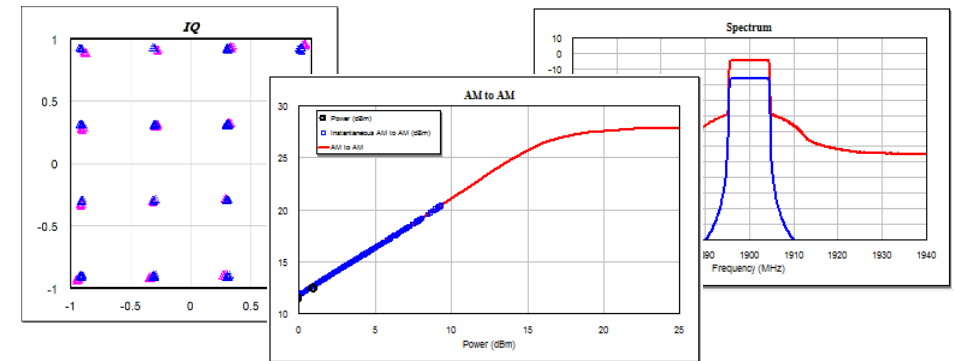
RF Budget Analysis



Spur Identification



Time Domain Simulations

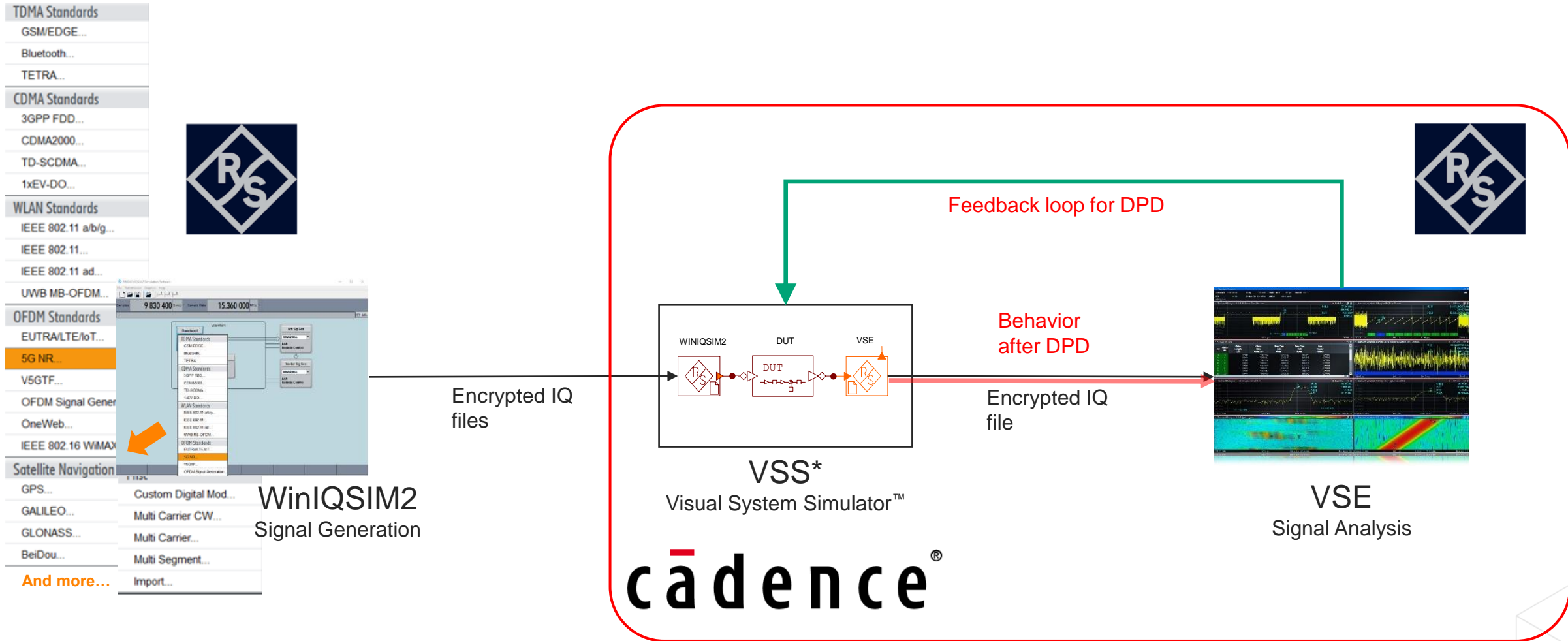


- Include in communication system/test bench

The same RF link is used by RF budget, spur analysis, and time domain simulators!



Joint solution: Rohde & Schwarz and Cadence

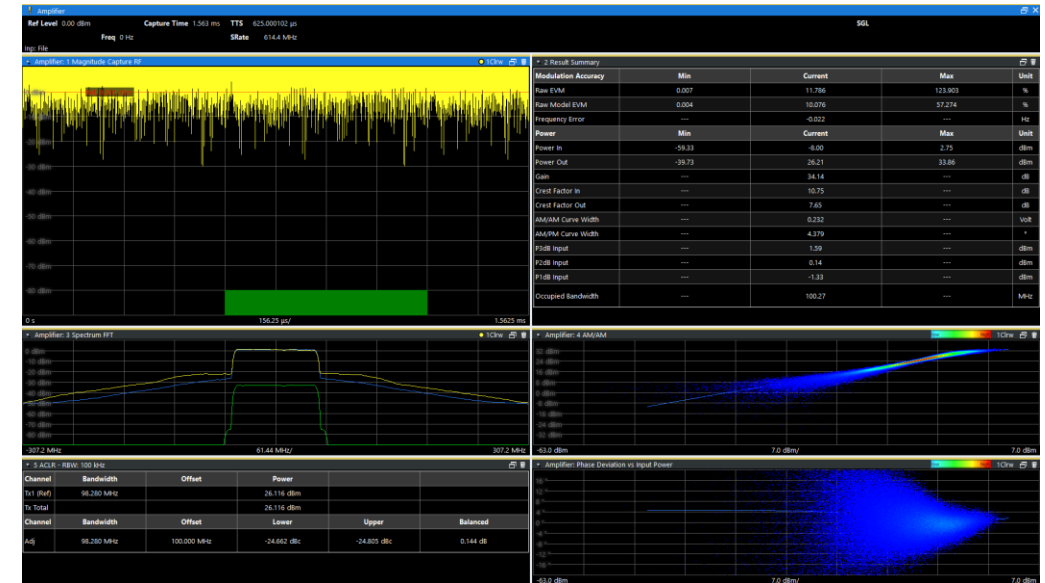
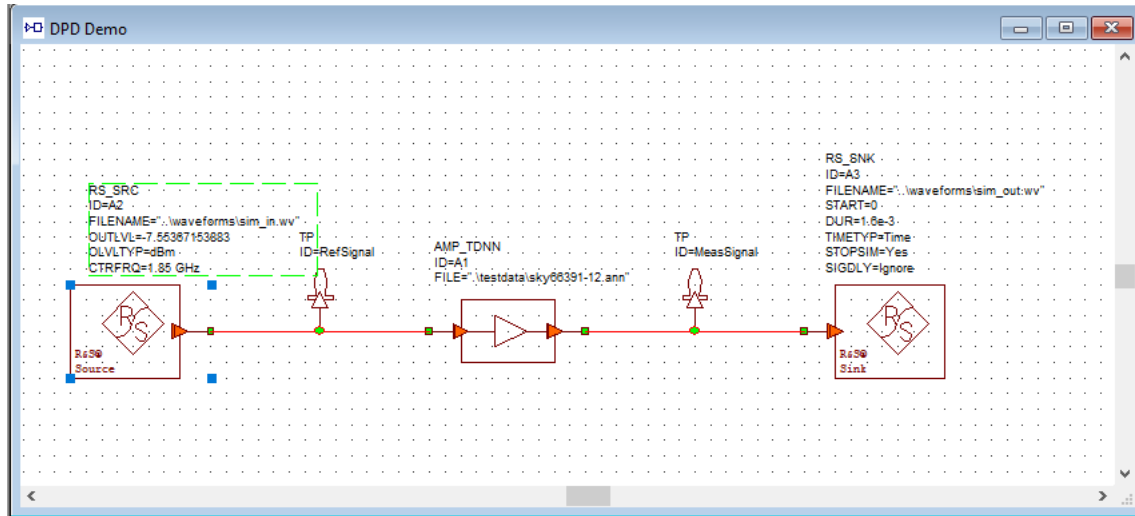


Pre-Distorting an RF Amplifier Purely in Simulation

Script controlling both software packages:
Cadence VSS and R&S VSE

RF simulation of PA in Cadence VSS

Iterative Direct DPD in R&S VSE



Summary

- With superior electrical performance, GaN HEMT power amplifiers are being widely adopted for commercial and aerospace/defense applications
- To capitalize on this performance, designers need accurate device models, robust nonlinear RF circuit simulation, and specific design tools
- For MMIC-based PAs, designers need to use PDKs authorized by the GaN foundry to ensure simulation accuracy and proper layout
- The successful design and simulation of GaN PAs is based on multiple simulation technologies including EM analysis for parasitic extraction and possibly circuit envelope for simulation-modulated performance metrics
- Packaging plays a key role in thermal dissipation, internal impedance matching, and multi-technology integration



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