PCIe 及其它高速連接器的多物理場模擬技術

日期： 2024年11月26日 (二)
發表單位：士盟科技
主講者：Job Wu 工程師

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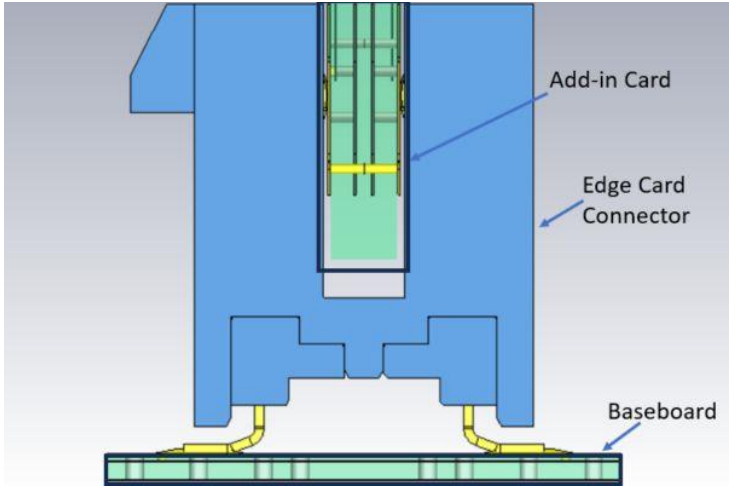
- Transitioning from PCIe Gen6 to Gen7
- MODSIM for Connectors
- System Level Simulation – Connector plus Cable
- Multiphysics Simulation for Connectors and Cables
- Measurement and Data Processing with IdEM
- Inspector – Connector Assessment Tool
  - PCIe 5.0 M.2

Simulation for PCIe Gen7

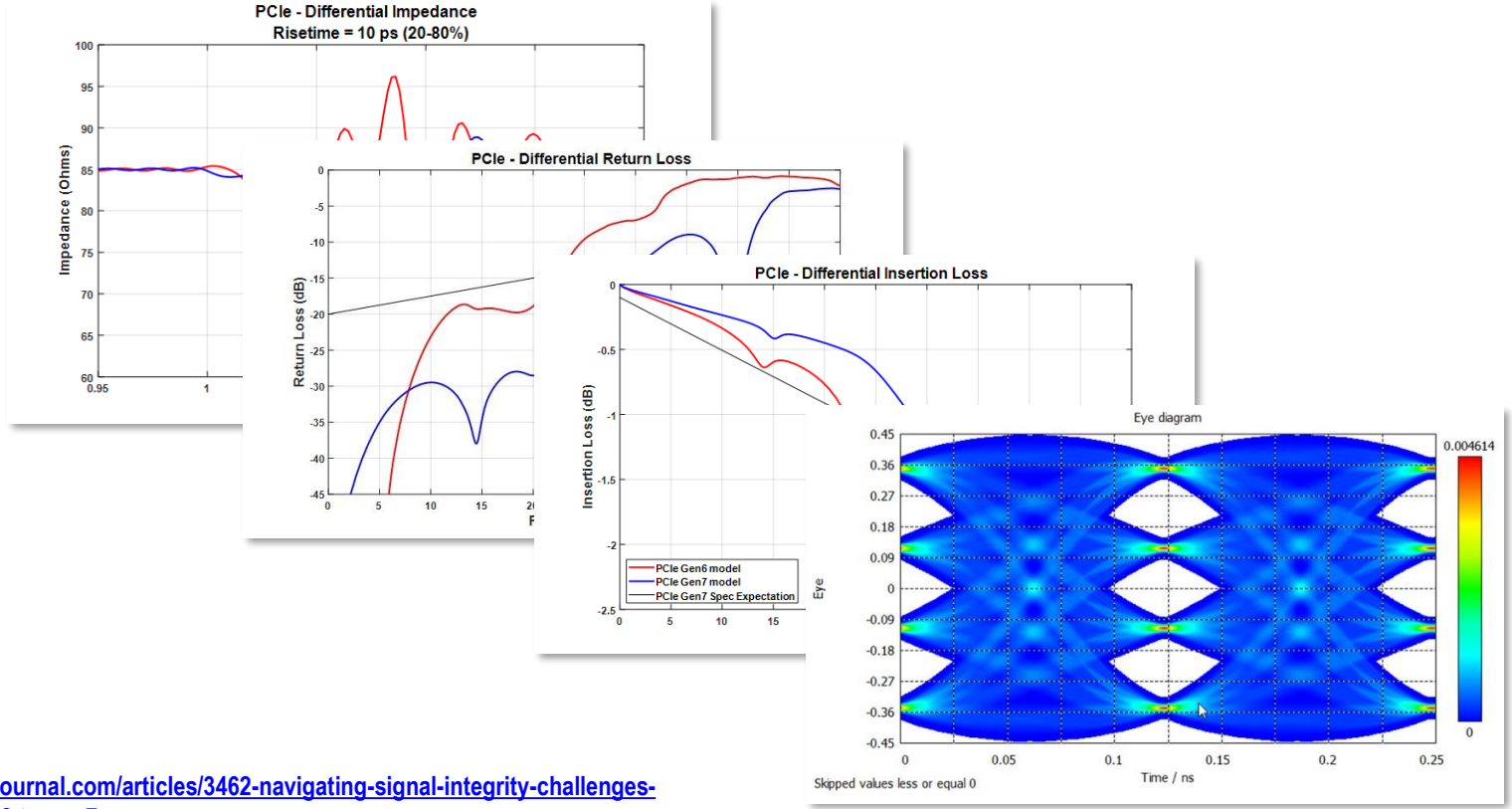
- **Example paper:** Navigating Signal Integrity Challenges: Transitioning from PCIe Gen6 to Gen7 by Amphenol FCI
  - Key Challenges for PCIe Gen7:
    - 128 GT/s data rate using PAM-4 modulation.
    - A pad-to-pad channel loss budget shift from 32 dB @ 16 GHz to 36 dB at 32 GHz.
    - Card Electromechanical (CEM) Connector must accommodate increasing frequency range whilst maintaining current form factors.



參考資料
https://www.signalintegrityjournal.com/articles/3462-navigating-signal-integrity-challenges-transitioning-from-pcie-gen6-to-gen7

PCIe Gen7 Simulation Requirements

- Impedance
- Return Loss
- Insertion Loss
- Eye Diagram



Eye diagram for reference only

參考資料

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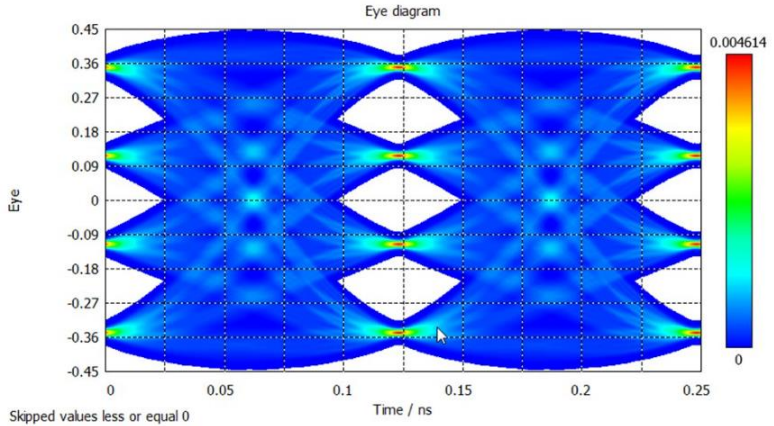
Eye-diagram in CST

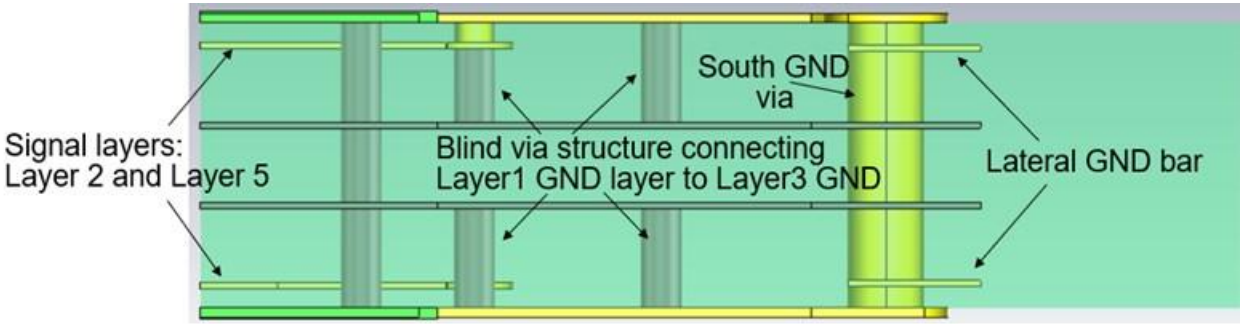
- Different types of encoding available:
  - 8b/10b: encoding of 8 bits by using 10 bits.
  - 64b/66b: encoding of 64 bits by using 66 bits.
  - 128b/130b: encoding of 128 bits by using 130 bits.
  - 128b/132b: encoding of 128 bits by using 132 bits.
  - PAM4: Pulse amplitude modulation with 4 levels.
  - PAM_N: Pulse amplitude modulation with N levels.
  - DBI8: 8-bit Data Bus Inversion



A typical PAM4 eye diagram

PCIe Gen7 Design Options: Add-In Card

- ► Solutions:
  - Reduce wipe length
  - Position of inner ground plane layers – reduce NEXT
  - Blind vias – improve IL
- ► Signal Integrity vs Mechanical Requirements
  - Reduced wipe length improves SI, but challenge for mechanical integrity
  - Multiphysics considerations



AIC design of PCIe Gen7 CEM connector

參考資料

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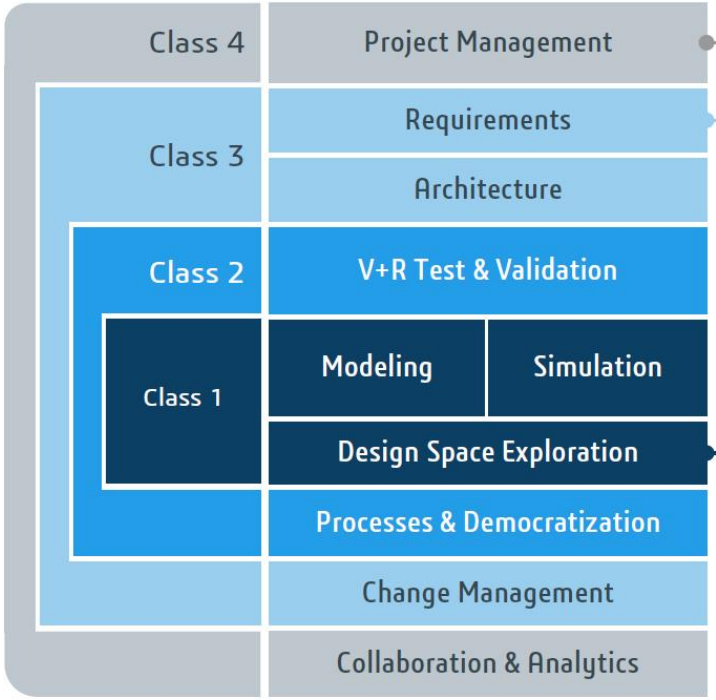
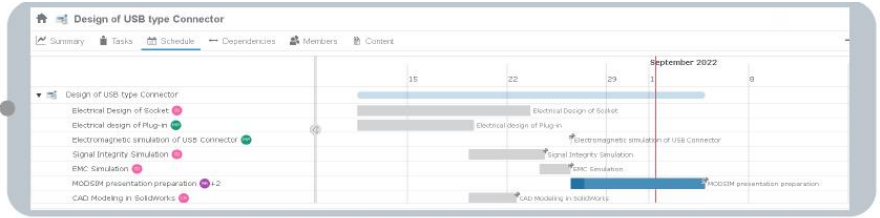
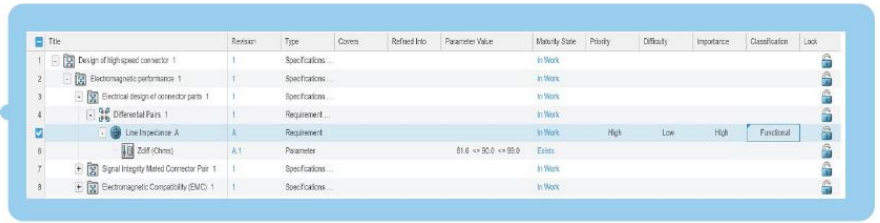
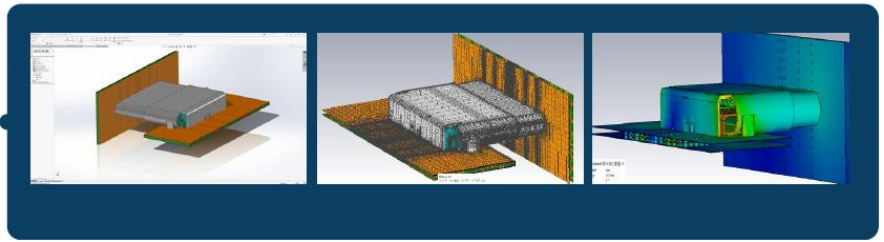
MODSIM: Modeling + Simulation









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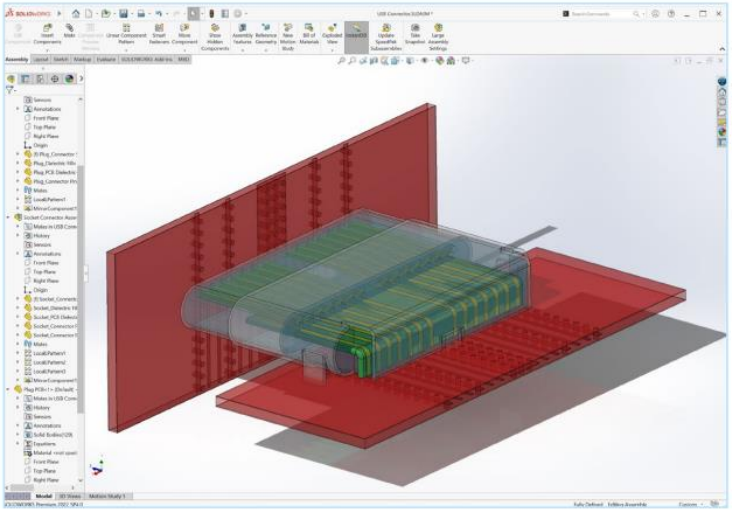
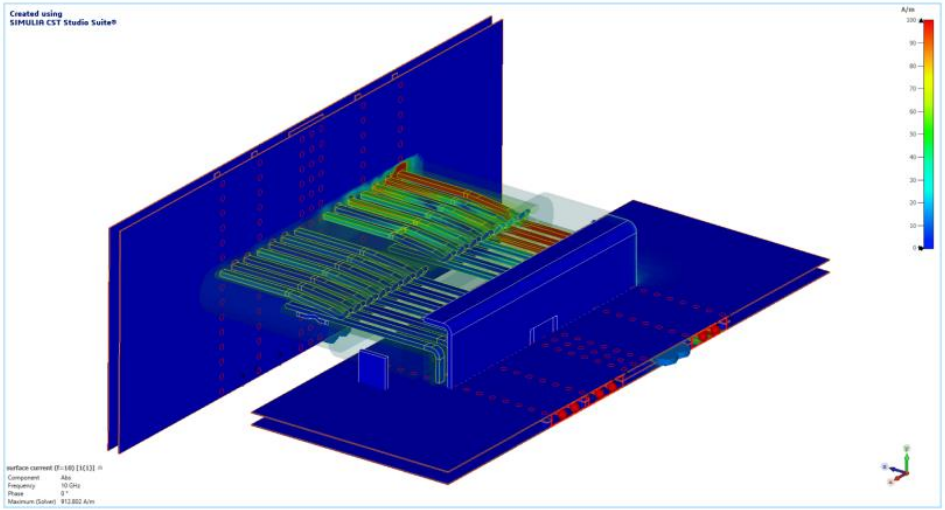
MODSIM: Modeling + Simulation



SolidWorks Parametric CAD



CST STUDIO Suite Electromagnetic Simulation

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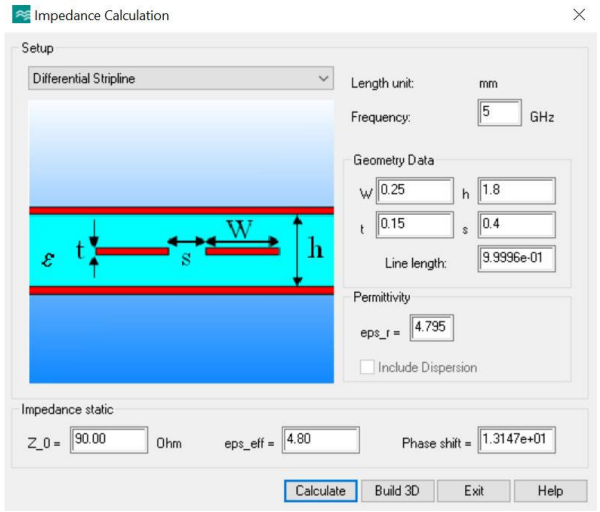
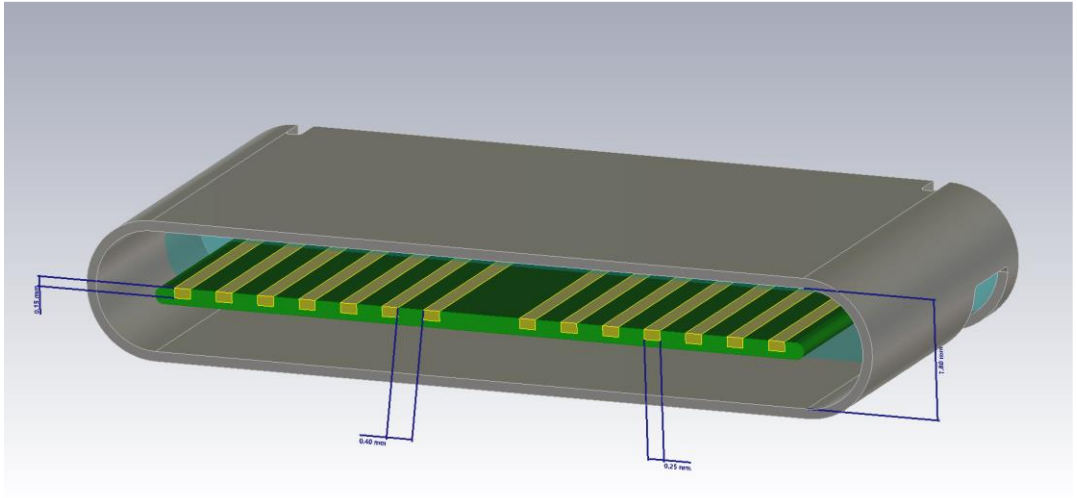
Electrical Design – Socket Line Impedance Calculation





Structural considerations – stiffness of board, pin seating and retention

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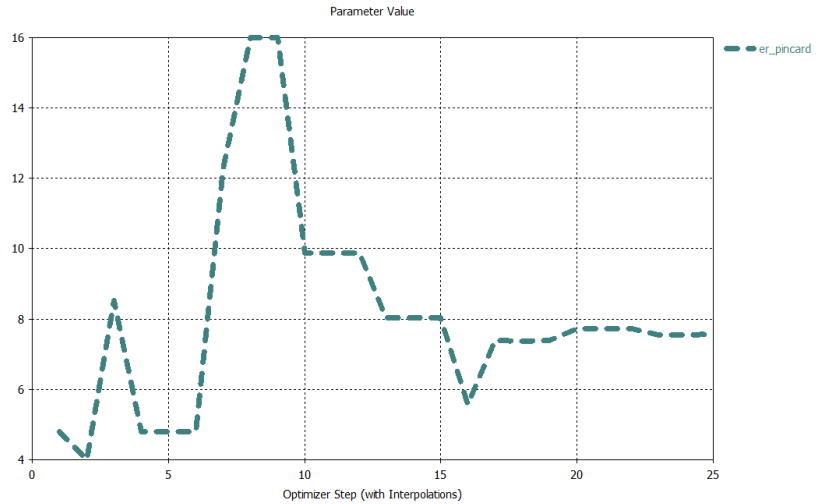
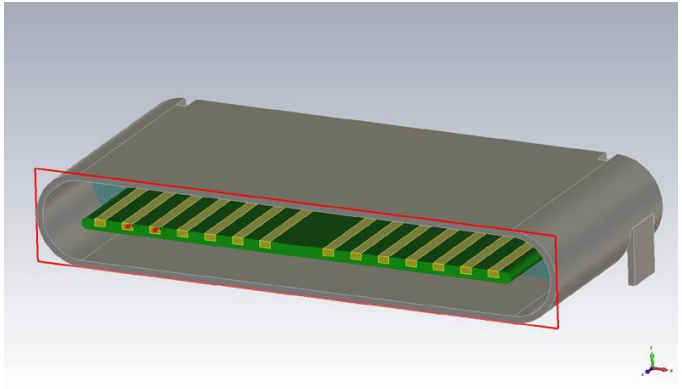
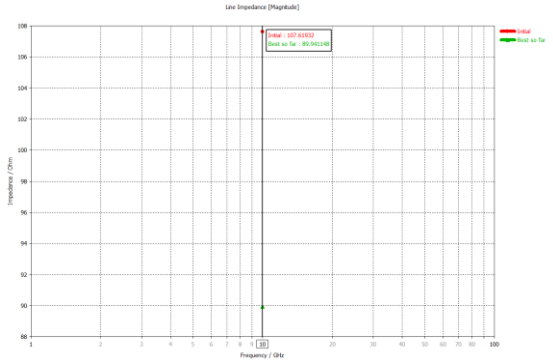
Electrical Design – Line Impedance Optimization

Pin card relative permittivity optimization







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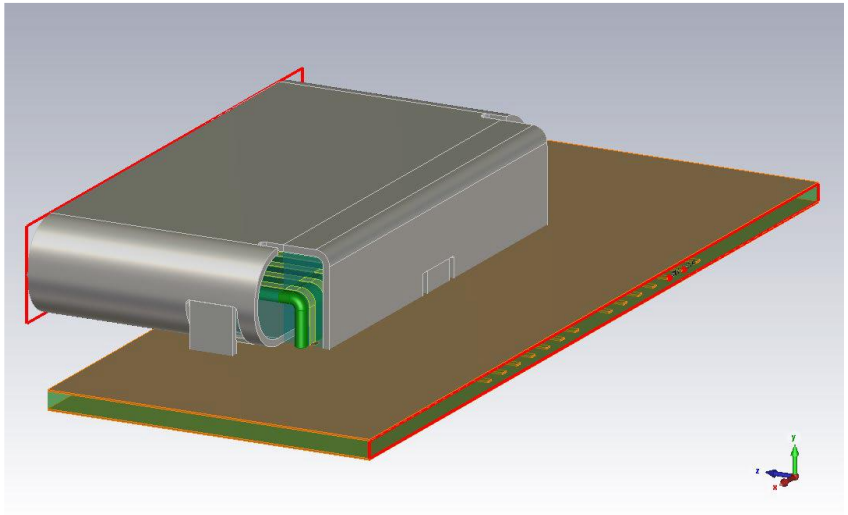
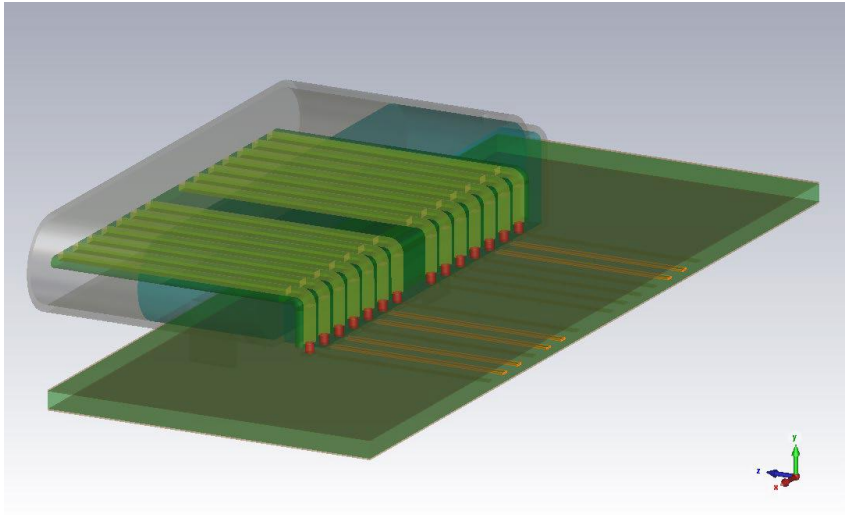
Socket Signal Integrity Design



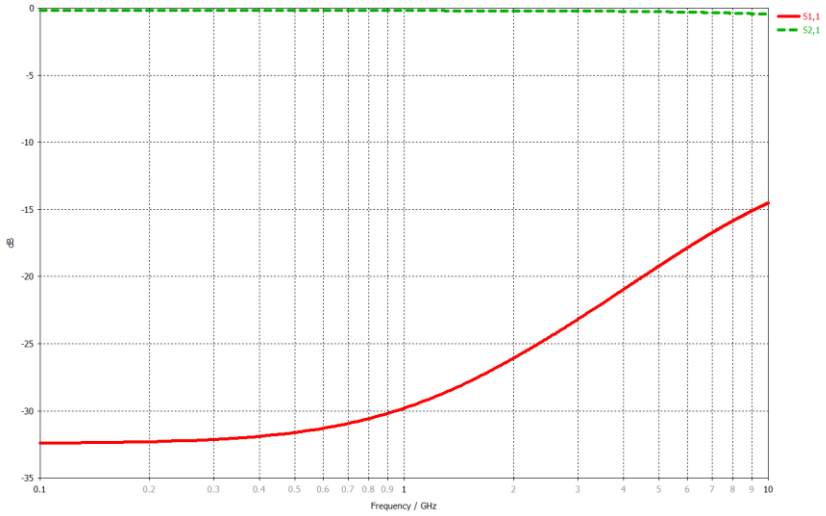
Right angle connection to PCB

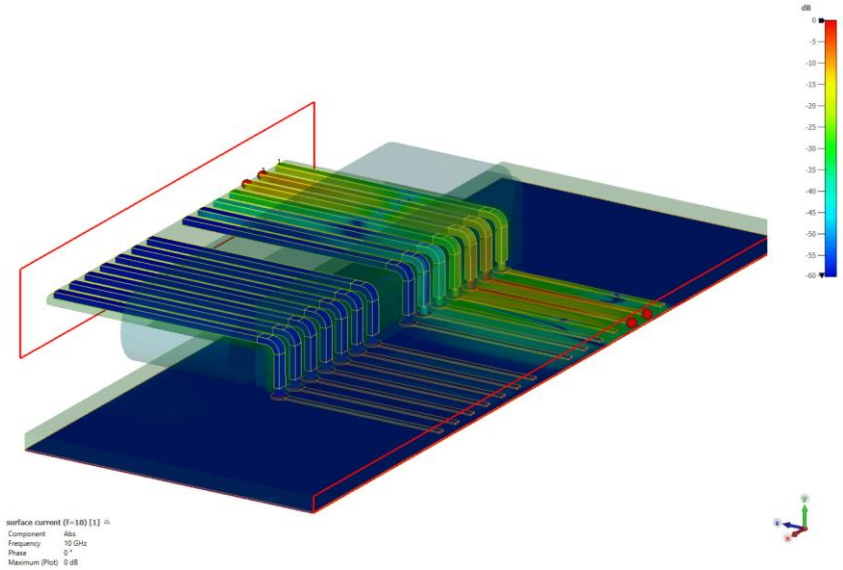


Design transition for minimal reflection

Socket Signal Integrity – S Parameters

S1,1





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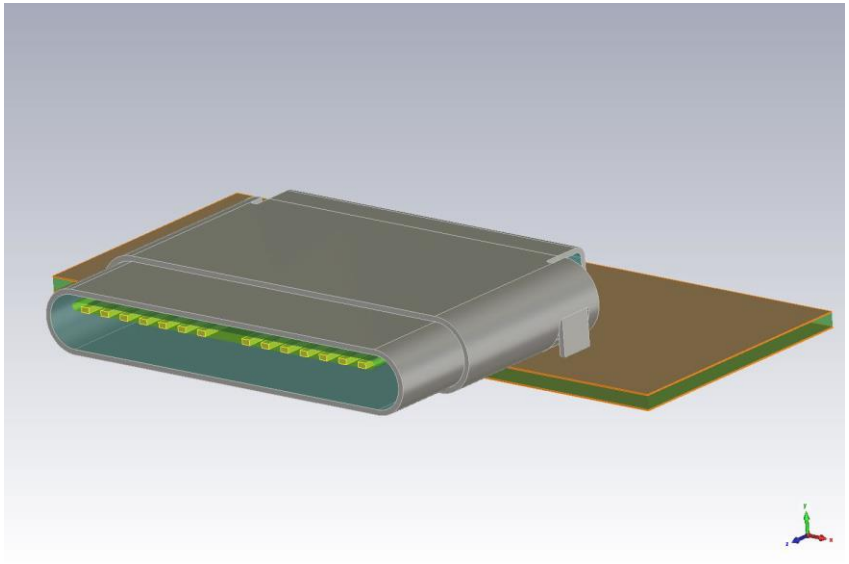
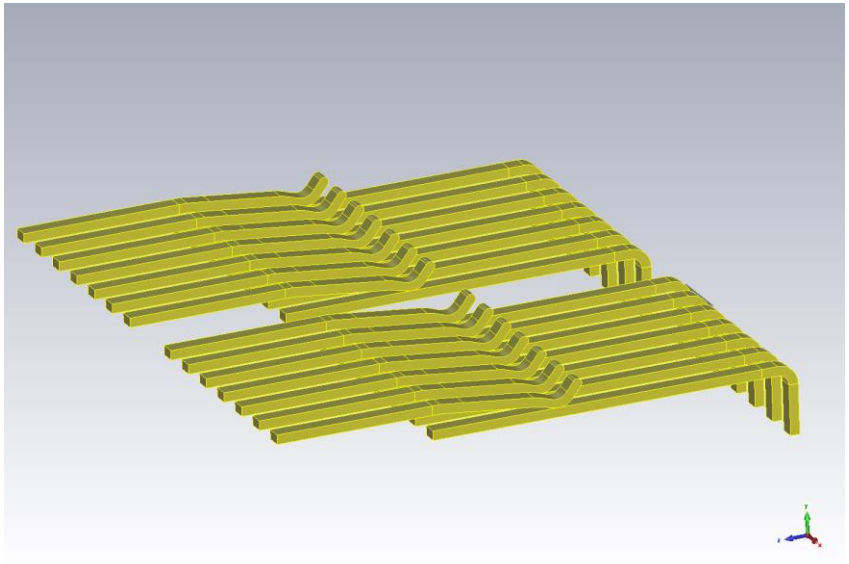
Plug / Socket Transition Design

Structural considerations –sliding parts, insertion force, fatigue

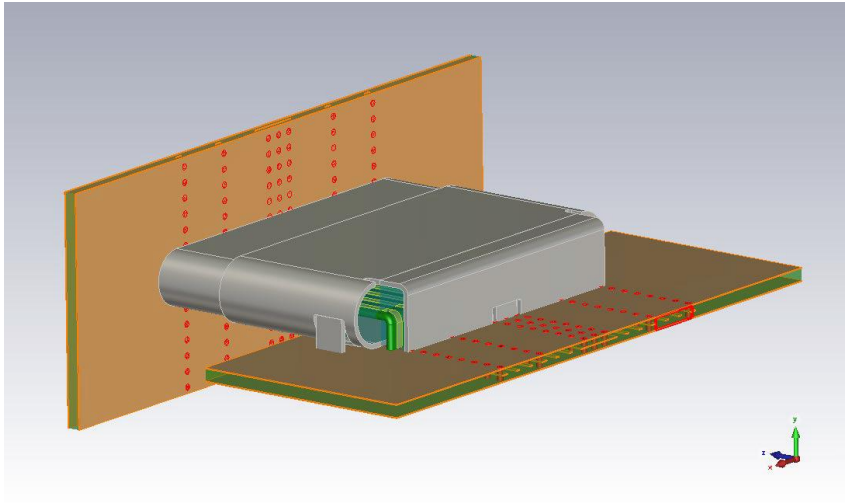


Plug inserted into socket

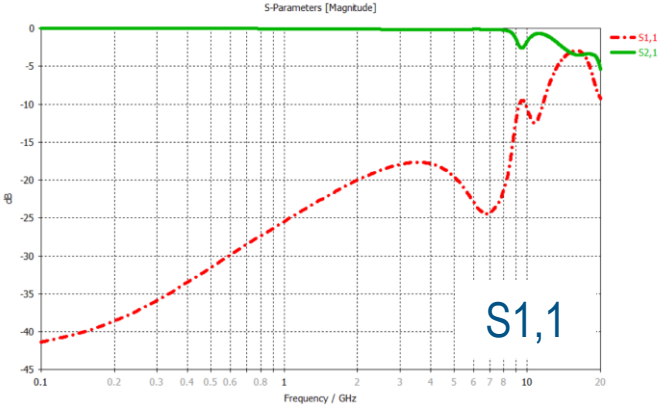


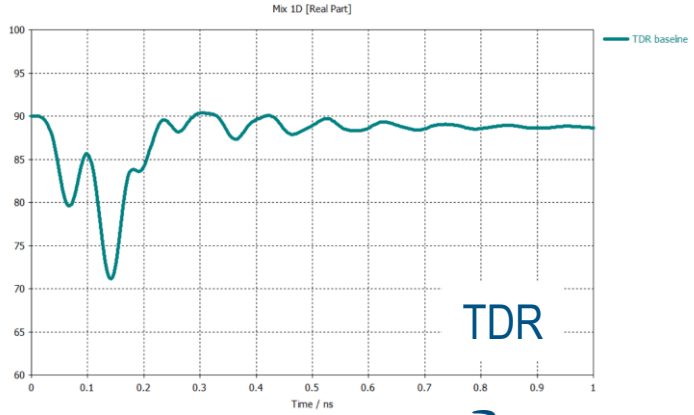
Plug springs in contact with socket pins

Plug / Socket Signal Integrity – S Parameters



Connector Interfaced with Test PCBs





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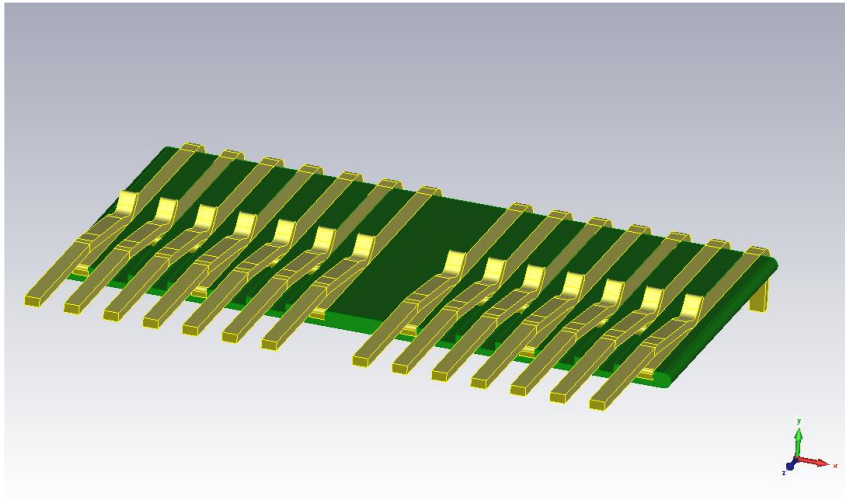
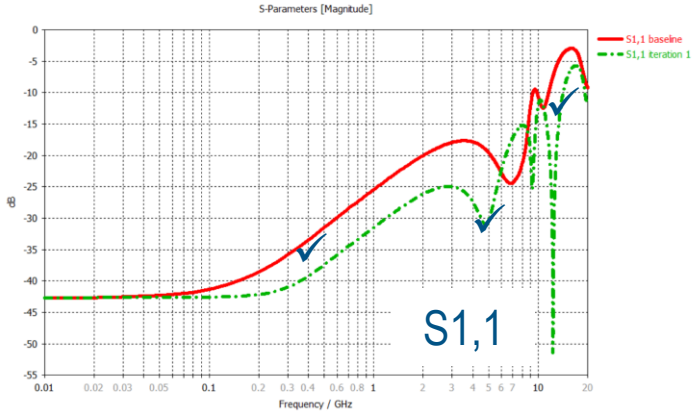
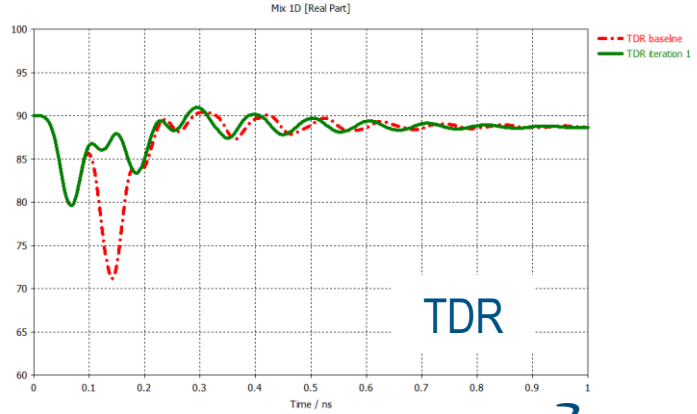
Plug / Socket Signal Integrity – Design Iteration 1



Socket Signal Pins Shortened





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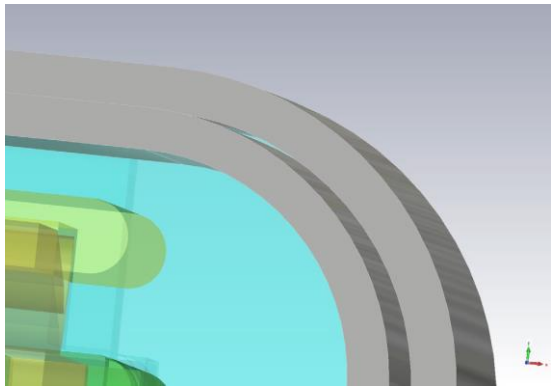
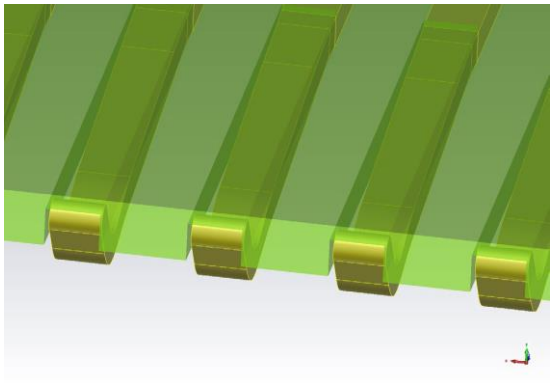
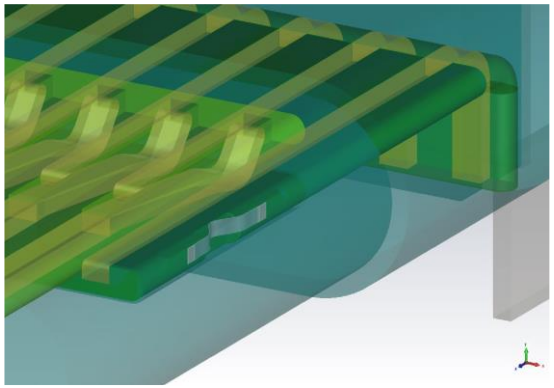
Plug / Socket Signal Integrity – Design Iteration 2



Gap Between Socket & Plug Housings



Gaps Around Plug Pin Springs

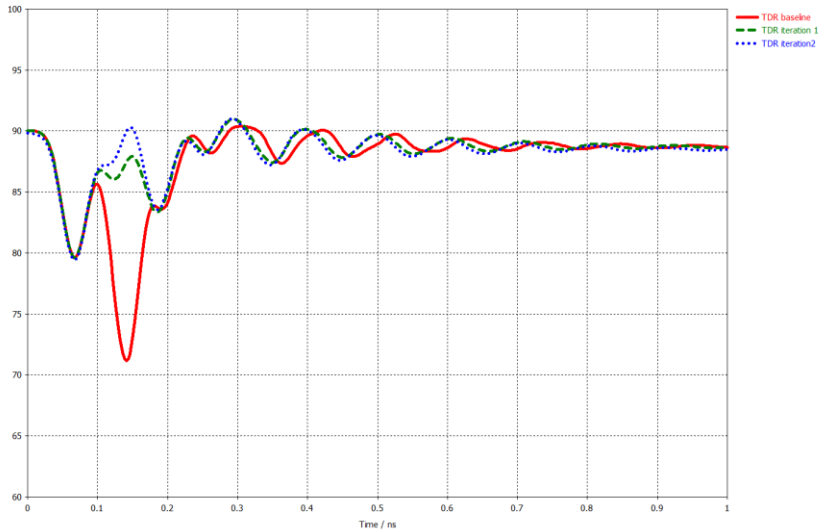


Side Retention Springs

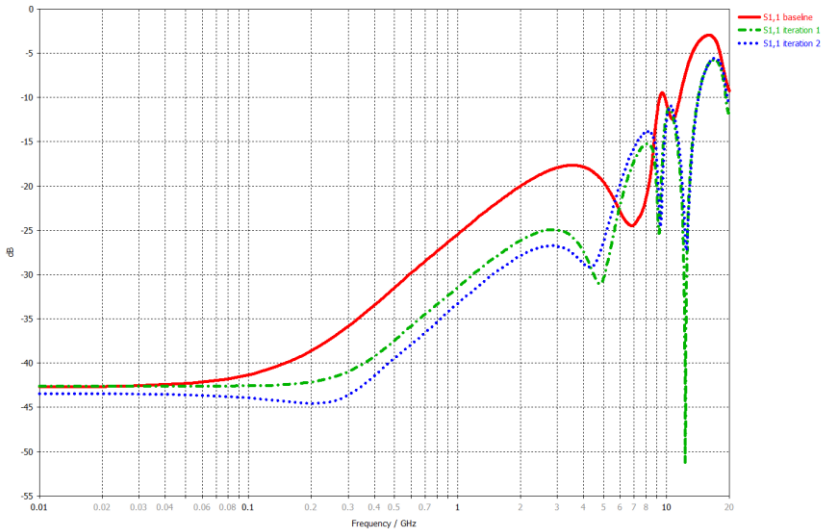
Structural considerations – sliding parts, insertion force, retention, fatigue

Plug / Socket Signal Integrity – Design Iteration 2

TDR



S1,1



EMAG Performance not Adversely Affected by Structural Requirements

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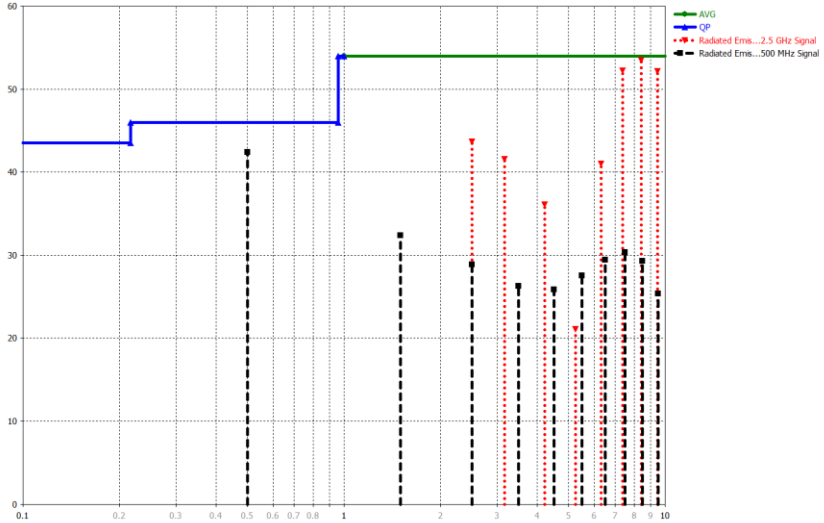
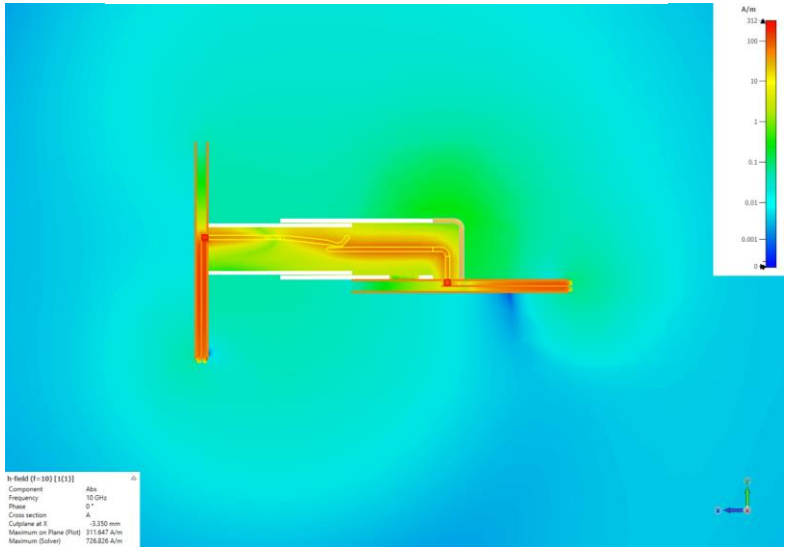
Plug / Socket Transition EMC Performance

Radiated Emissions



Radiated Emissions – H-Field



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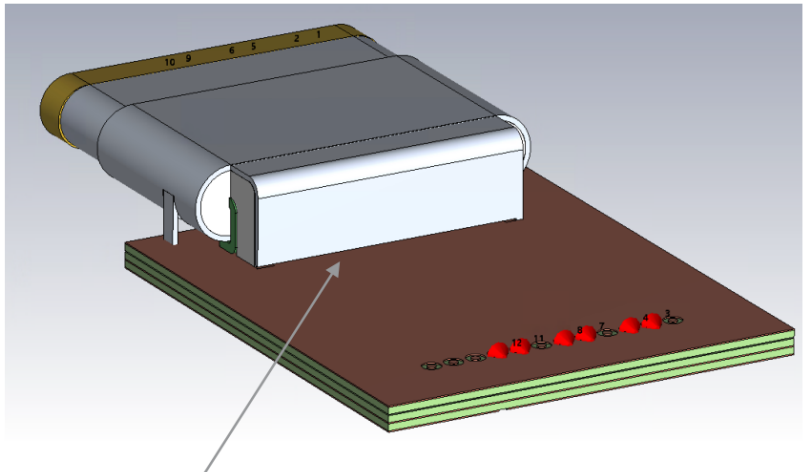
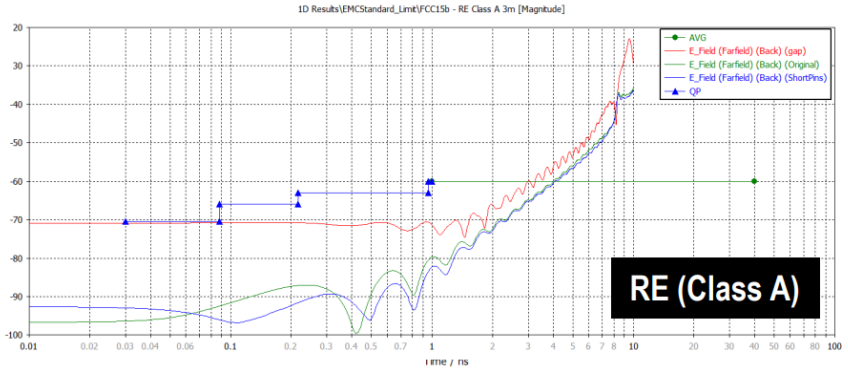
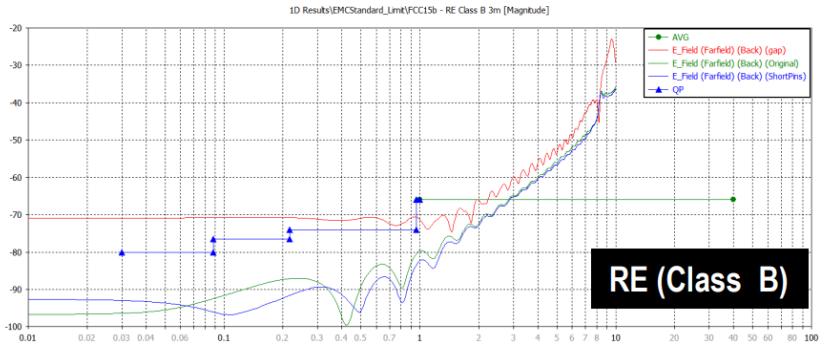
Plug / Socket Transition EMC Performance

Plug / Socket EMC – Radiated Emissions (RE)







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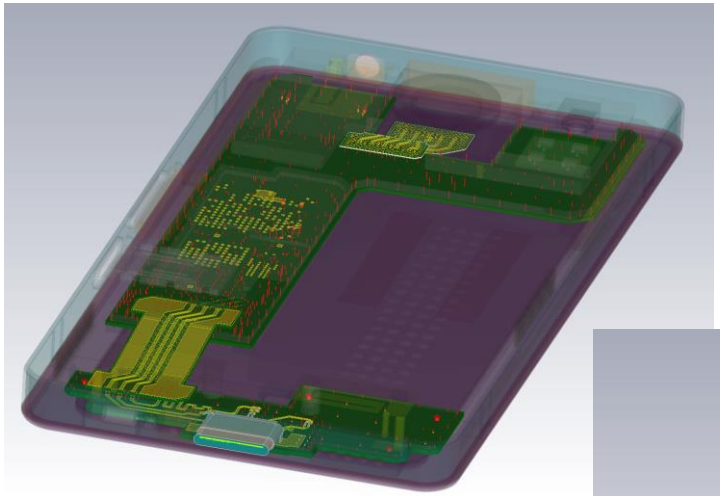
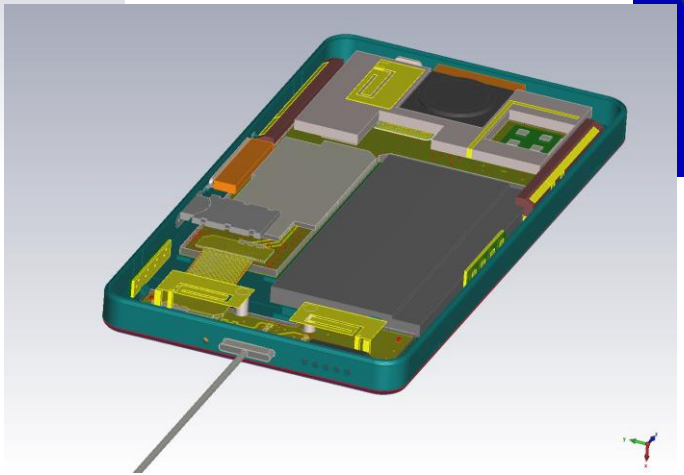
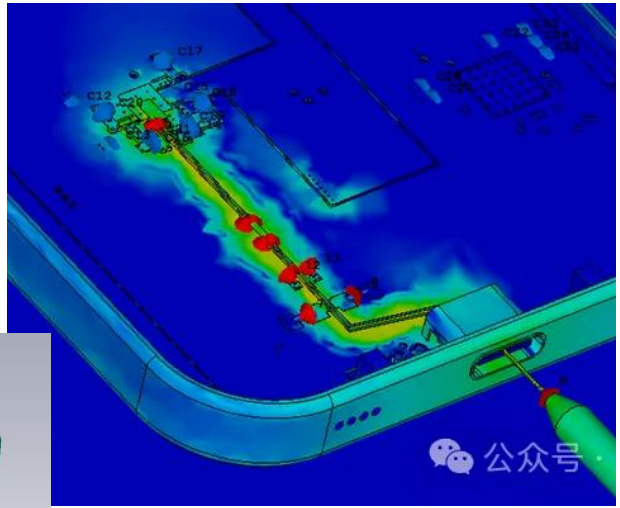
Full System Simulation



Simulate Full Channel SI Performance



Add Cable to Connector



Electrostatic Discharge

https://simutech.com.tw/article/content/370

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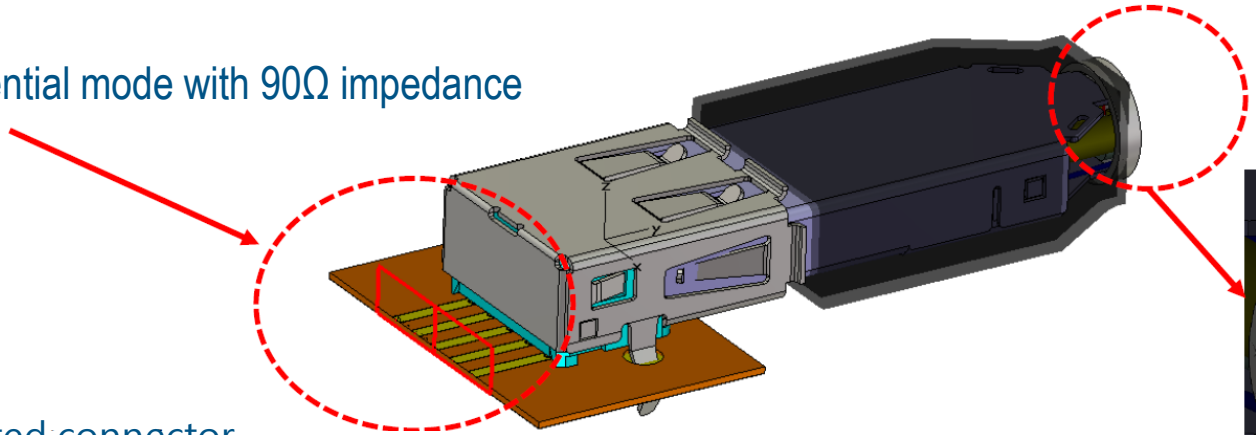
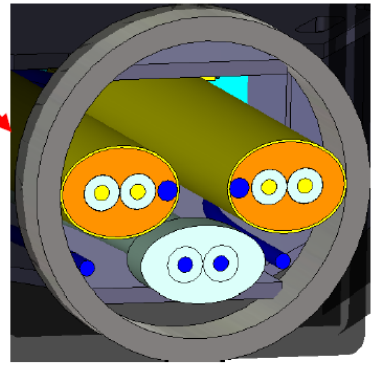
System Level Simulation – Connector plus Cable





Simplified 3D cable cross section

- Mated connector
- Fmax = 11.52GHz for 50ps Trise (20% - 80%)
- T-solver hexahedral mesh (22M mesh)
- Energy decay -40dB
- Open boundary in all directions
- Copper 100% IACS and LCP for plastic component

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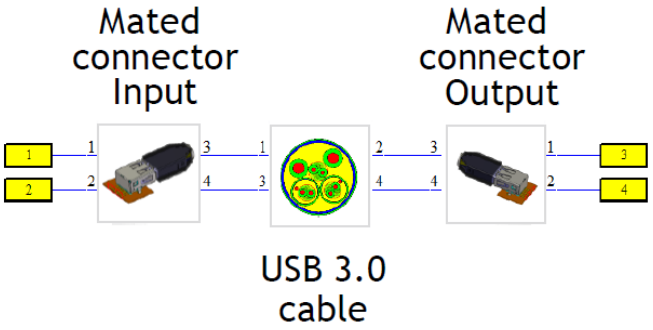
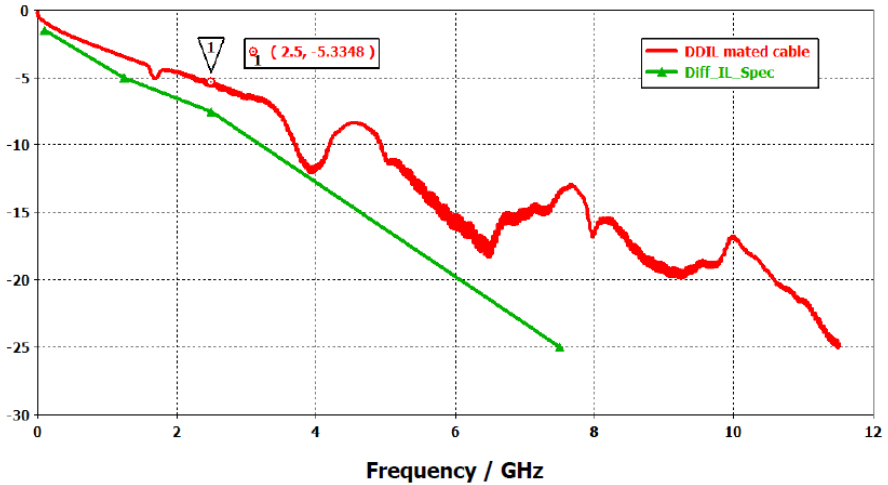
System Level Simulation – Connector plus Cable

- Differential insertion loss -7.5dB @2.5 GHz for mated cable assembly



Circuit simulator
CST DESIGN STUDIO™



5.3dB loss @2.5GHz

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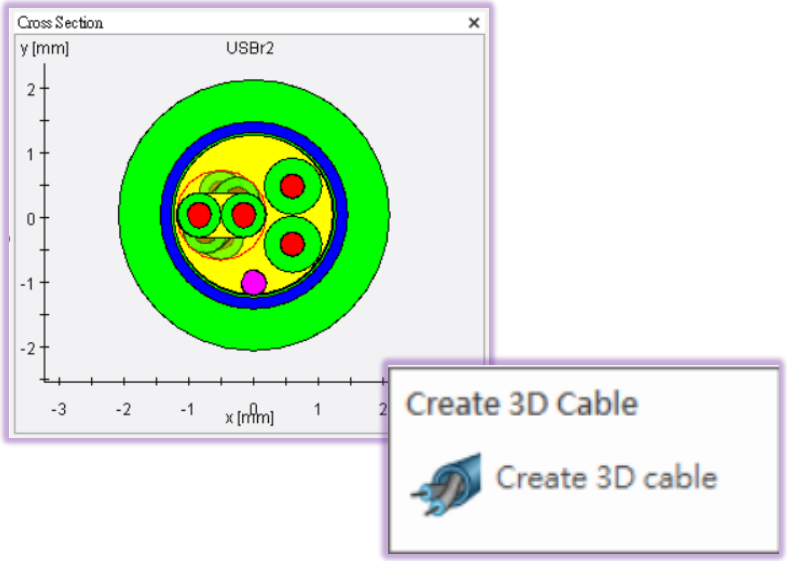
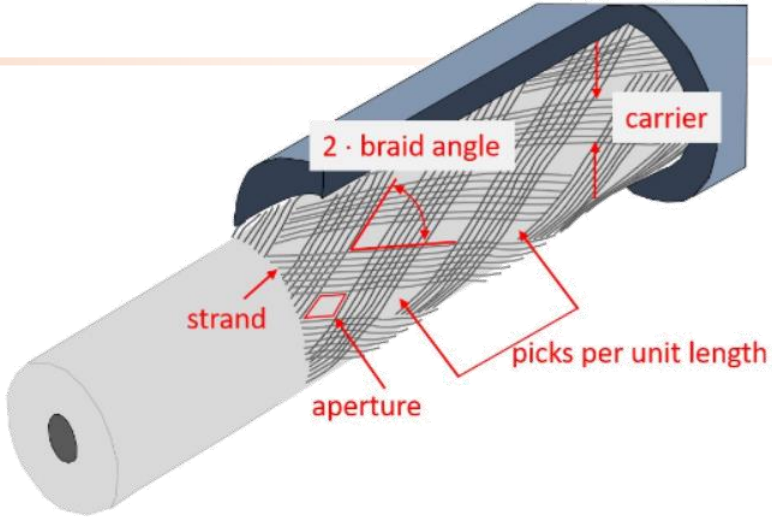
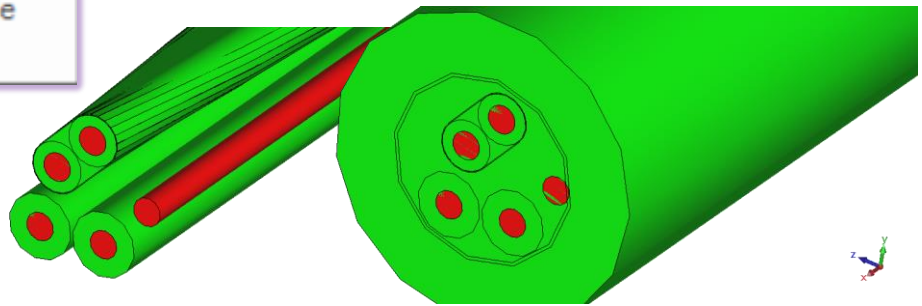
Creating 3D Cable







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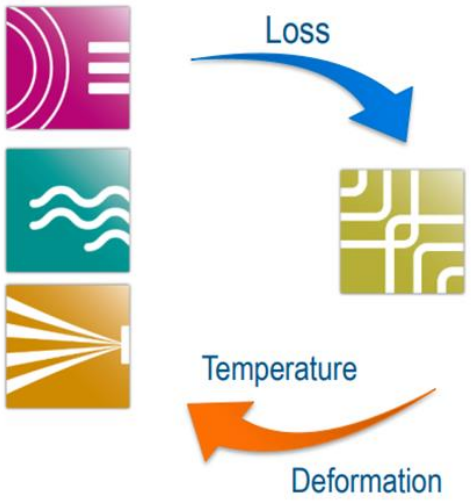
CST MPHYSICS STUDIO®

Shared GUI
Seamless EM-MPS link



Classic Thermal

THs THt

- Steady State and Transient
- Tet and Hex Meshes
- Moving Media
- Bio-heat transfer

Conjugate Heat Transfer

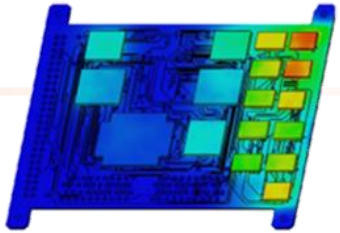
CHT

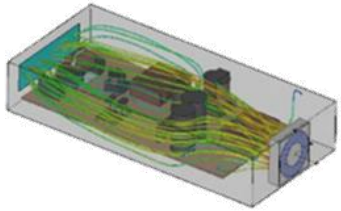
- Solve thermal conduction, convection and radiation using CFD
- Laminar and turbulent flow
- Octree meshing, GPU support
- Fan, flow resistance, compact IC model, automatic altitude correction

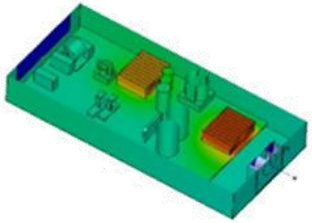
Structural Mechanics

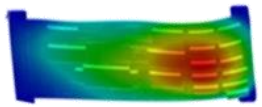
ST

- Tet mesh, displacement, force
- Thermal stress from temp distribution









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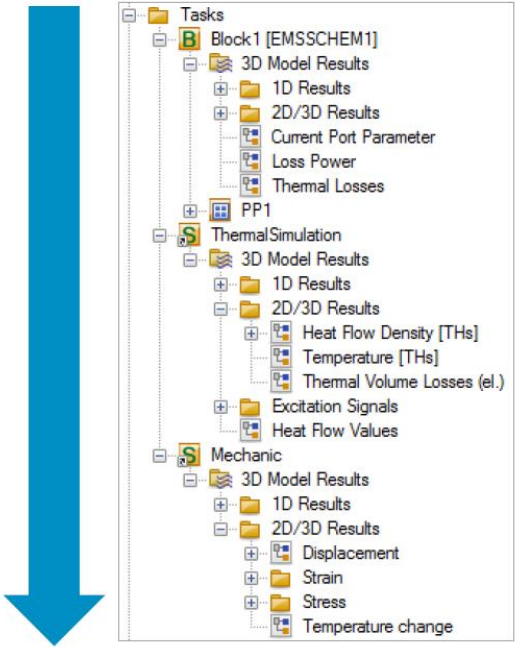
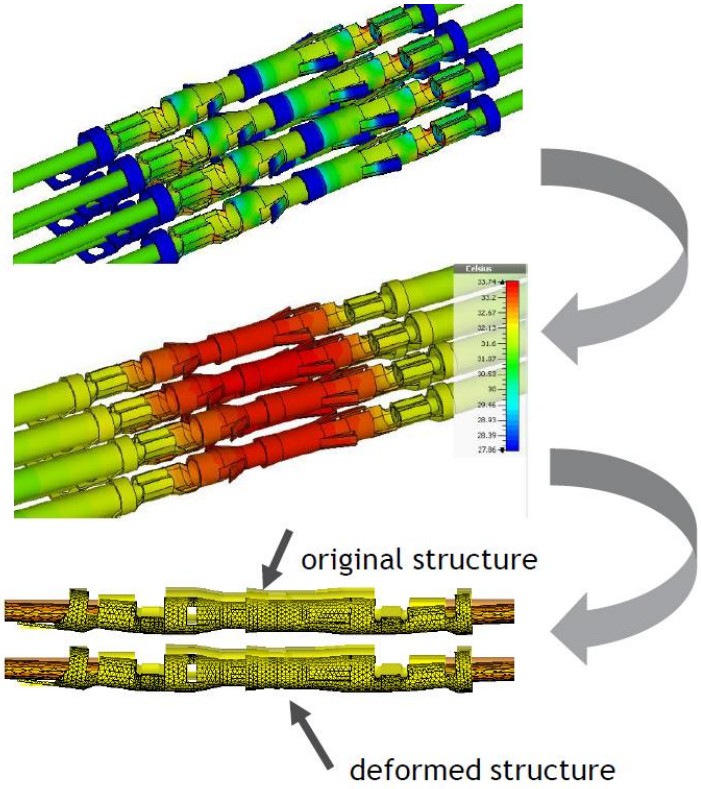
CST MPHYSICS STUDIO® for Connectors



Automatic update all tasks!



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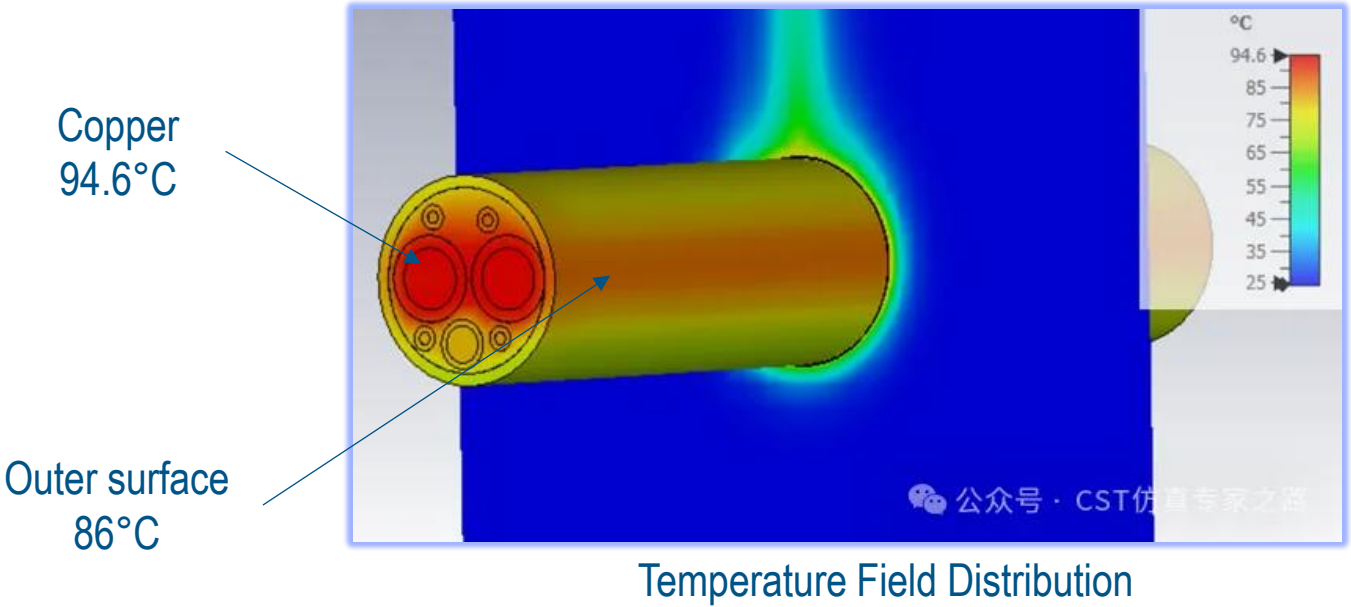
電動車直流快充 Cable 熱模擬

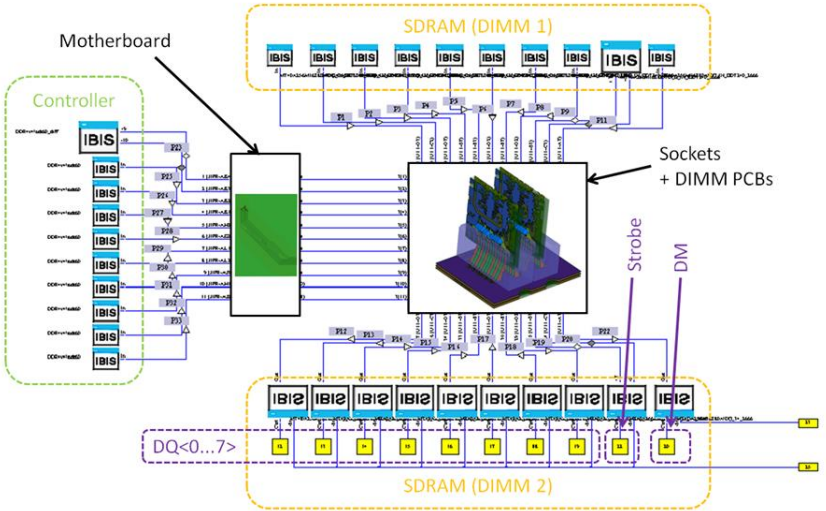
- 設定 current 為 300A，透過 Js solver 的計算得到 Thermal loss 為 7.9W。
- 我們使用 CHT solver 對此場景進行模擬。可以看到在 300A 電流的情況下，Cable 中心銅線最高溫度達到了 94.6°C，Cable 表面的溫度則來到了 86°C。



Temperature Field Distribution

CST案例：電動車直流快充Cable熱模擬
https://simutech.com.tw/article/content/374

System Level Simulation



- Passivity/causality violations can give inaccurate models
- Errors from measurement data:
  - **improper calibration and de-embedding**
  - human mistakes
  - measurement noise
- Errors from simulation data:
  - poor meshing
  - inaccurate solver
  - bad models or assumptions on material properties
  - human mistakes
  - improper use of data interpolation or extrapolation features of the solver
  - putting together results from two solvers

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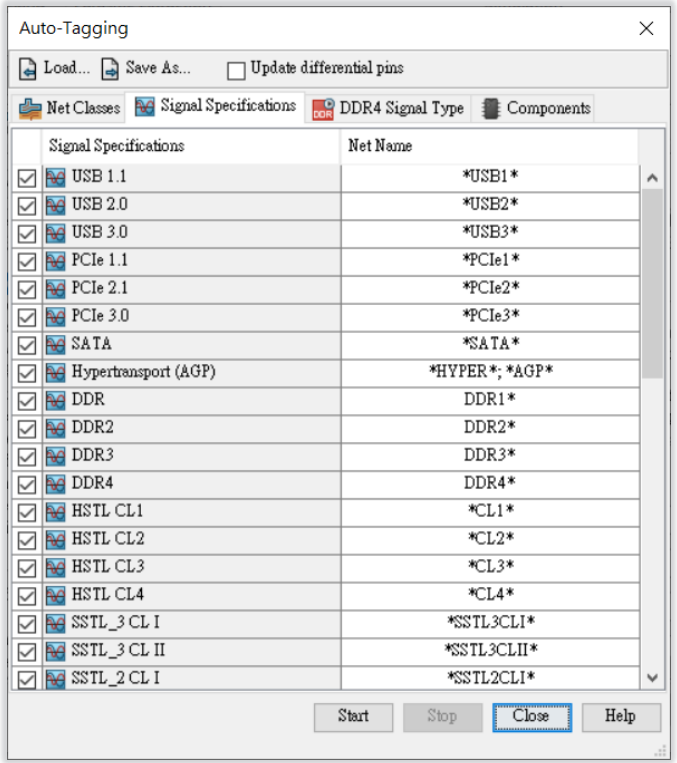
CST Boardcheck: Rules



EMC Rules

- Signal Reference
  - Net Crossing Split
  - Net Changing Reference
  - Net Near Edge of Reference
- Wiring/Crosstalk
  - Critical Net Near I/O Net
  - Exposed Critical Trace Length
  - Critical Net Isolation
  - Critical Differential Net Isolation
  - Critical Differential Net Matching
  - Wide Power/Ground Traces
- Decoupling
  - Decoupling Capacitor Density
  - Power Pin Capacitor Distance
  - IC Power/Ground Pin-Via Distance
  - Decoupling Cap Distance to Via
  - Power/Ground Trace Decoupling
  - Power Via Density
- Placement
  - I/O Filter Distance
  - Distance from Oscillator to Clock Driver

SI Rules

- Net Integrity
  - Net Length
  - Net Coupling
  - Exposed Critical Trace Length
  - Net Stub
  - Net Crossing Split
  - Net Near Edge of Reference
  - Between Ref Plane Routing
- Via Integrity
  - Unconnected Via Pads
  - Via Clearance Overlap
  - Via->Net Coupling
  - Via Stub
- Power Integrity
  - Wide Power/Ground Traces
  - Decoupling Capacitor Density
  - Power Pin Capacitor Distance
  - IC Power/Ground Pin-Via Distance
  - Decoupling Cap Distance to Via
  - Power/Ground Trace Decoupling
  - Power Vias

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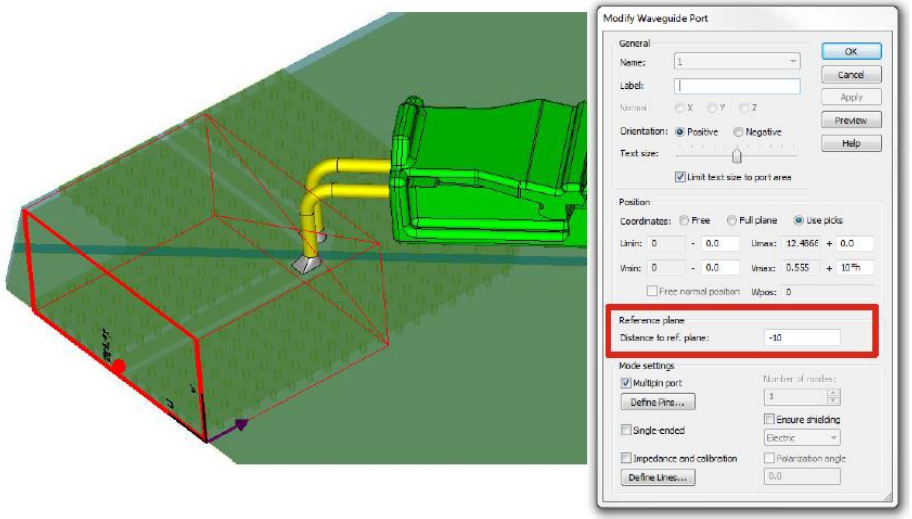
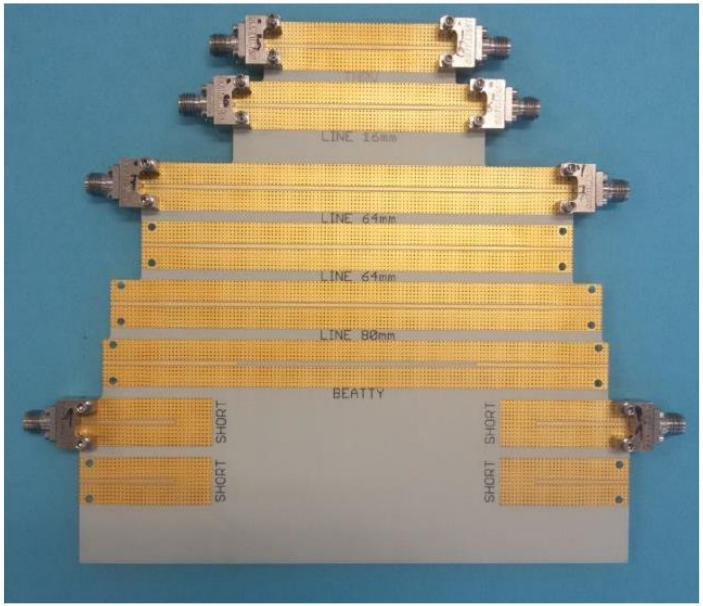
'Virtual' Calibration

In CST MWS:



In laboratory:
Multiline TRL calibration kit



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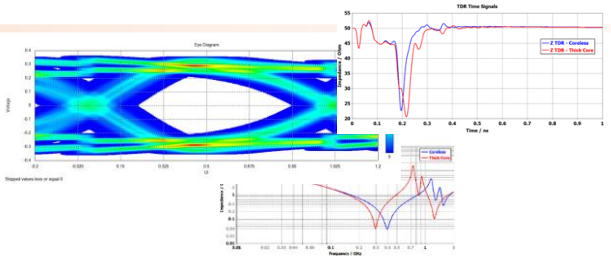
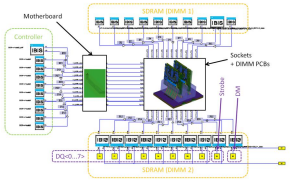
IdEM-Based Simulation Flow

7 SI/PI analysis

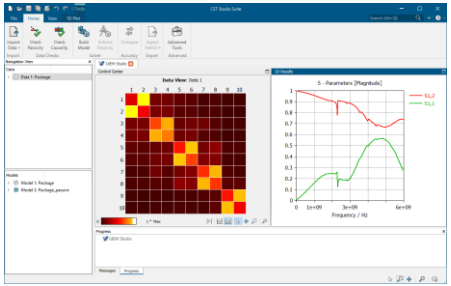


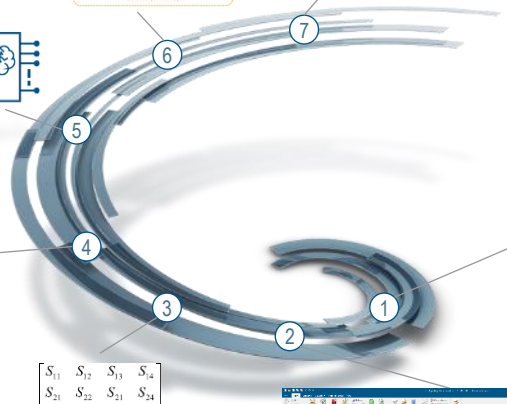
6 Circuit solver



5 IdEM output surrogate model

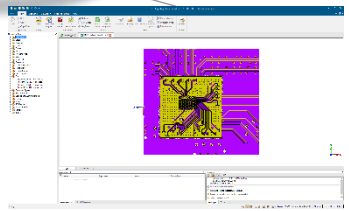
4 IdEM



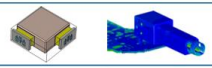
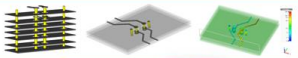
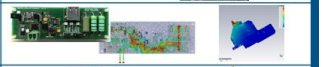


$$\begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{21} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix}$$

3 EMAG output
S-parameters
or Touchstone file



1 Electrical interconnects: showcases

Connectors	
Vias, via fields	
Packages	
PDN	
Backplane links	

2 EMAG simulation or measurements

- *Data certification*
- *Model generation: passive and causal*
- *Frequency-time domains: bridge the gap*

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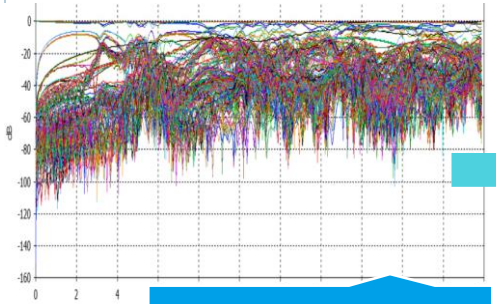
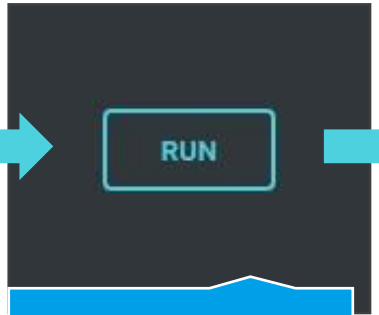
InSPECTOR

- A new tool to aid the signal integrity assessment of connectors.
- Simple to use.

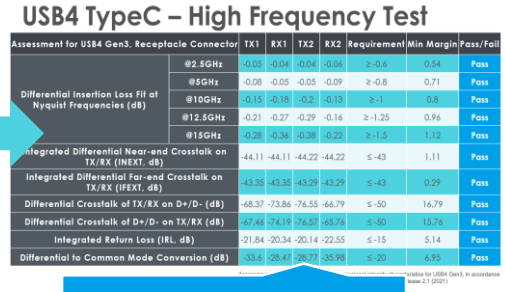


Read S-parameters (Touchstone)

Identify port numbering



Run



View report

Developed by Simutech

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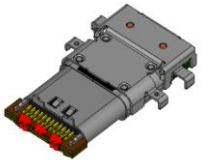
Specifications

- ▶ USB4 Gen3 Mated Connector Signal Integrity.
  - In accordance with Table 3-29 USB Type-C Cable and Connector Specification, August 2019.



- ▶ PCIe 5.0 M.2 Connector Signal Integrity for 32.0 GT/s.
  - In accordance with Table 6-3 PCI Express M.2 Specification, Rev 5.0, Version 0.7, June 24, 2022.

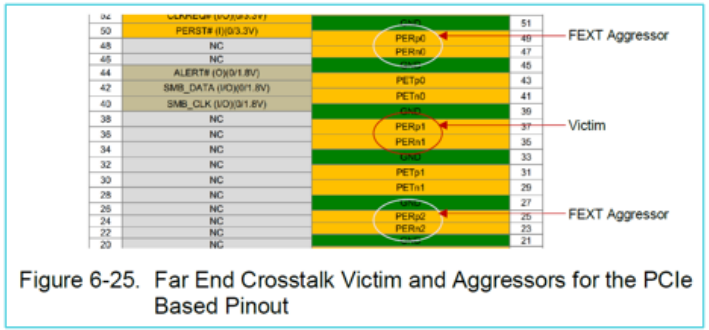


Figure 6-25. Far End Crosstalk Victim and Aggressors for the PCIe Based Pinout

Crosstalk Definition

Inspector

PCIe 5.0 M.2 Connector

- The assessment requires the calculation of component contribute integrated crosstalk noise (ccICN).
- Inspector can help with the post-processing required for the assessment.

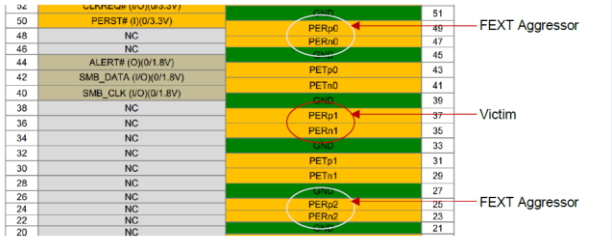


Figure 6-25. Far End Crosstalk Victim and Aggressors for the PCIe Based Pinout

Crosstalk Definition

Equation 6-1.Component Contribute Integrated Crosstalk Noise – $ccICN_{NEXT}$

$$ccICN_{NEXT} = \sqrt{\frac{1}{2}df\sum_{k=1}^{N_{max}}\left(\frac{A_{NT}^{2}}{f_b}\right)sinc^2(k\cdot df/f_b)10^{\left(2\frac{IL_{post-channel}(k)}{10}\right)}\left[\frac{1}{1+\left(\frac{k\cdot df}{f_t}\right)^4}\right]\left[\frac{1}{1+\left(\frac{k\cdot df}{f_r}\right)^8}\right]10^{\frac{MDNEXT(k)}{10}}}$$

Equation 6-2.Component Contribute Integrated Crosstalk Noise – $ccICN_{FEXT}$

$$ccICN_{FEXT} = \sqrt{\frac{1}{2}df\sum_{k=1}^{N_{max}}\left(\frac{A_{FT}^{2}}{f_b}\right)sinc^2(k\cdot df/f_b)10^{\left(\frac{IL_{pre-channel}(k)}{10}+\frac{IL_{post-channel}(k)}{10}\right)}\left[\frac{1}{1+\left(\frac{k\cdot df}{f_t}\right)^4}\right]\left[\frac{1}{1+\left(\frac{k\cdot df}{f_r}\right)^8}\right]10^{\frac{MDFEXT(k)}{10}}}$$

- $IL_{pre-channel}(k) = -\left(\frac{27.75}{f_b/2}\right)k.df$, $IL_{post-channel}(k) = -\left(\frac{7.5}{f_b/2}\right)k.df$
- f_{max} = 24 GHz, f_{min}=10 MHz, df = 10 MHz, f_b = 32 GHz
- A_{FT}= 800 mVpp, A_{NT}= 800 mVpp
- f_t = 31.53 GHz, f_r = 24 GHz

ccICN Definition

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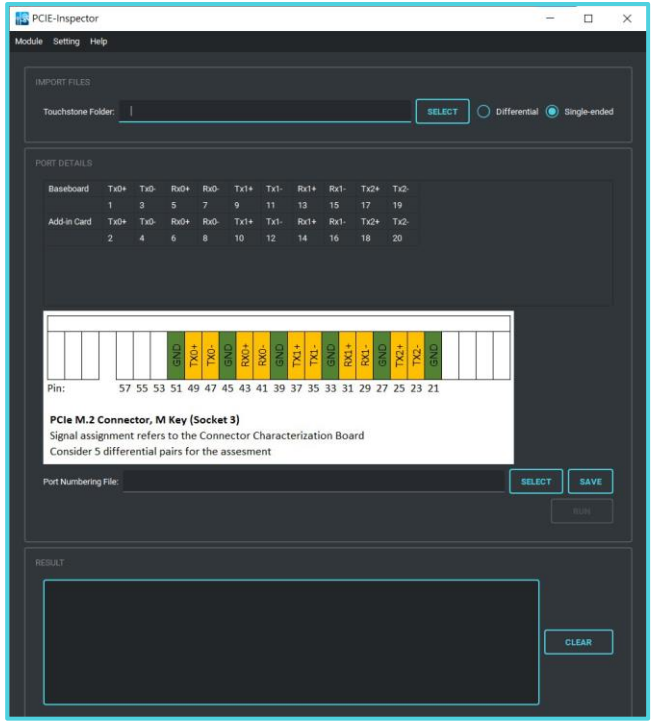
PCIe 5.0 M.2 Connector

- Complete the connector analysis in CST and export the TOUCHSTONE file.
- Import the TOUCHSTONE file into Inspector and specify the pin layout.



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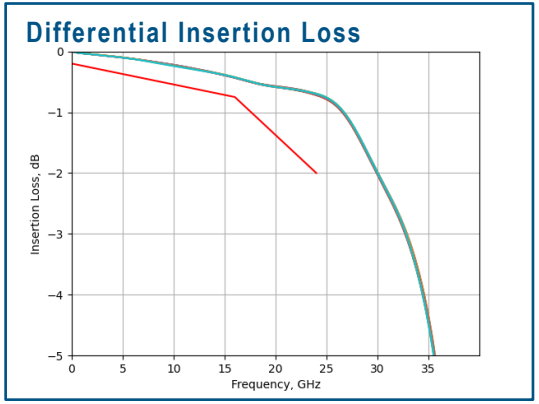
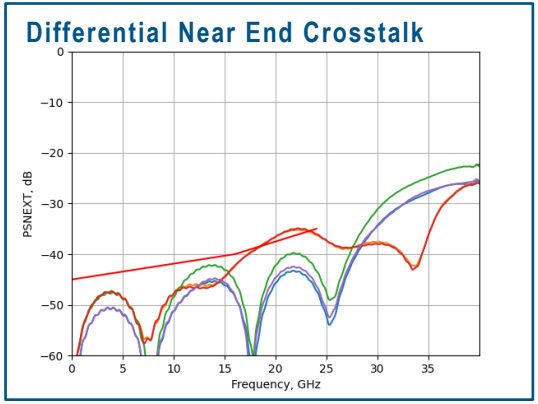
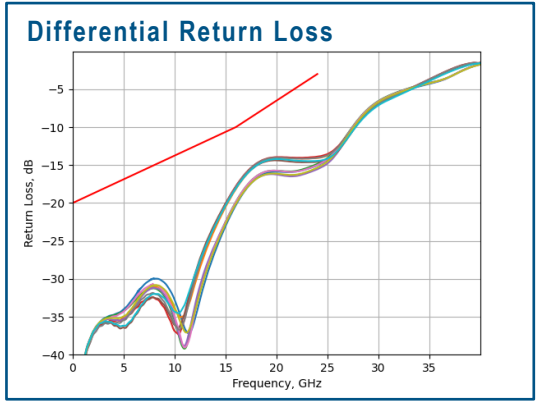
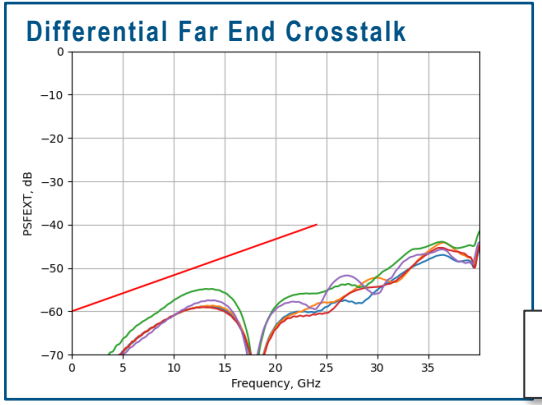
PCIe 5.0 M.2 Connector









All plots and tables are compiled into a report

Inspector

PCIe 5.0 M.2 Connector

Signal Integrity Requirements and Test Procedures for 32.0 GT/s M.2 Connectors					
Pair	Tx0	Rx0	Tx1	Rx1	Tx2
Differential Insertion Loss (DDIL)	Pass	Pass	Pass	Pass	Pass
Differential Return Loss (DDRL)	Pass	Pass	Pass	Pass	Pass
Differential Near End Crosstalk (DDNEXT)	Pass	Fail	Pass	Fail	Pass
Component Contribute Integrated Crosstalk Noise ($cclCN_{NEXT}$)	1646.56	1605.62	2412.46	1593.71	1648.75
Differential Far End Crosstalk (DDFEXT)	Pass	Pass	Pass	Pass	Pass
Component Contribute Integrated Crosstalk Noise ($cclCN_{FEXT}$)	66.41	67.93	98.87	66.51	69.91

All plots and tables are compiled into a report

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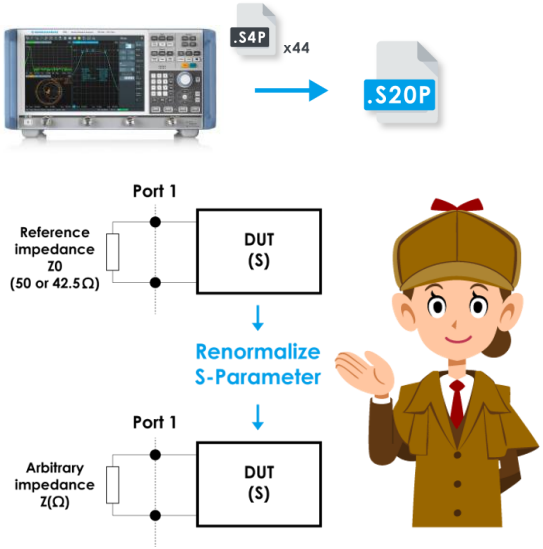
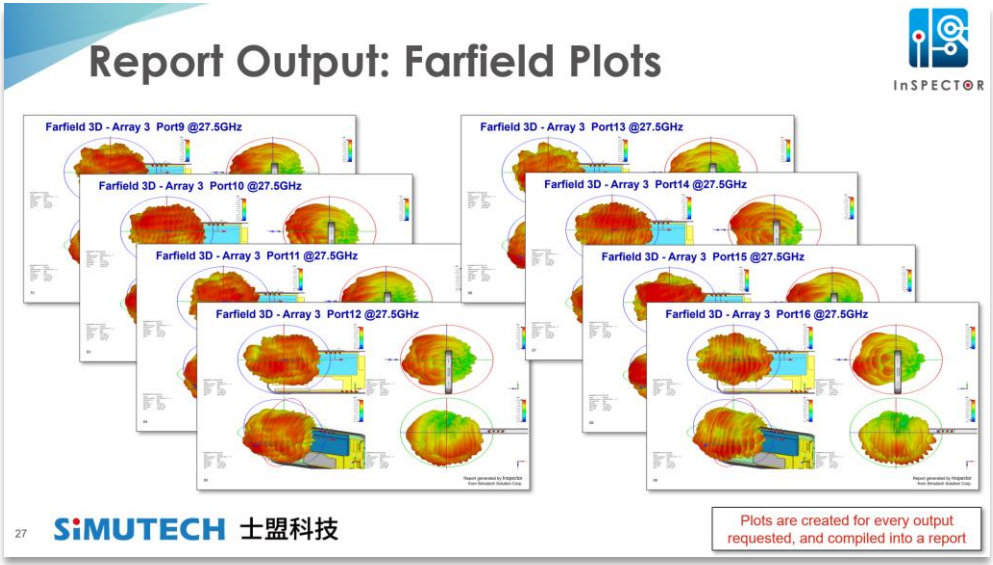
Additional Functions

Combine and normalize Touchstone files



Auto-report function for antenna simulations



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Inspector Links

- Inspector 規範檢核軟體
  https://simutech.com.tw/article/content/292
- Inspector 2023 推出全新後處理功能
  https://simutech.com.tw/article/content/324
- Inspector 2023推出全新 PCIe 5.0 規範檢核功能
  https://simutech.com.tw/article/content/341
- [天線]
  Inspector新功能 - AutoReport助您成為分析報告達人*New* 🔥
  https://simutech.com.tw/article/content/350

Summary

- PCIe Gen 7 will require high speed connectors and add-in cards to enable fast data transfer.
- 3D simulation is essential for high-speed SI analysis.
- CST Studio Suite provides a suite of solvers for EM and Multiphysics.
- MODSIM approach for modeling and simulation.
- System level simulation enables mixture of 3D and schematic analysis for complicated systems.
- Multiphysics considerations cannot be neglected – MPHYSICS Studio included in CST.
- Enhanced models for system simulation using IdEM.
- Additionally, Inspector is very useful for post-processing PCIe connector analysis results.

Contact Us

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