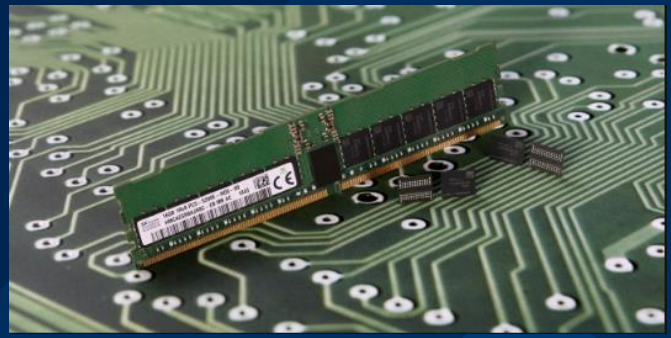
R&S RTP Oscilloscope

(LP)DDR5 MEMORY INTERFACE SIGNAL INTEGRITY DEBUGGING & COMPLIANCE TESTING



Guido Schulze, Product Manager Oscilloscopes
Johannes Ganzert, Senior Application Engineer Oscilloscopes

ROHDE&SCHWARZ

Make ideas real

OUTLINE

- DDR Memory Refresher
- (LP)DDR5 Details
- Signal Integrity Debugging
- Compliance Testing with R&S ScopeSuite
- Live Demonstration
- Summary

DDR MEMORY TECHNOLOGY - REFRESHER

DDR SDRAM

What is DDR?

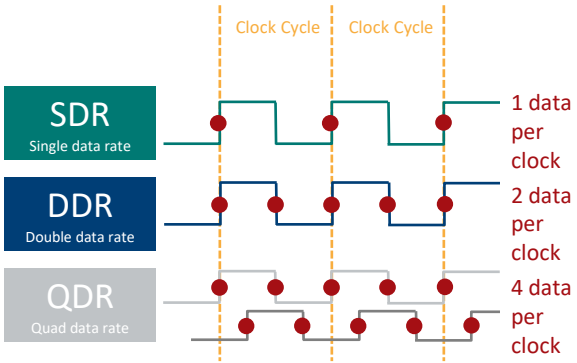
- Double-Data Rate
- Data bit is transmitted at both rising and falling edges of clock

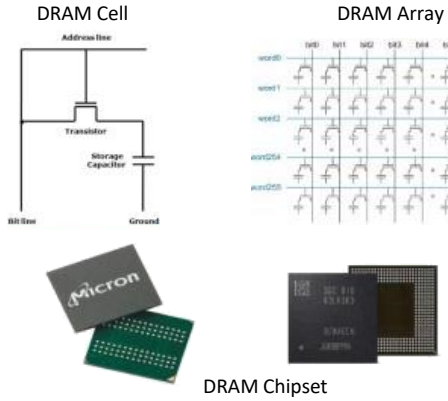
What is SDRAM?

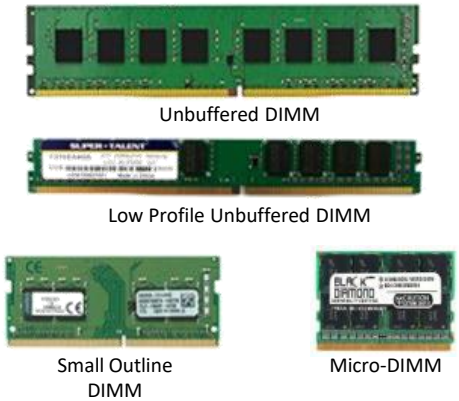
- Synchronous Dynamic Random Access Memory
- Volatile memory that can store data fast but temporarily

What is DIMM?

- Dual Inline Memory Module
- Commonly found in PC & servers as array of SDRAMs

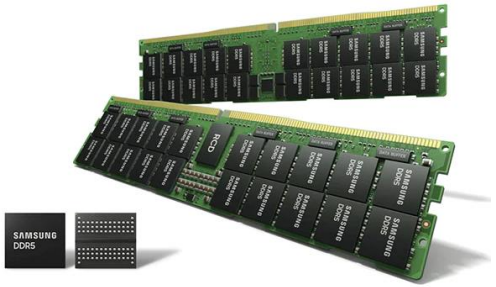




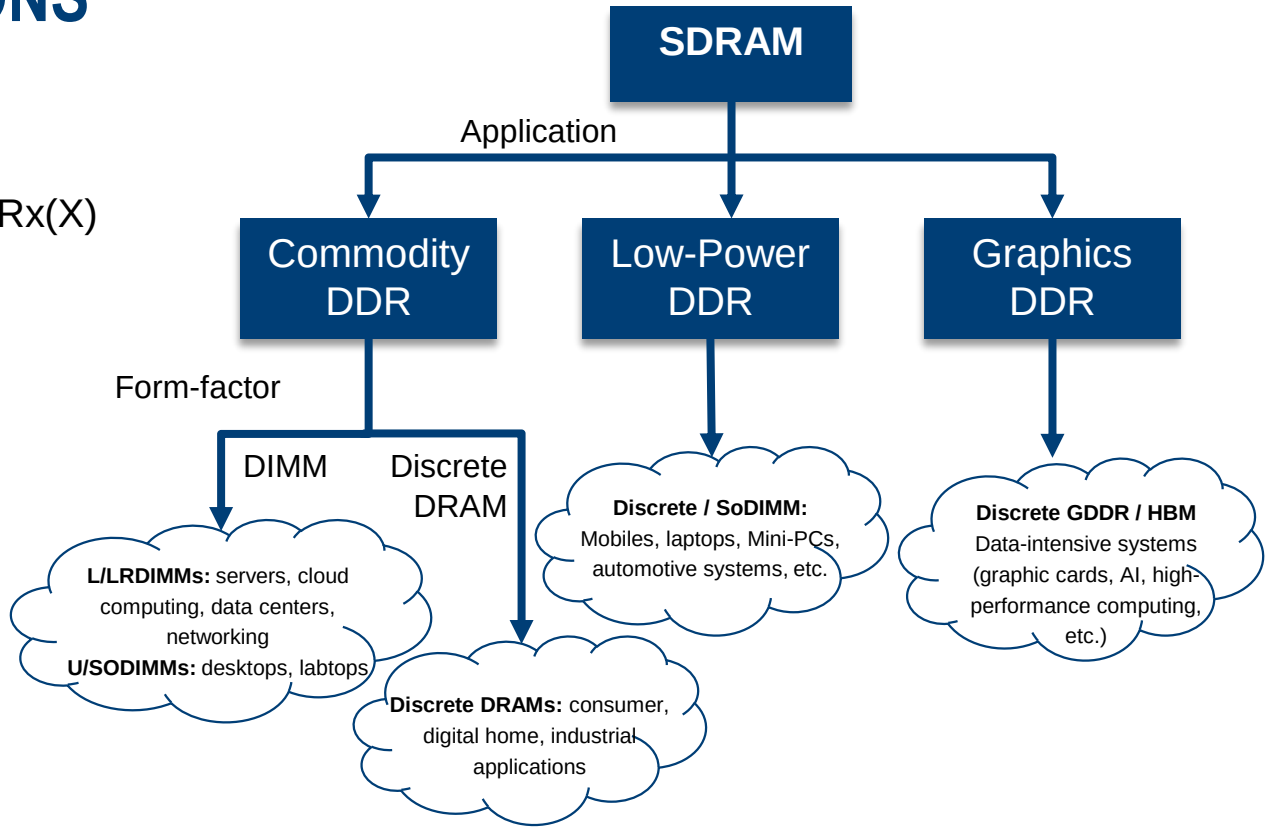


SDRAM APPLICATIONS

- **SDRAM Types:**
  - Main memory: DDRx(L)
  - Low Power / Mobile: LPDDRx(X)
  - Graphics: GDDRx(X)



Source: Samsung



DDR SDRAM: THE KEY SPECS

Clock Frequency

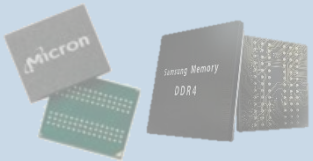
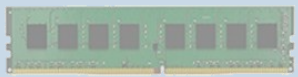
Transfer 2 bits per clock

Data bandwidth = 64-bit * transfer rate

Standard	Release year	Chip	Bus			Voltage (V)
		Prefetch	Clock rate (MHz)	Transfer rate (MT/s)	Bandwidth (GB/s)	
SDR	1993	1n	66 .. 133	66 .. 133	0.53 .. 1.06	3.3
DDR	1998	2n	100 .. 200	200 .. 400	1.6 .. 3.2	2.5
DDR2	2003	4n	200 .. 533	400 .. 1066	3.2 .. 8.5	1.8
DDR3	2007	8n	400 .. 1066	800 .. 2133	6.4 .. 17.066	1.5/1.35
DDR4	2014	8n	800 .. 1600	1600 .. 3200	12.8 .. 25.6	1.2/1.05
DDR5	2020	16n	1600 .. 4400	3200 .. 8800	25.6 .. 70.4	1.1
DDR6	2025			.. 12800 (17600)	102.4 (136)	

TYPICAL DDR TEST SCENARIOS

- **Focus on System Test:**
  - Measure signal integrity to verify quality of board design margin
  - Prove signal integrity for customers
  - Debug signal integrity issues on the memory interface

SDRAM Chip	DIMM	Memory Controller	PCB (DDR-System)
			   Computer board Application specific boards
▪ Most tests are done on wafer or dedicated fixture ▪ Full electrical, protocol and functional testing	▪ Test are mainly done in fixture board ▪ Full electrical protocol and functional testing ▪ Test required with different SDRAM chip ▪ DIMM raw card are per JEDEC design hence focus is more on performance	▪ Ensure controller signals meet the JEDEC requirement ▪ Test with different SDRAM and DIMM for interoperability ▪ Need to do thorough validation based on different functions	▪ Using SDRAM or DIMM with Memory controller on the PCB will require electrical and functional testing ▪ Can be found in slightly more complex setup, range from simple embedded application to high-end server computing ▪ Focus on design margin of the board and compliance report

DDR SYSTEM – SIGNAL INTEGRITY LIMITS

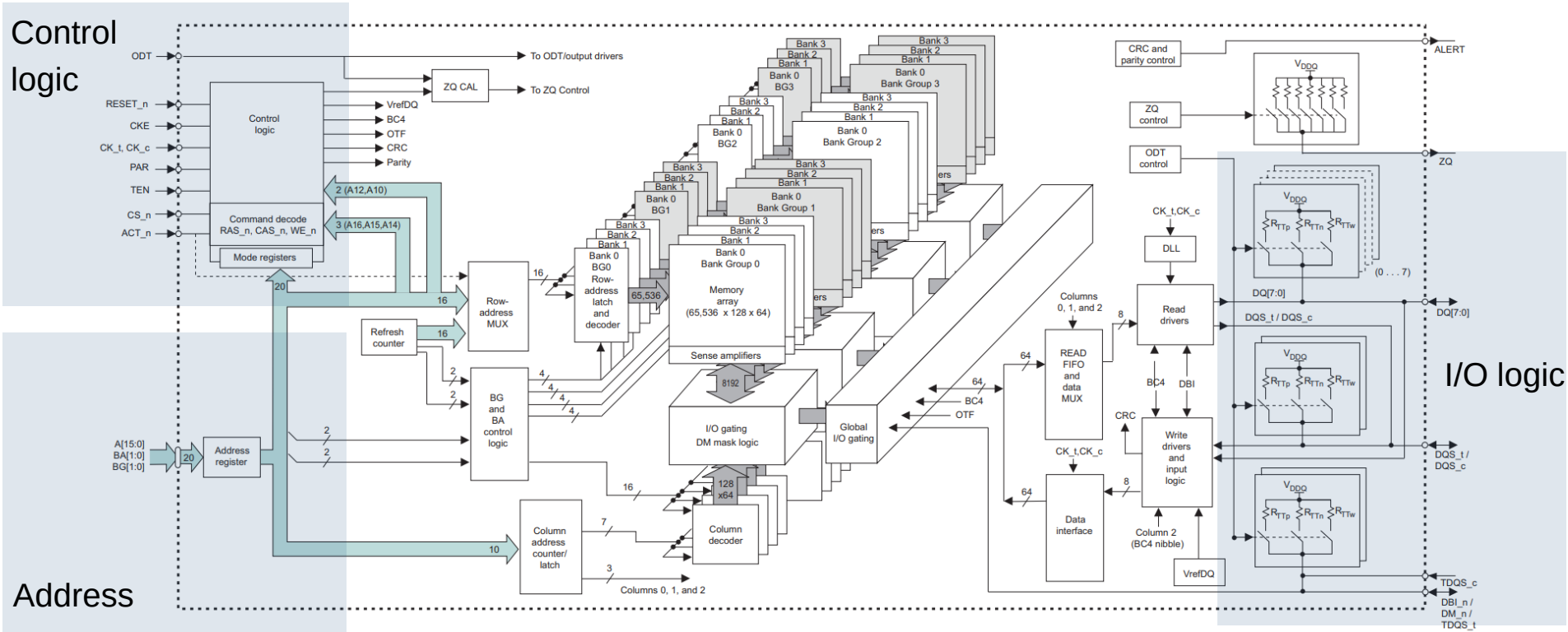
- **Memory bus**
  - Source-synchronous bus with single-ended DQ and CA (X-talk, etc.)
  - Multidrop bus with connects several DIMMs in parallel (trade density vs. speed)
  - High load on CA bus (connects all DRAMs on a DIMM)
- **PCB board design**
  - Transmission lines
  - Power supply
  - Reference clock
  - Isolation from other IPs

The transmission rate doubles from generation to generation.

The voltage level and margins reduce from generation to generation.

(LP)DDR5 DETAILS

DDR SIGNALS
FUNCTIONAL BLOCK DIAGRAM



source: Micron – 8gb_ddr4_sdram

COMMAND TRUTH TABLE DDR5

Source: JESD79- 5C

- All SDRAM commands are defined by states of command bus
- Example DDR5:
  - Signals are either command or address depending on ACT_n
  - Actived at the rising edge of the clock
  - ***For Debugging Read / Write Separation CS and CA4 are very useful***

Table 30 — Command Truth Table

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Activate	ACT	L	L	L	R0	R1	R2	R3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11, 17, 20
		H	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	CID3/ R17	
RFU	RFU	L	H	L	L	L	L	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
RFU	RFU	L	H	L	L	L	H	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Write Pattern	WRP	L	H	L	L	H	L	H	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11, 15, 18,19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	H	H	V	CID3	
Write Pattern w/ Auto Precharge	WRPA	L	H	L	L	H	L	H	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11, 15, 18,19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V or DRFM=L	AP=L	H	V	CID3	
RFU	RFU	L	H	L	L	H	H	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Mode Register Write	MRW	L	H	L	H	L	L	MRA0	MRA1	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V	8, 11, 13, 20
		H	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	V	CW	V	V	V	
Mode Register Read	MRR	L	H	L	H	L	H	MRA0	MRA1	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V	8, 13, 21, 20
		H	L	L	V	V	V	V	V	V	V	V	CW	V	V	V	
Write	WR	L	H	L	H	H	L	BL=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8, 12, 15, 19, 20
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	H	WR_ Partial=L	V	CID3	
Write w/Auto Precharge	WRA	L	H	L	H	H	L	BL=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8, 12, 15, 19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V or DRFM=L	AP=L	WR_ Partial=L	V	CID3	
Read	RD	L	H	L	H	H	H	BL=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8, 15, 19, 20
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	H	V	V	CID3	
Read w/Auto Precharge	RDA	L	H	L	H	H	H	BL=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8, 15, 19, 20
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V or DRFM=L	AP=L	V	V	CID3	
VrefCA Command	VrefCA	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	L	V	
VrefCS Command	VrefCS	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	H	V	
Refresh All	REFab	L	H	H	L	L	H	CID3	V	V	V or RIR	V or H	L	CID0	CID1	CID2	3, 23, 24

Write

Read

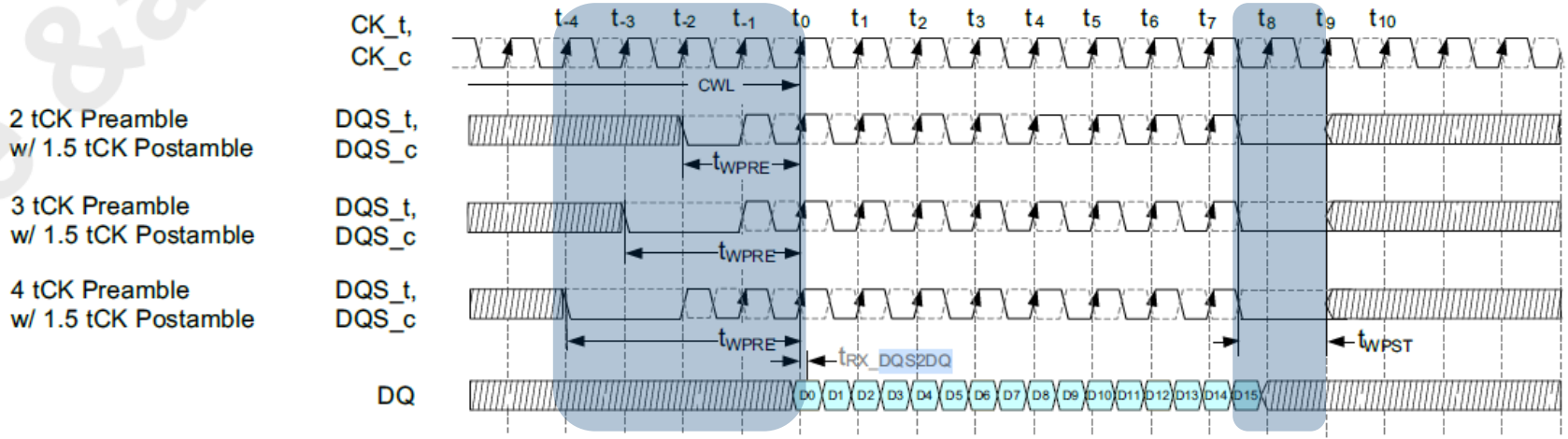
PRE-/ POSTAMBLE
TIMING VARIABLES - WRITE

- Write:
  - Preamble: 2/ 3/ 4 tCK
  - Postamble: 0.5 or 1.5 tCK
  - DQS clock tree delay: tRX_DQS2DQ

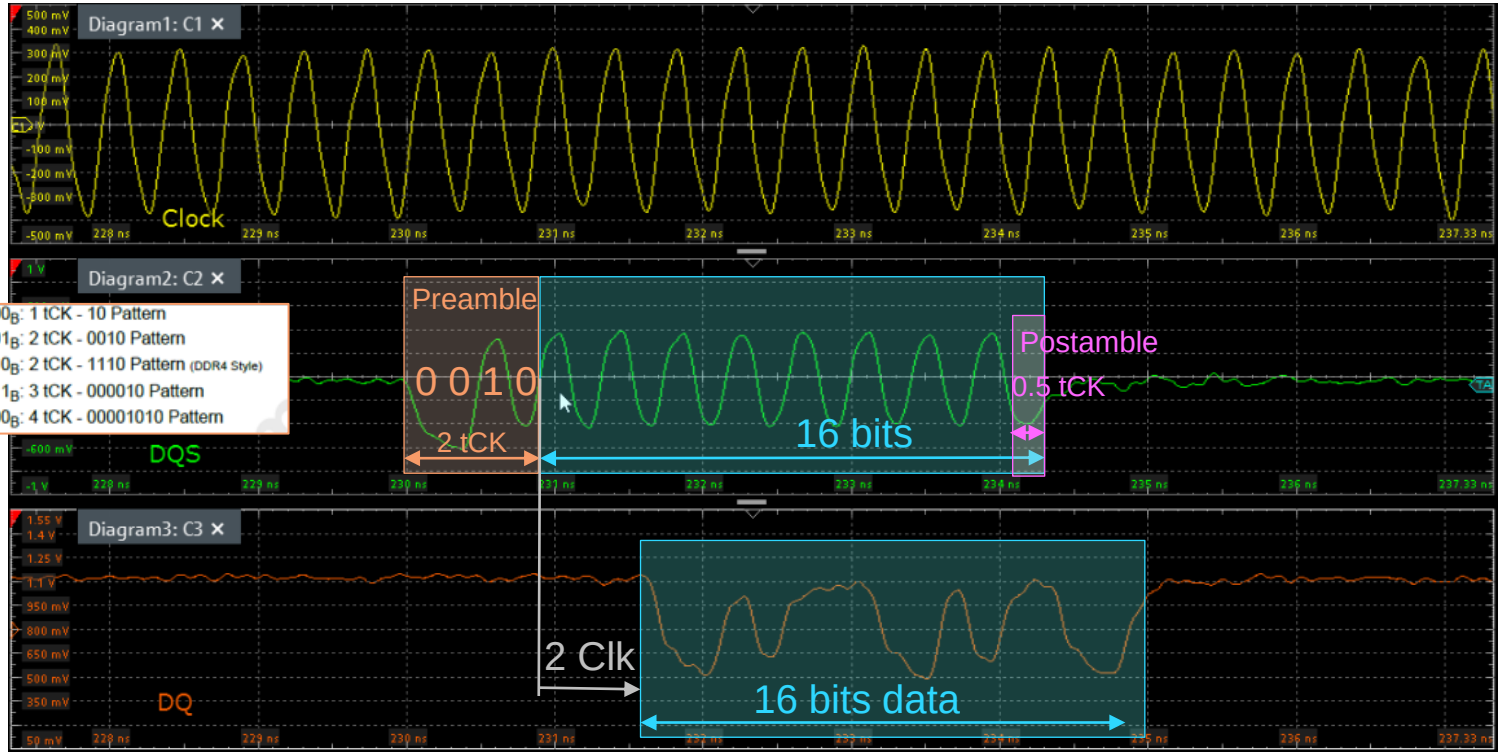
Table 146 — tRX_DQS2DQ Offset Due to Temperature and Voltage Variation for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS to DQ offset temperature variation	tRX_DQS2DQ_temp	-	12.75	-	11.34	-	10.20	-	9.28	-	8.50	ps/10°C	1,3
DQS to DQ offset voltage variation	tRX_DQS2DQ_volt	-	45.00	-	43.00	-	41.00	-	39.00	-	32.00	ps/ 50mV	2,3

NOTE 1 tRX_DQS2DQ max delay variation as a function of temperature
NOTE 2 tRX_DQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD. It includes the VDDQ and VDD AC noise impact for frequencies >20MHz and max voltage of 45mVpk-pk from DC -20MHz at a fixed temperature on the package. For tester measurement VDDQ=VDD is assumed
NOTE 3 Absolute value of DQS to DQ offset

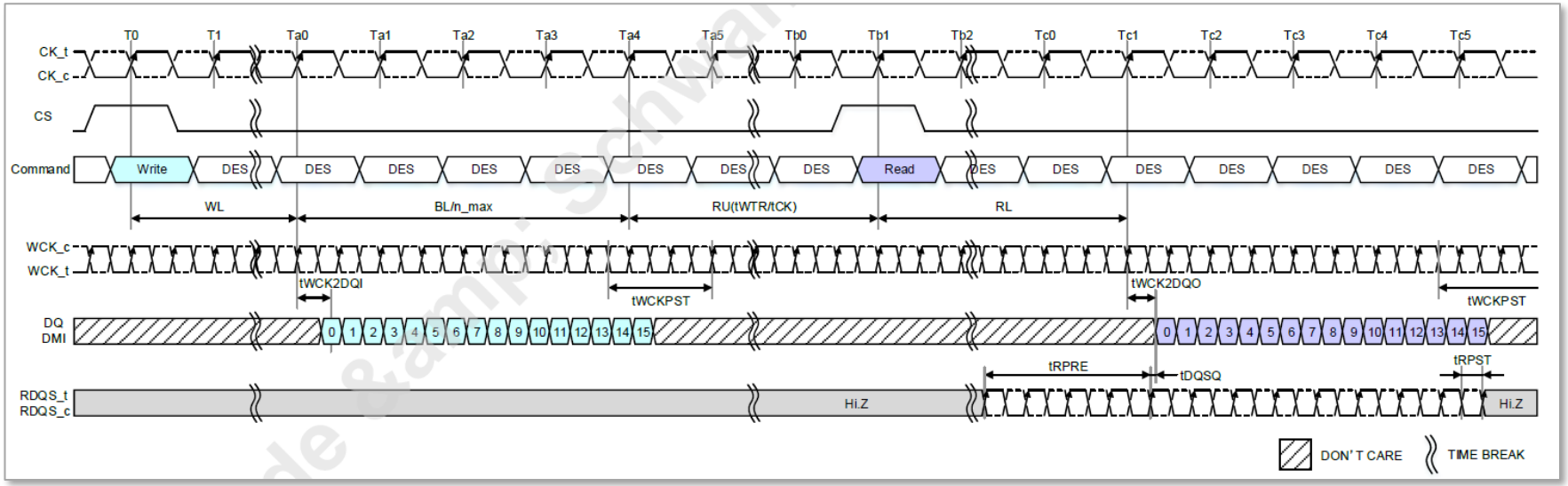


DDR5-4800 SINGLE RANK UDIMM (CRUCIAL)
WRITE



LPDDR5 SIGNALS

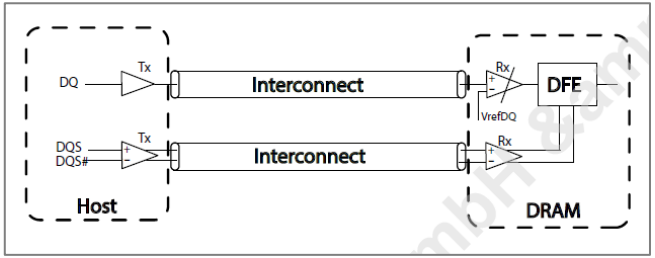
- **New**: Two forwarding **Strobe Clock signals:**
  - WCK: timing reference for WRITE data capture and READ data output
  - RDQS: is derived from WCK and timing reference for READ

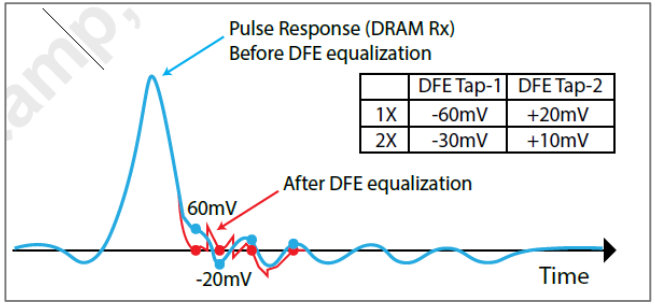


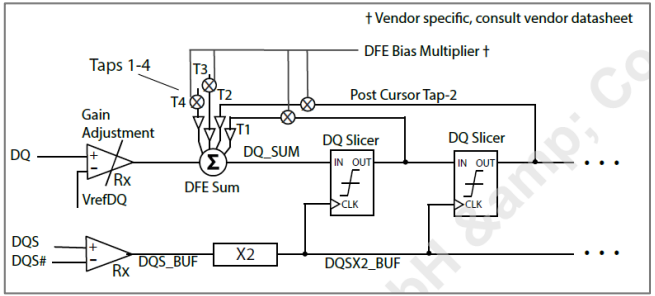
source: JESD209-5C

DFE

- ISI due to reflections is particular concern for DDR5
- 4-tap DFE for data rates >= 2933 MT/s
  - Gain amplifier
  - DFE summer
  - 4 DQ slicers (tabs) looping back to summer
- Mode Register to define DFE settings for memory controller
- Optimal settings are system dependent







CONTACTING THE DDR INTERFACE
VIAS, INTERPOSERS

- DDR JEDEC compliance focus on SDRAM chip and specifies measurement at package ball
- On single-sided DIMM or PCB, it is still possible to probe behind the package
- For design without access to back of PCB, interposer is required

- For interposers we refer to Nexus or EyeKnowHow

Contacting at the via

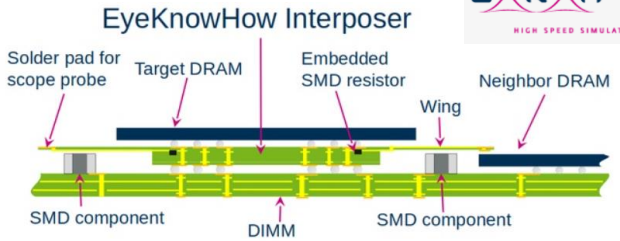
Interposer solution from EKH

NEXUS TECHNOLOGY

BGA Interposers

		Interposers				Options	
		Oscilloscope			MA51x0 Analyzer		
Package	Balls	EdgeProbe™	Direct Attach	Target Socketed	Logic Compliance	Riser	Component Socket
x4/x8	78/82	√(XH)	√(XH)	√(XH)	*	Yes	Yes
x16	102/106	√(XH)	√(XH)	√(XH)	*	Yes	Yes
RCD	240	*	√(XH)	*	*	Yes	No
Data Buffer	55	*	√(XH)	*	*	Yes	No

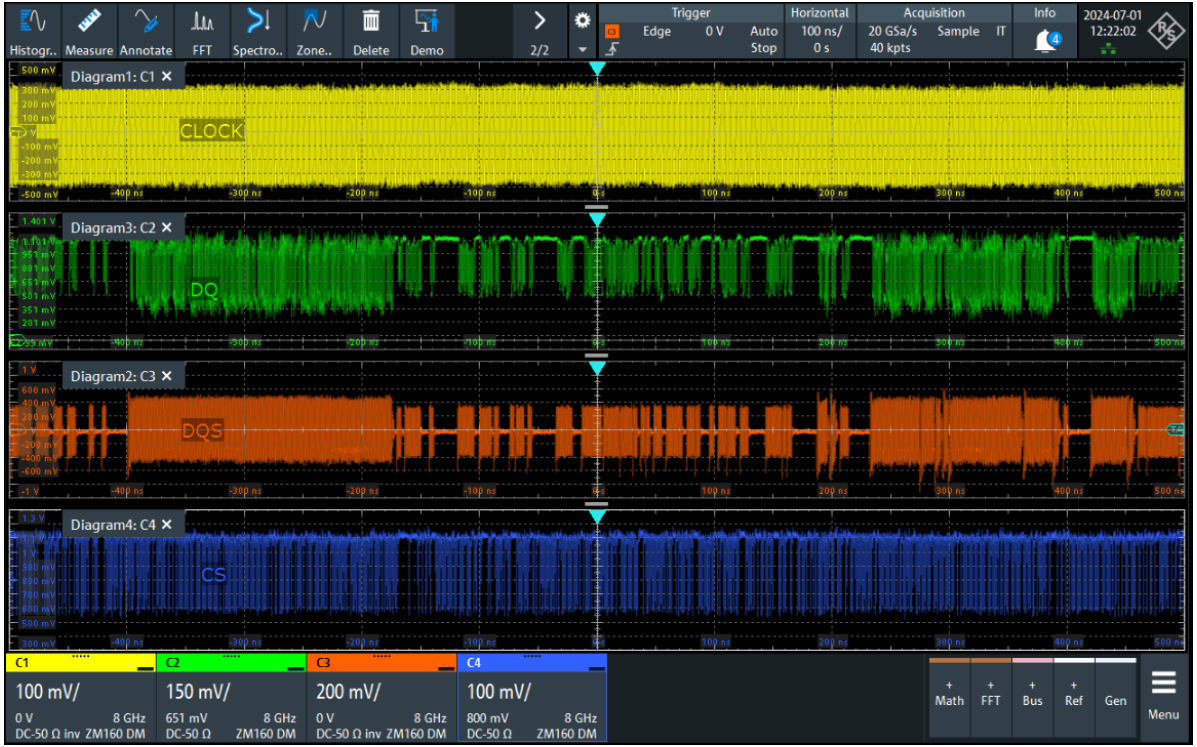
EXKH EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT



(LP)DDR5 SIGNAL INTEGRITY DEBUGGING
THE POWER OF THE ZONE TRIGGER

THE POWER OF ZONE TRIGGER

SIGNAL OVERVIEW



- Single Acquisition over a longer time scale (e.g. 1us)
- In the example an amplitude difference for different bursts at DQ and DQS is visble

THE POWER OF ZONE TRIGGER
PRE-/ POSTAMBLE

- The pre- and postamble depends on the data rate and system configuration.
- With the Zone trigger you easily can focus the acquisition on Read or Write bursts
- Focus on short bursts

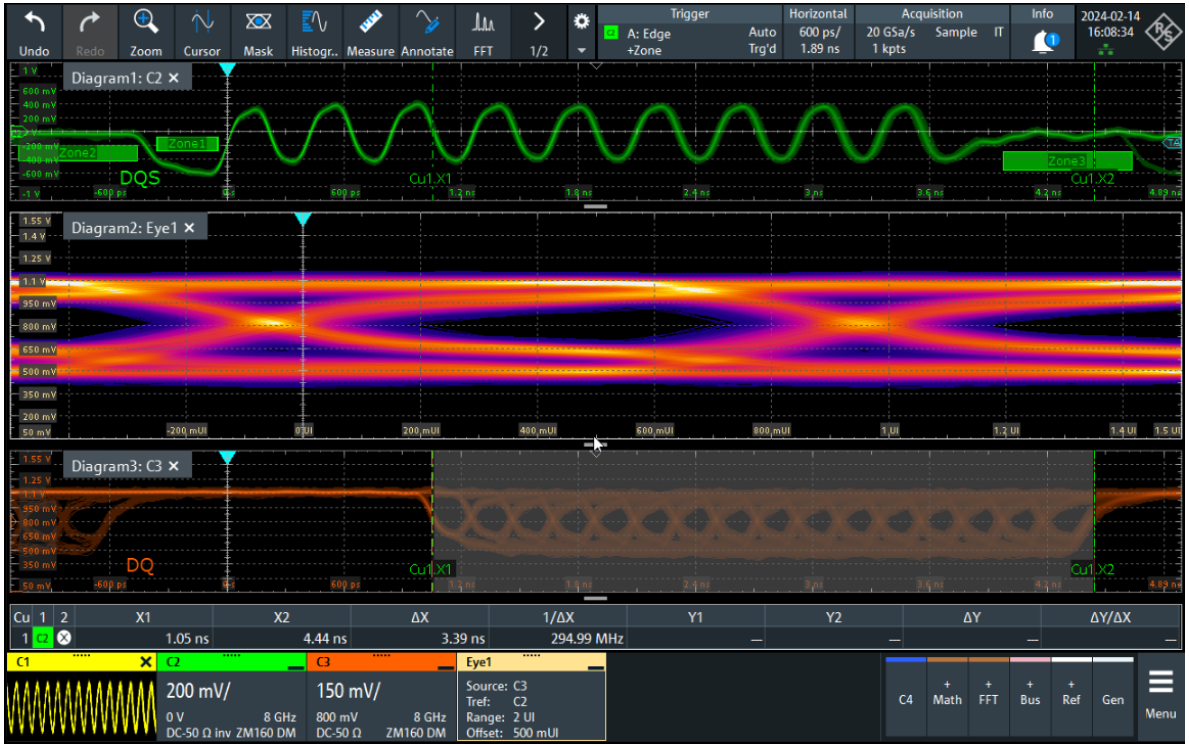
THE POWER OF ZONE TRIGGER
PRE-/ POSTAMBLE: WRITE

- **Preamble:**
  - Pattern 0010 – 2 tCK
- **Postamble:**
  - Pattern 0 – 0.5tCK

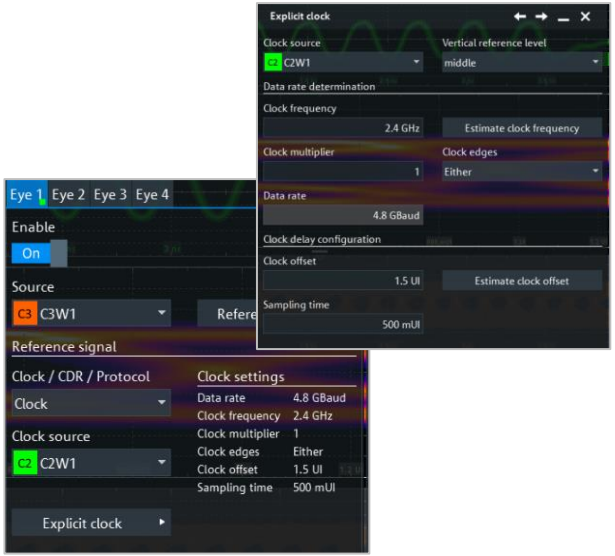
THE POWER OF ZONE TRIGGER
ISOLATING WRITES FOR DATA EYES

- Use Zone Trigger for Read/ Write burst separation and respective eye analysis

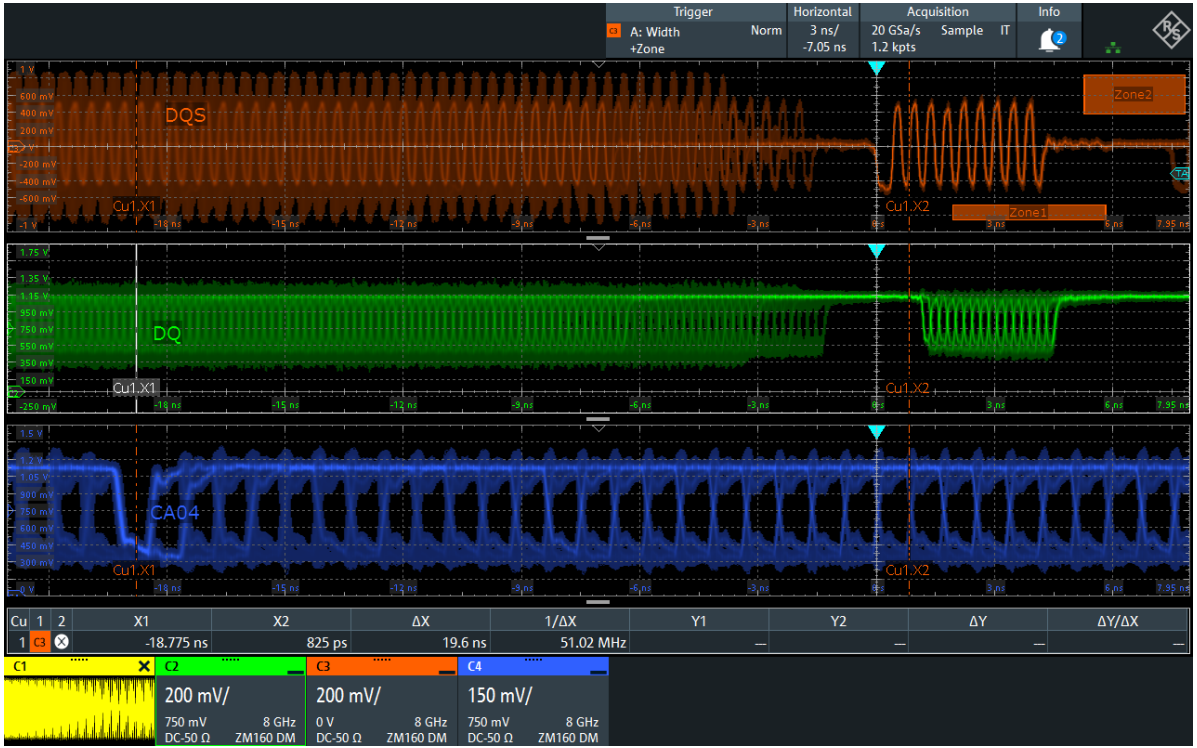
THE POWER OF ZONE TRIGGER
EYE DIAGRAM - WRITE BURSTS



- Gate focusing on the WRITE bursts
- Explicit clock with respective clock delay



THE POWER OF ZONE TRIGGER
VERIFY CL/CWL LATENCY

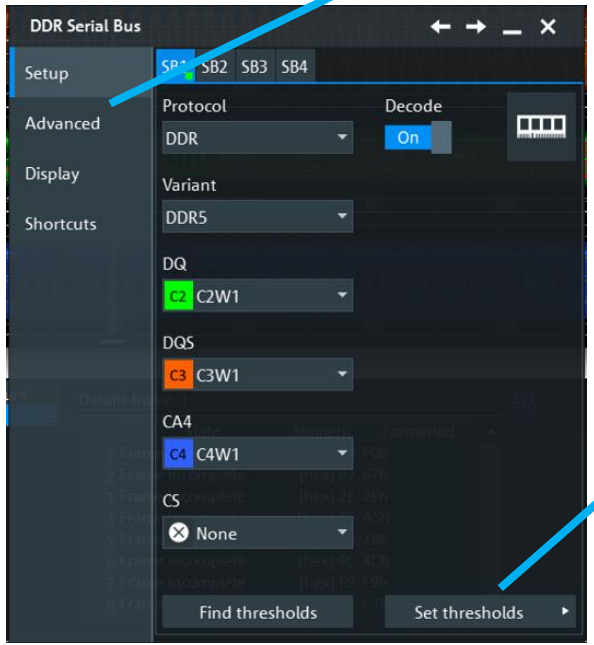


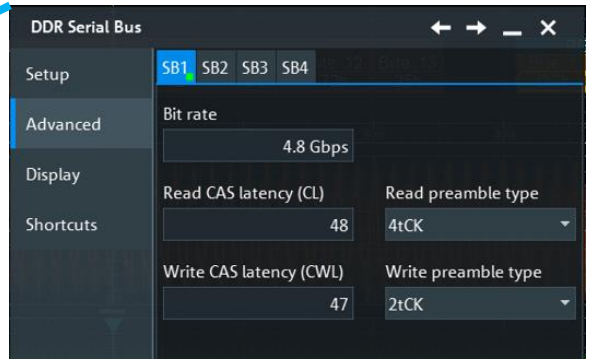
- Use Zone Trigger for R/W burst separation and respective eye analysis
- Apply “Persistence Mode”
- Measure Latency on CS and CA04

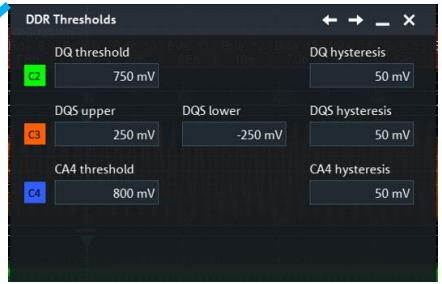
(LP)DDR5 SIGNAL INTEGRITY DEBUGGING
DDR PROTOCOL DECODE (READ/ WRITE)

PROTOCOL DECODE: READ/WRITE

- **DDR5 Decode:**
  - based on CL/CWL and Preamble
  - DQ, DQS, CA04
- **LPDDR5 Decode:**
  - Based on RDQS toggling
  - DQ, WCK, RDQS







PROTOCOL DECODE: READ/WRITE
DDR5-4800

- Read/ Write Decoding Example at 4800 Mbit/s

PROTOCOL DECODE: READ/WRITE

DDR5-4800

- Decode table

PROTOCOL DECODE: READ/WRITE
DDR5-4800

- Scaling in to Result details

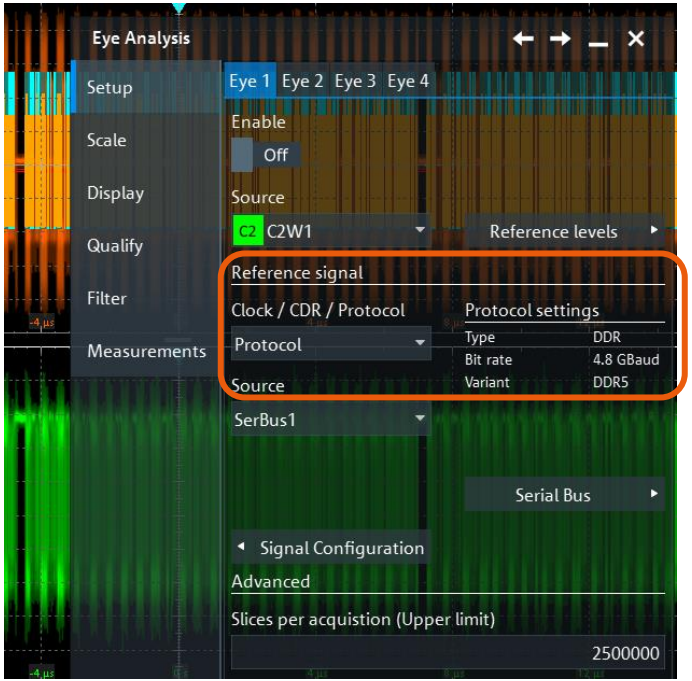
PROTOCOL DECODE: READ/WRITE
LPDDR5-4267

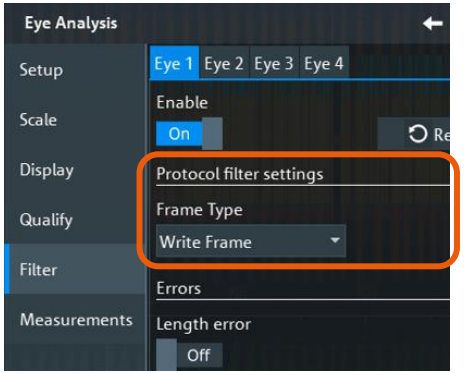
- Scaling in to Result details

(LP)DR5 SIGNAL INTEGRITY DEBUGGING
DDR EYE

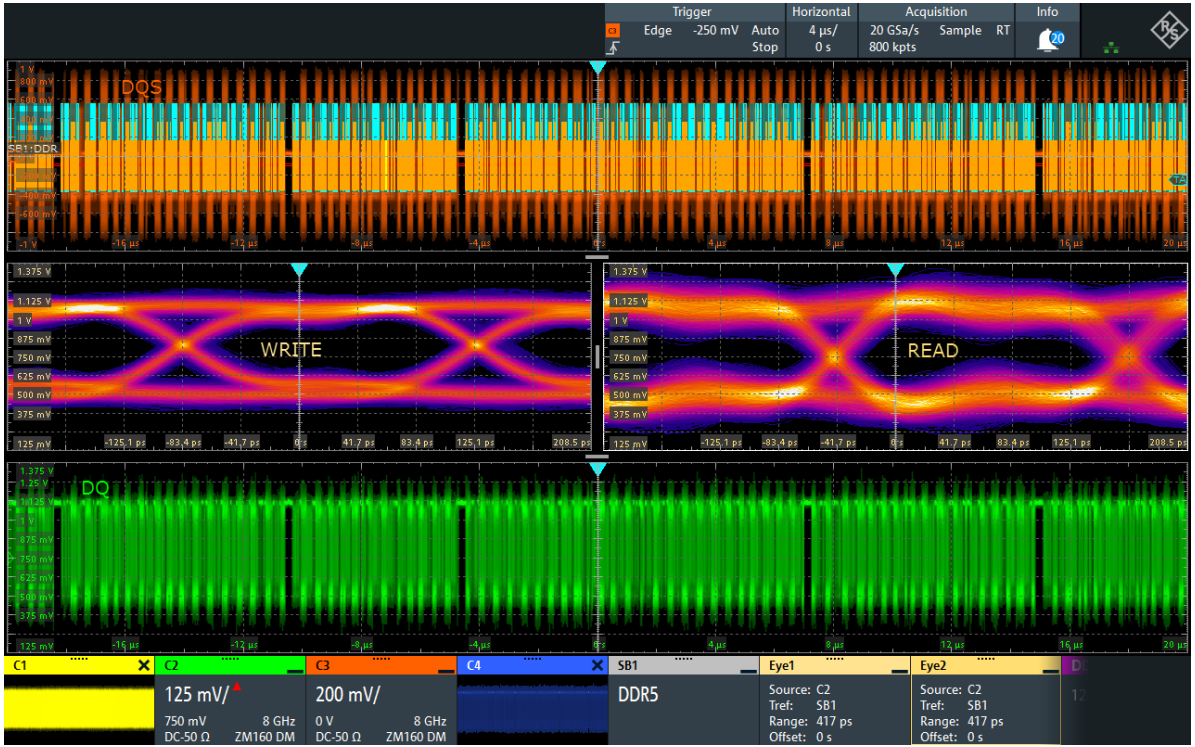
DATA EYE ANALYSIS
BASED ON DDR PROTOCOL DECODE

- **DDR Data Eye:**
  - DDR protocol as timing reference
  - Use the power of the Advanced Eye function
  - Filter to distinguish Read and Write Eyes



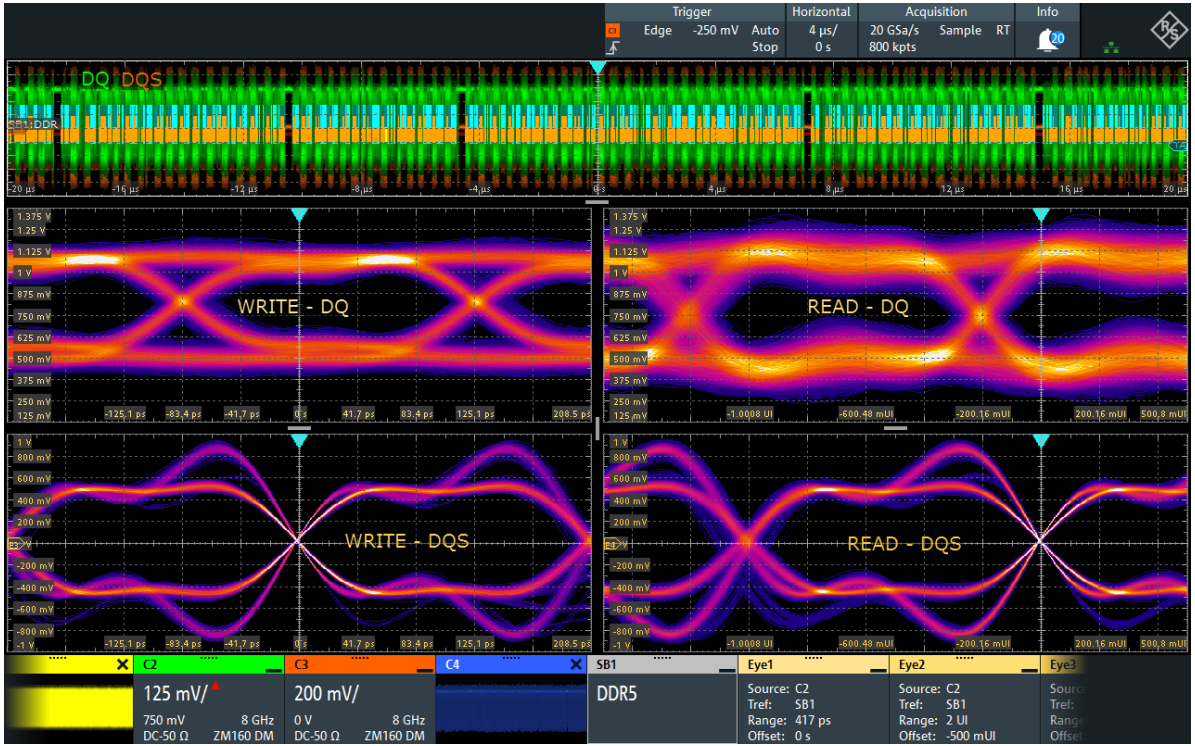


DATA EYE ANALYSIS
BASED ON DDR PROTOCOL DECODE: DDR5-4800



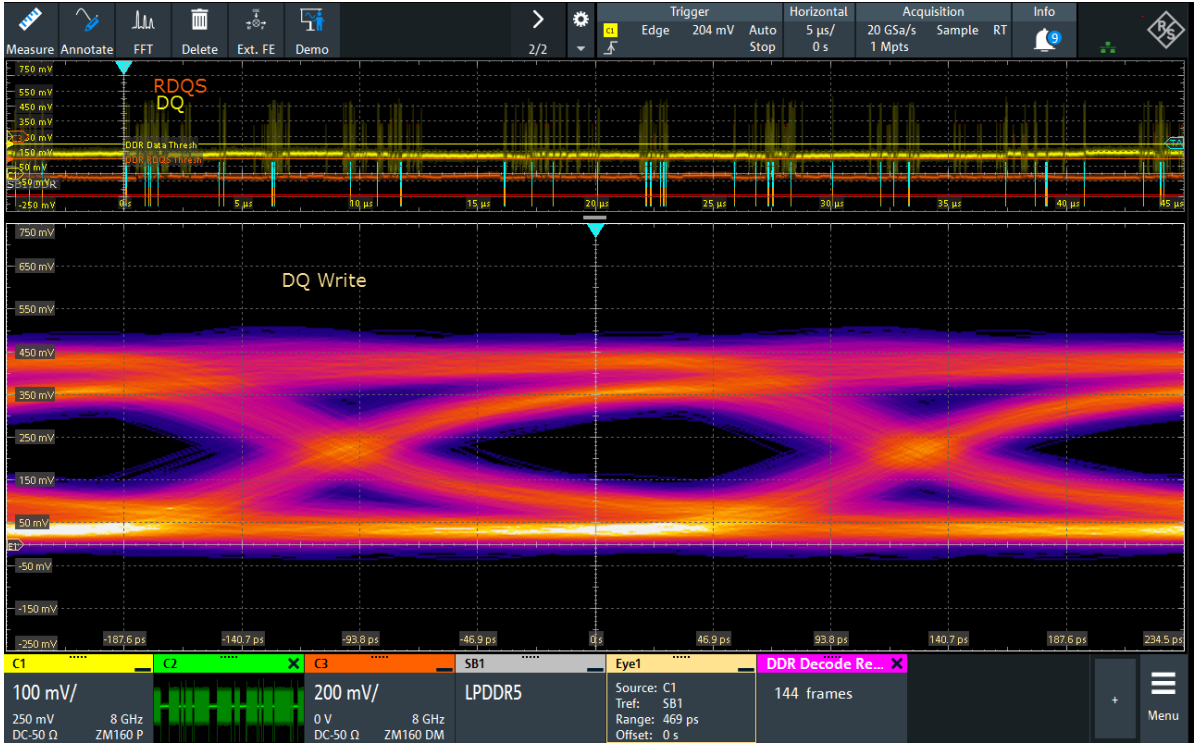
- READ & WRITE DQ data eyes

DATA EYE ANALYSIS
BASED ON DDR PROTOCOL DECODE: DDR5-4800



- READ & WRITE DQ data and DQS strobe clock eyes

DATA EYE ANALYSIS
BASED ON DDR PROTOCOL DECODE: LPDDR5-4267

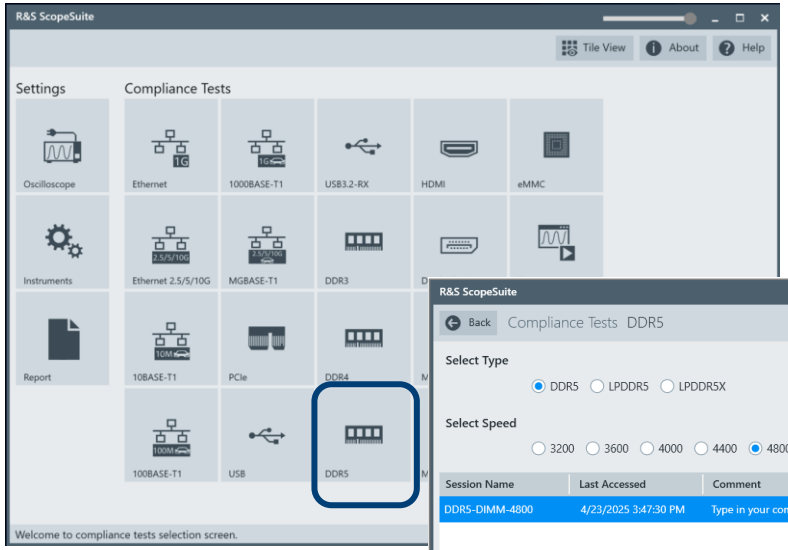


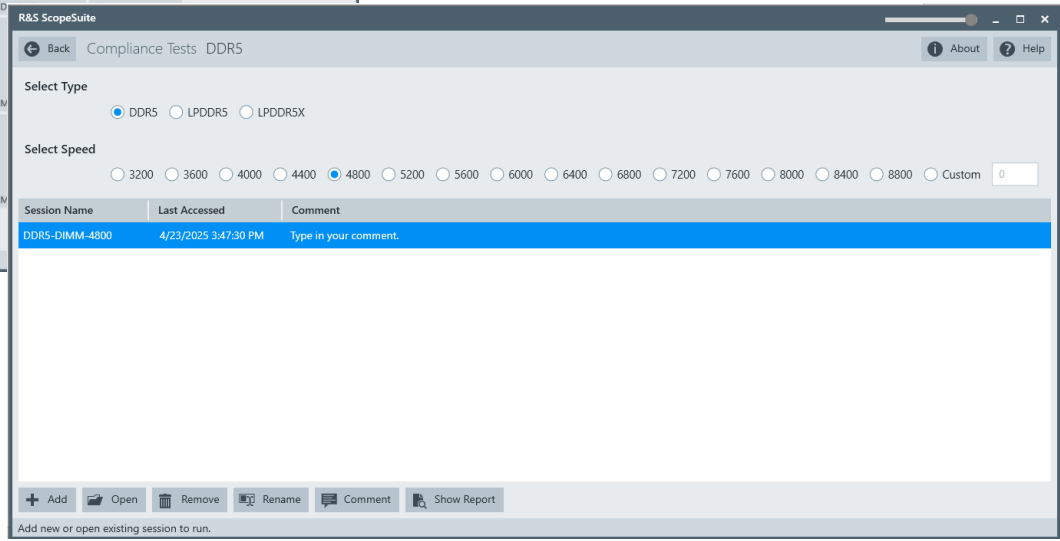
- WRITE DQ data

COMPLIANCE TESTING

DDR5 – SCOPESUITE

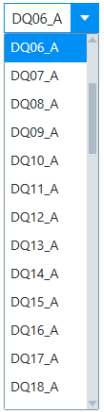
- **DDR5 Tile**
- **Select Type**
  - DDR5
  - LPDDR5
  - LPDDR5X
- **Select Speed:**
  - JEDEC speed grade or
  - Custom

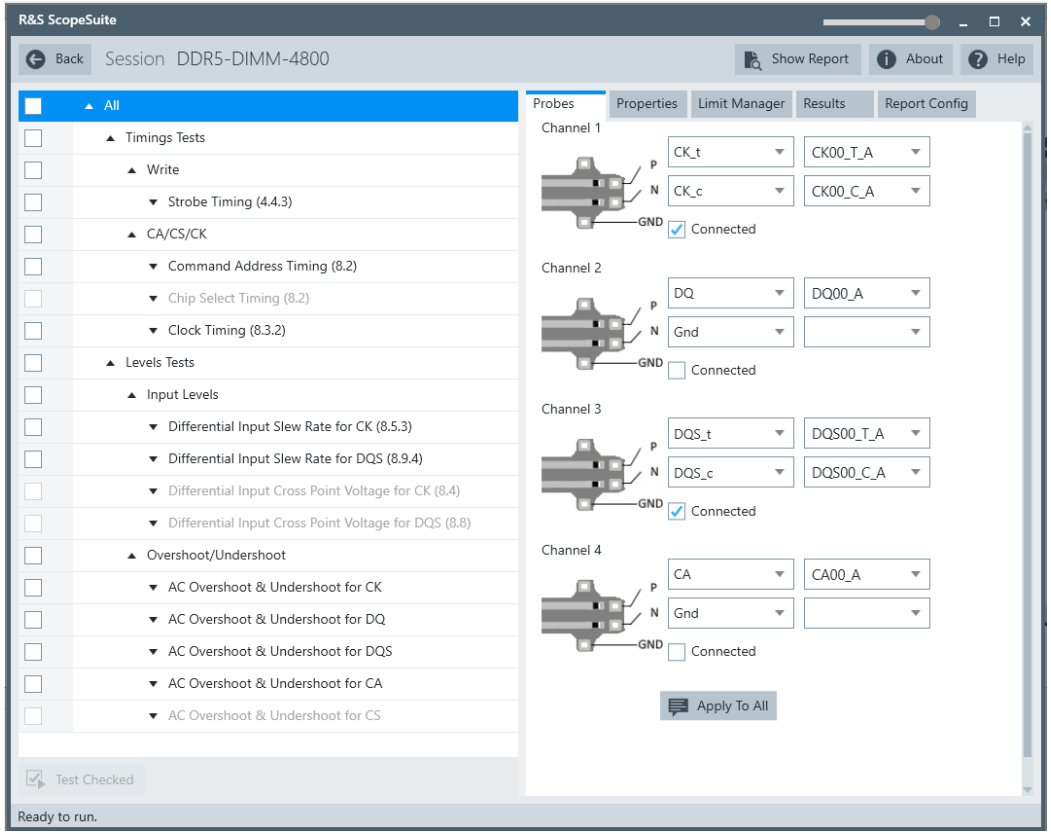




DDR5 – SCOPESUITE PROBE SETUP

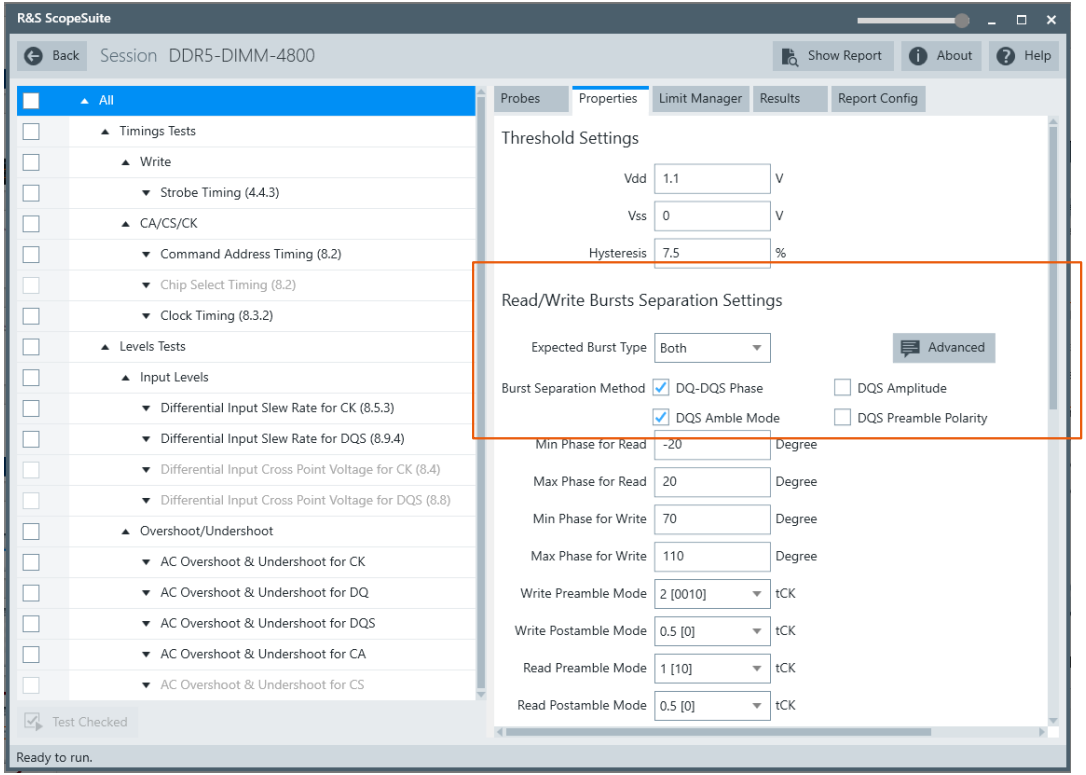
- New flexibility for Signal-to-Probe configuration:
  - use single-ended mode to connect to two DQ or CA signals
  - use diff mode for connecting to se signals
- Probe labels for
  - CLK, DQ, DQS, CS and CA signals





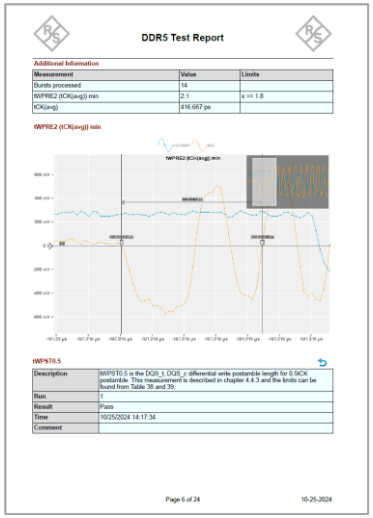
DDR5 – SCOPESUITE PROPERTIES

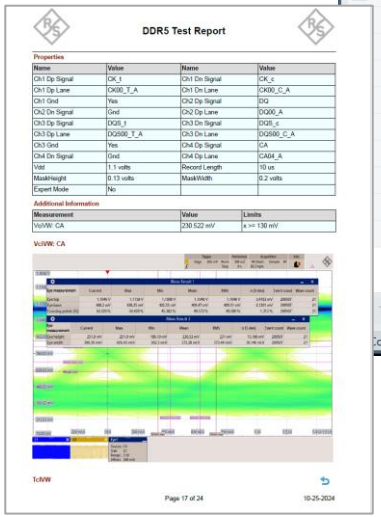
- Flexible Read / Write separation
  - DQ-DQS Phase
  - DQS Amplitude
  - DQS Preamble Pattern
  - DQS Preamble Polarity

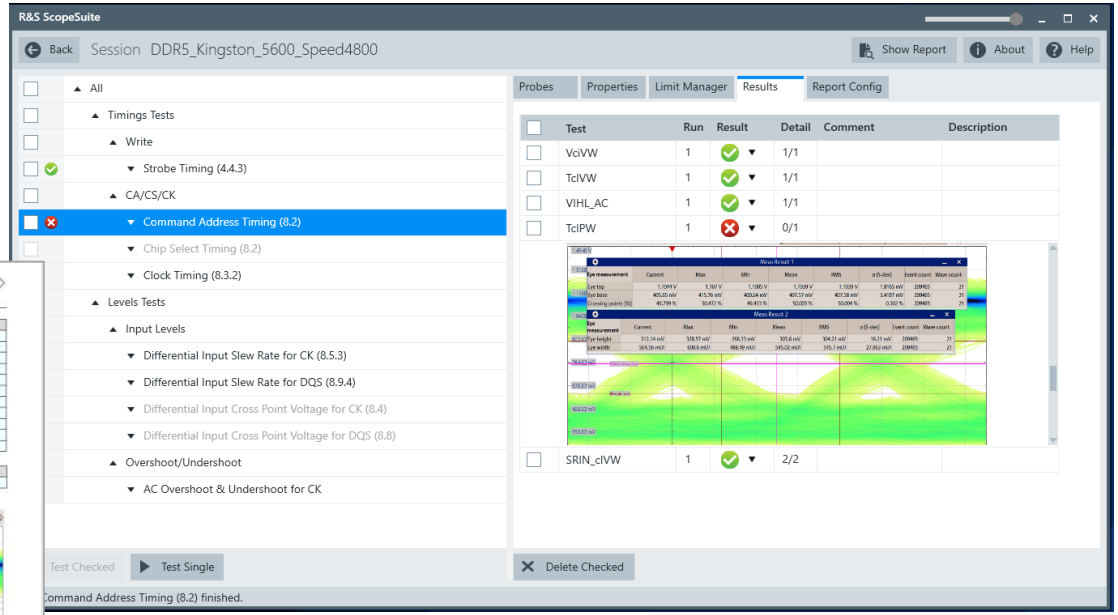


DDR5 – SCOPESUITE RESULTS DDR5-4800

- Results per test item within the ScopeSuite application
- Detailed Report







DDR5 Memory Interface - Signal Integrity Debugging & Compliance Testing

DEMO

SUMMARY

SUMMARY

- The need for memory continuously increases
- Data rates are increasing, voltage levels decreasing
- RTP’s 16 GHz covers DDR5
- The RTP can address SI debugging with Zone Trigger and Advanced Eye
- R&S addresses compliance testing with dedicated options for DDR5 and LPDDR5

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