Practical AC Analysis Methods for AC-DC Converters in Modern Data Centers

Prof. Katherine A. Kim
Electrical Engineering Department
National Taiwan University
November 17, 2025

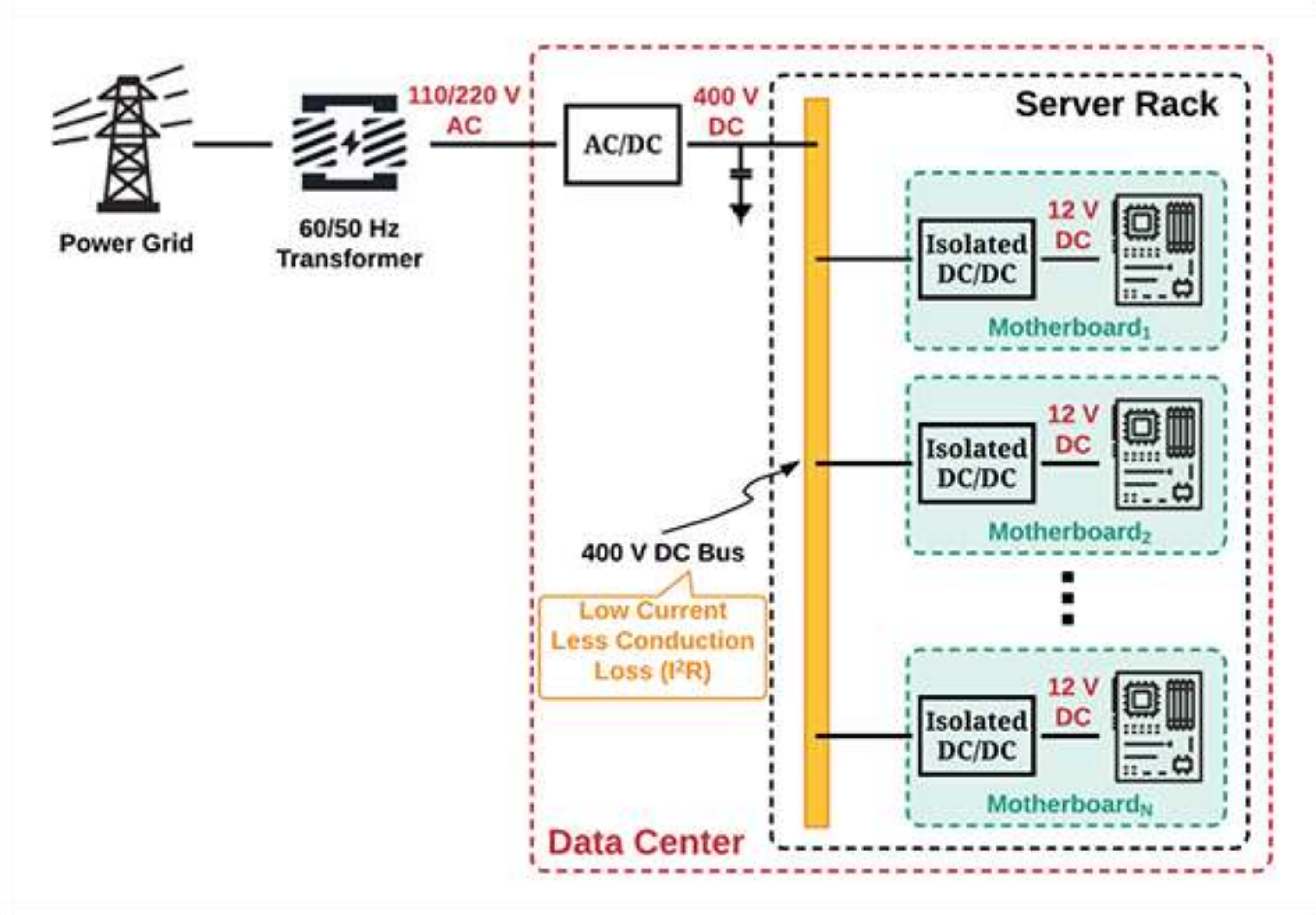
National Taiwan University
國立臺灣大學

PEARS
POWER ELECTRONICS FOR ADVANCED RENEWABLE SYSTEMS LAB

Outline

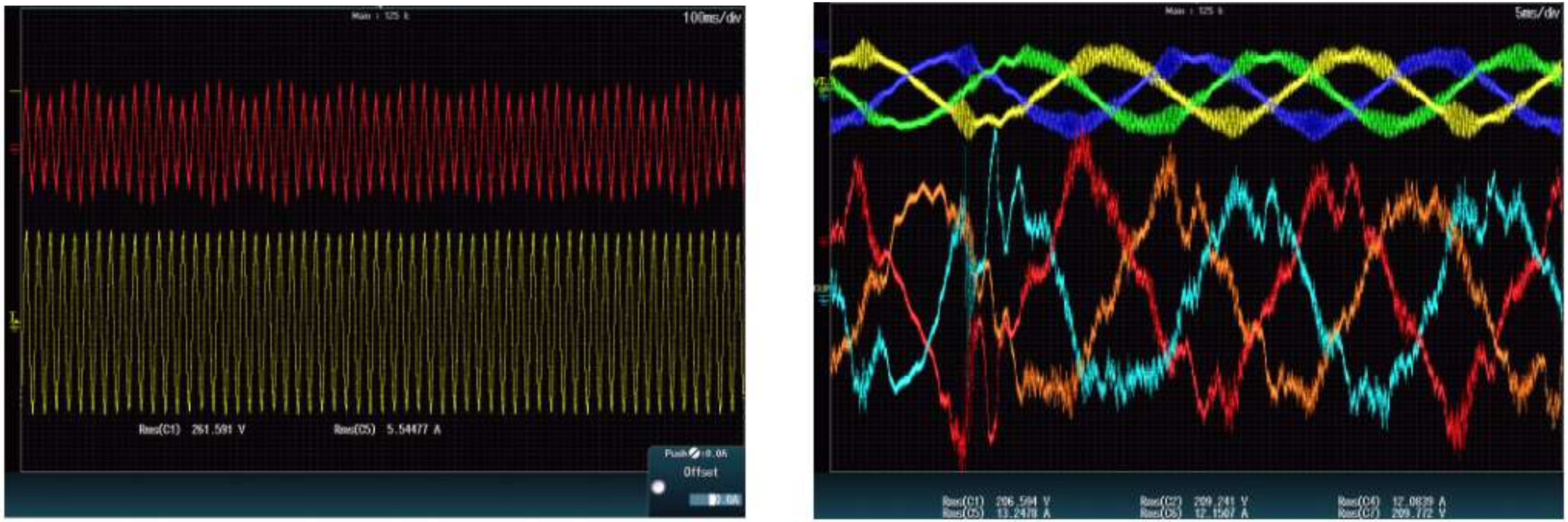
1. Data Centers Power Converter Architectures & Challenges
2. Power Factor Correction Basics
3. Modeling for DC-DC Converter Circuits
4. Modeling for PFC Circuits
5. Conclusion

Data Centers: Typical Power Converter Architecture



Source: https://khaligh.ece.umd.edu/portfolios/datacenter-power-electronics/

Data Centers: Instability Issue



(a) (b)

- Measured resonances in data center power systems: (a) low-frequency resonance and (b) high-frequency resonance
- Modeling impedance can help to reduce the resonance problems.

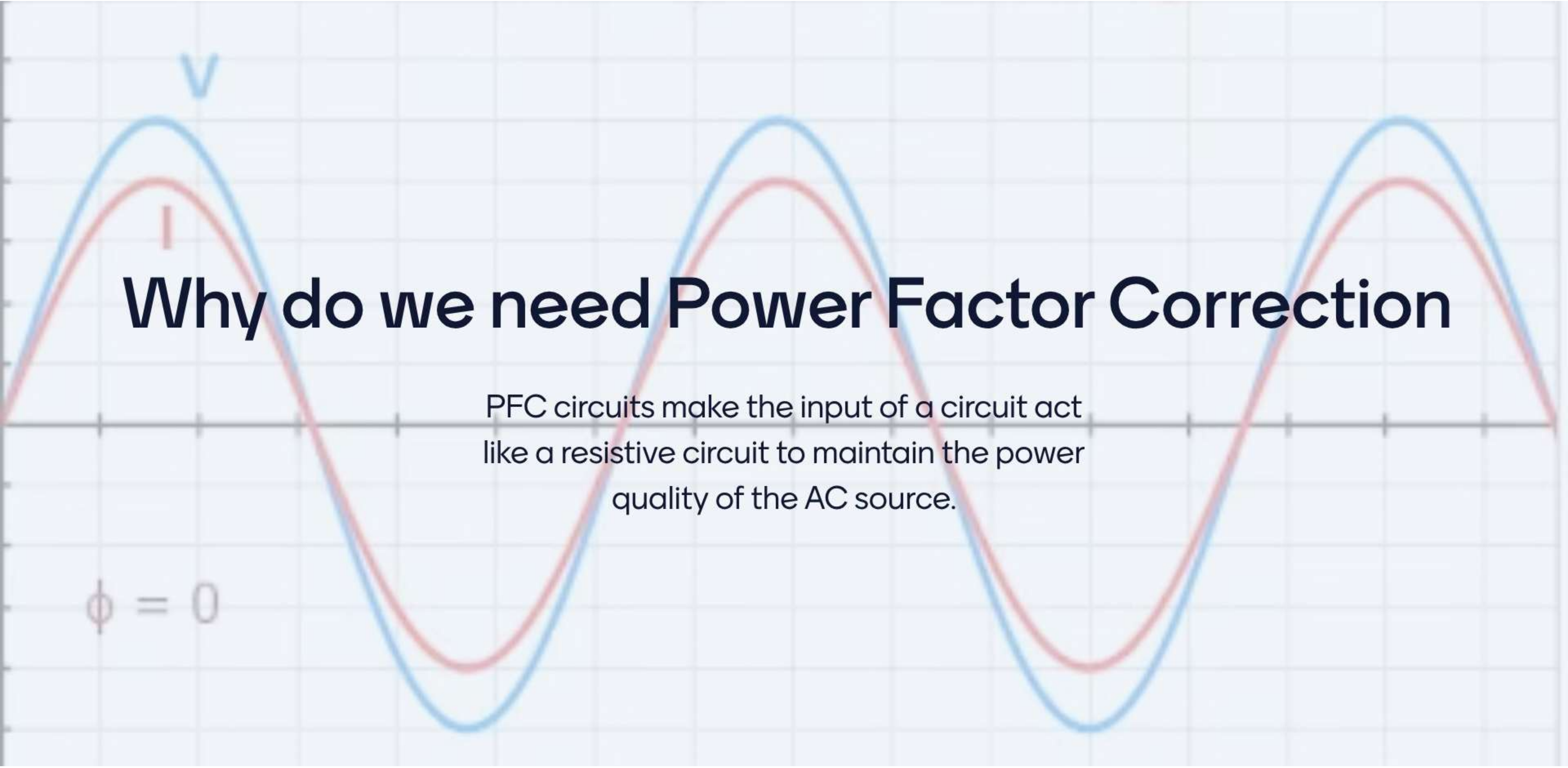
National Taiwan University 國立臺灣大學

Reference: J. Sun, M. Xu, M. Cespedes and M. Kauffman, "Data Center Power System Stability — Part I: Power Supply Impedance Modeling," in CSEE Journal of Power and Energy Systems, vol. 8, no. 2, pp. 403-419, March 2022.

PEARS LAB

Outline

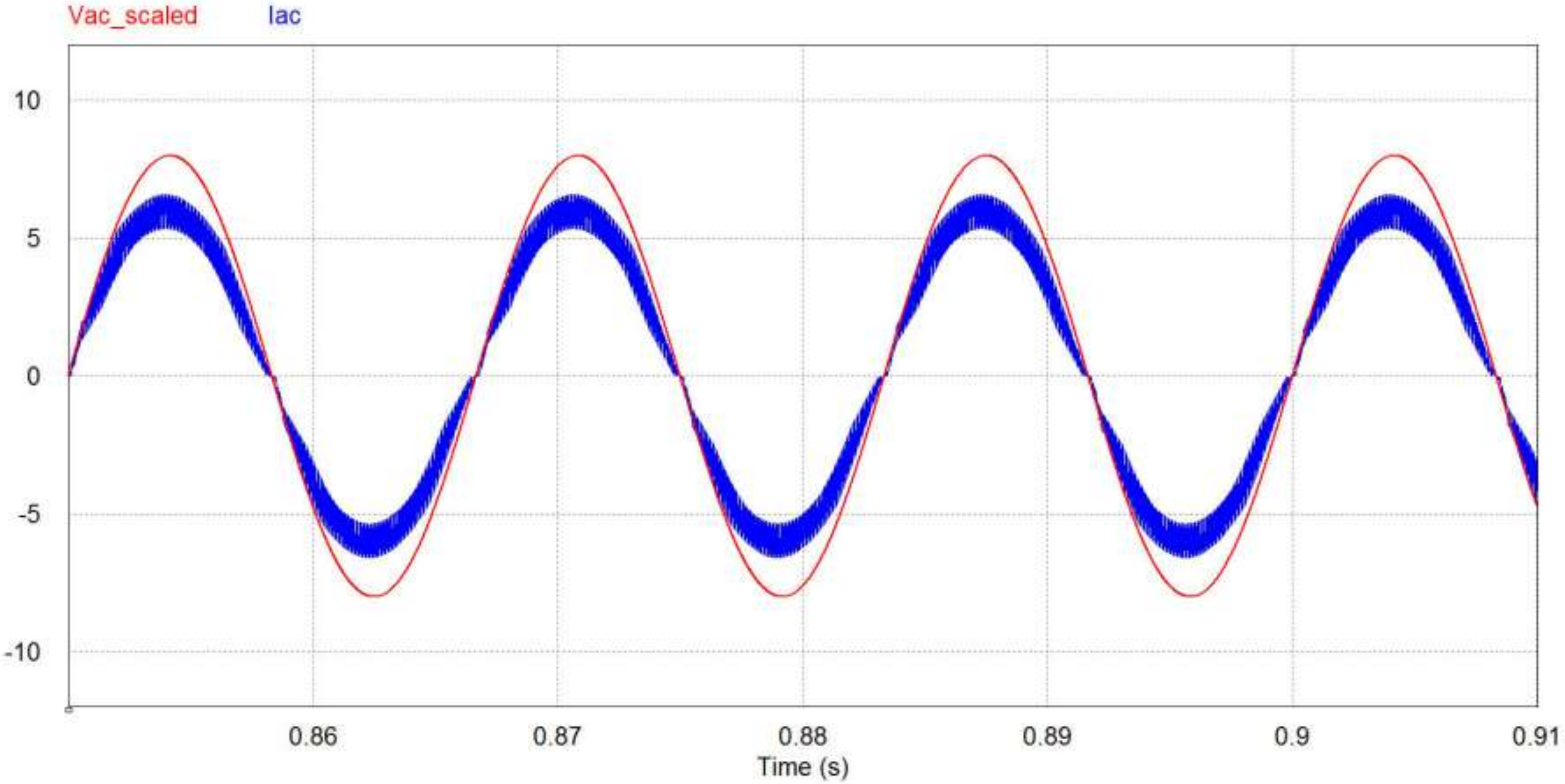
1. Data Centers Power Converter Architectures & Challenges
2. Power Factor Correction Basics
3. Modeling for DC-DC Converter Circuits
4. Modeling for PFC Circuits
5. Conclusion



Why do we need Power Factor Correction

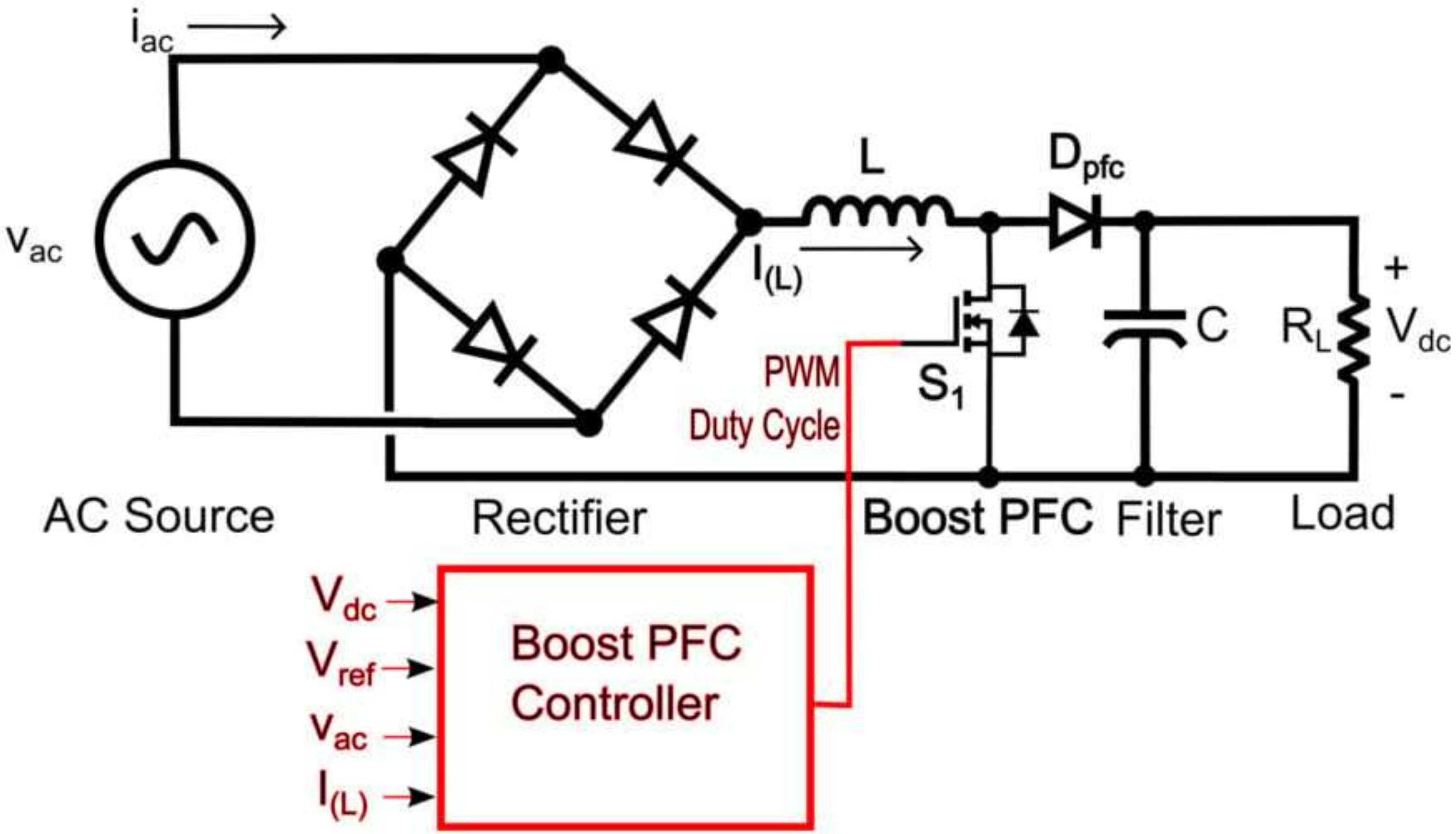
PFC circuits make the input of a circuit act like a resistive circuit to maintain the power quality of the AC source.

Desired PFC Input Waveforms



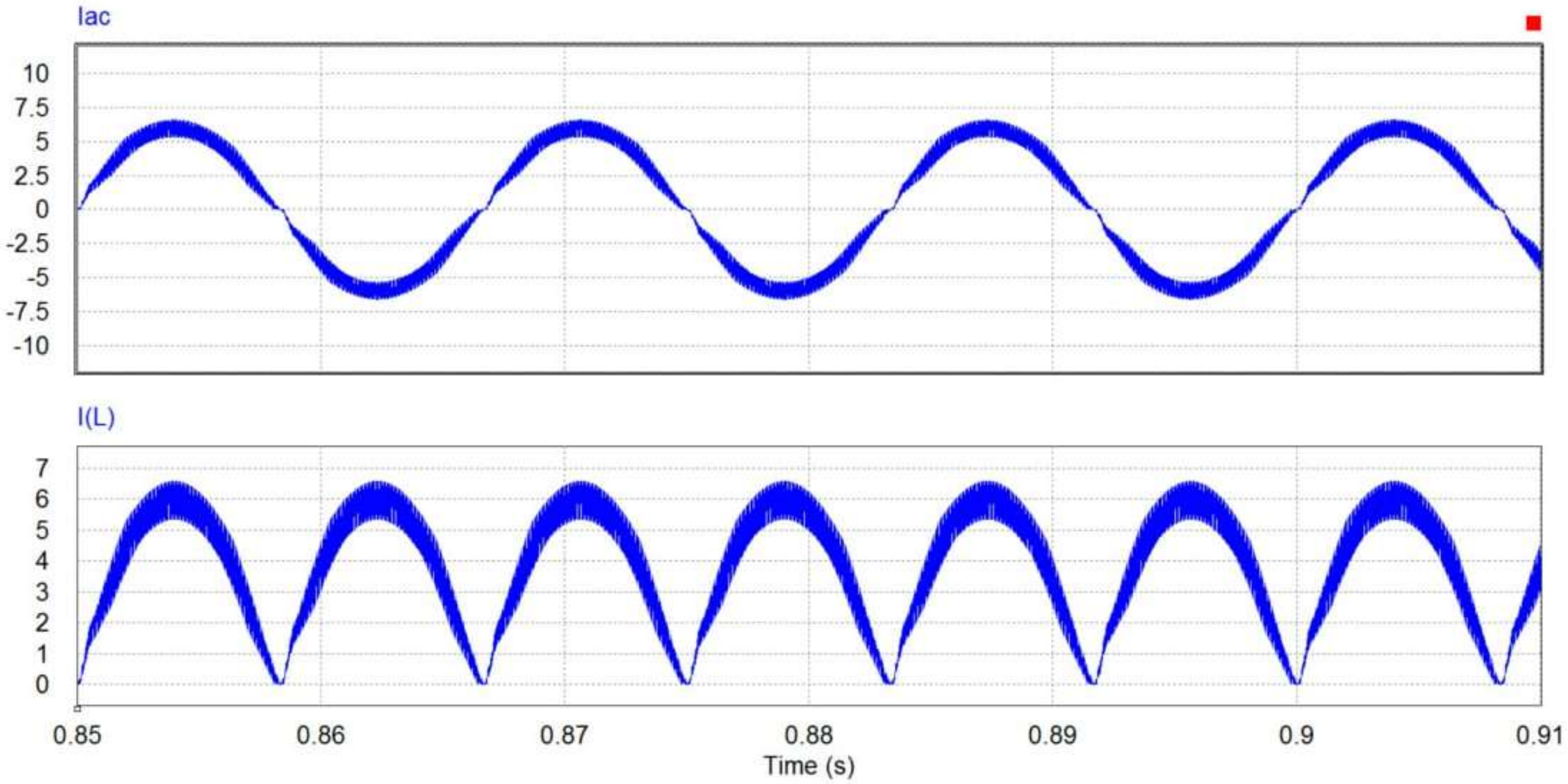
Source: https://www.allaboutcircuits.com/technical-articles/how-the-boost-pfc-converter-circuit-improves-power-quality/

Example PFC Boost Converter

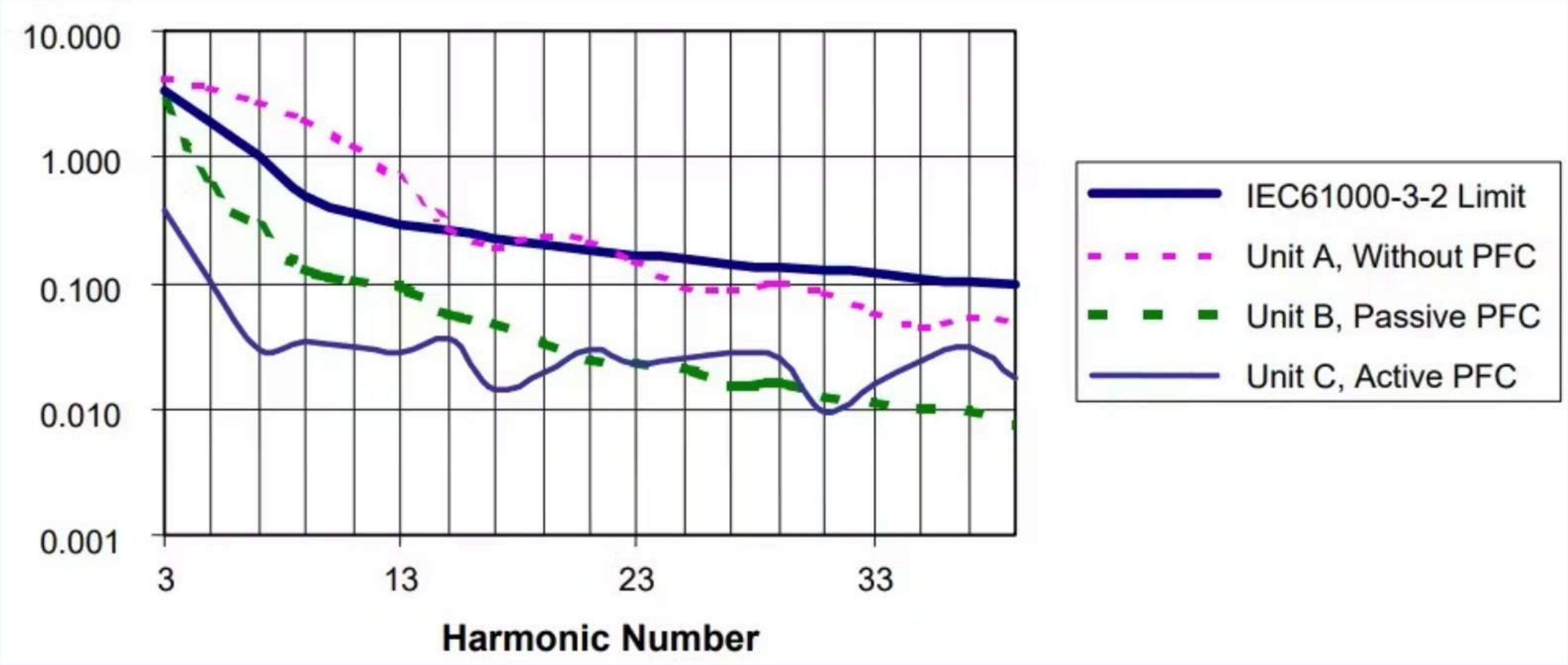


Source: https://www.allaboutcircuits.com/technical-articles/how-the-boost-pfc-converter-circuit-improves-power-quality/

PFC Input Current and Inductor Current Waveforms

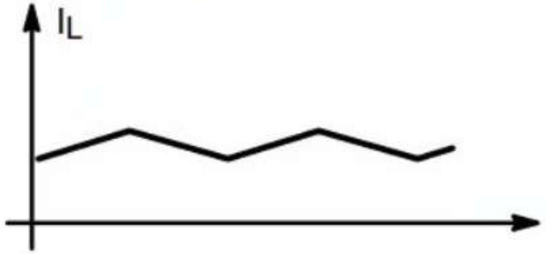
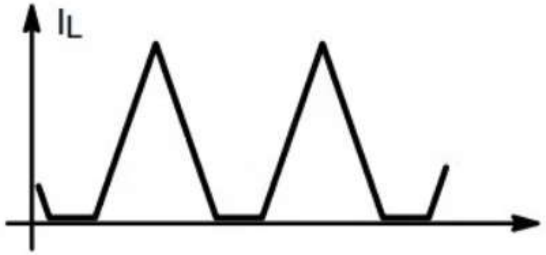
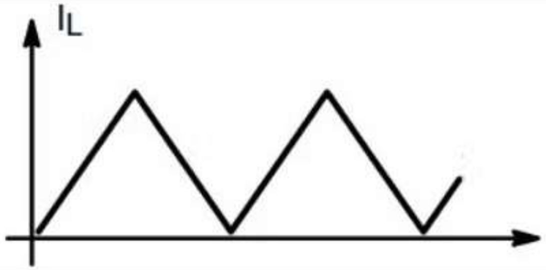


Source: https://www.allaboutcircuits.com/technical-articles/how-the-boost-pfc-converter-circuit-improves-power-quality/



Source: Power Factor Correction (PFC) Handbook, ON Semiconductor, Rev. 5, 2014

Harmonic Content with Different PFC Types

Rating	Symbol	Unit
	**C**ontinuous **C**onduction **M**ode (CCM)	• Always hard-switching • Inductor value is largest • Minimized rms current
	**D**iscontinuous **C**onduction **M**ode (DCM)	• Highest rms current • Reduce coil inductance • Best stability
	**Cr**itical **C**onduction **M**ode (CrM)	• Largest rms current • Switching frequency is not fixed

Source: Power Factor Correction (PFC) Handbook, ON Semiconductor, Rev. 5, 2014

Converter Conduction Modes

Outline

1. Data Centers Power Converter Architectures & Challenges
2. Power Factor Correction Basics
3. Modeling for DC-DC Converter Circuits
4. Modeling for PFC Circuits
5. Conclusion

Why do we need to model converters using small-signal analysis?

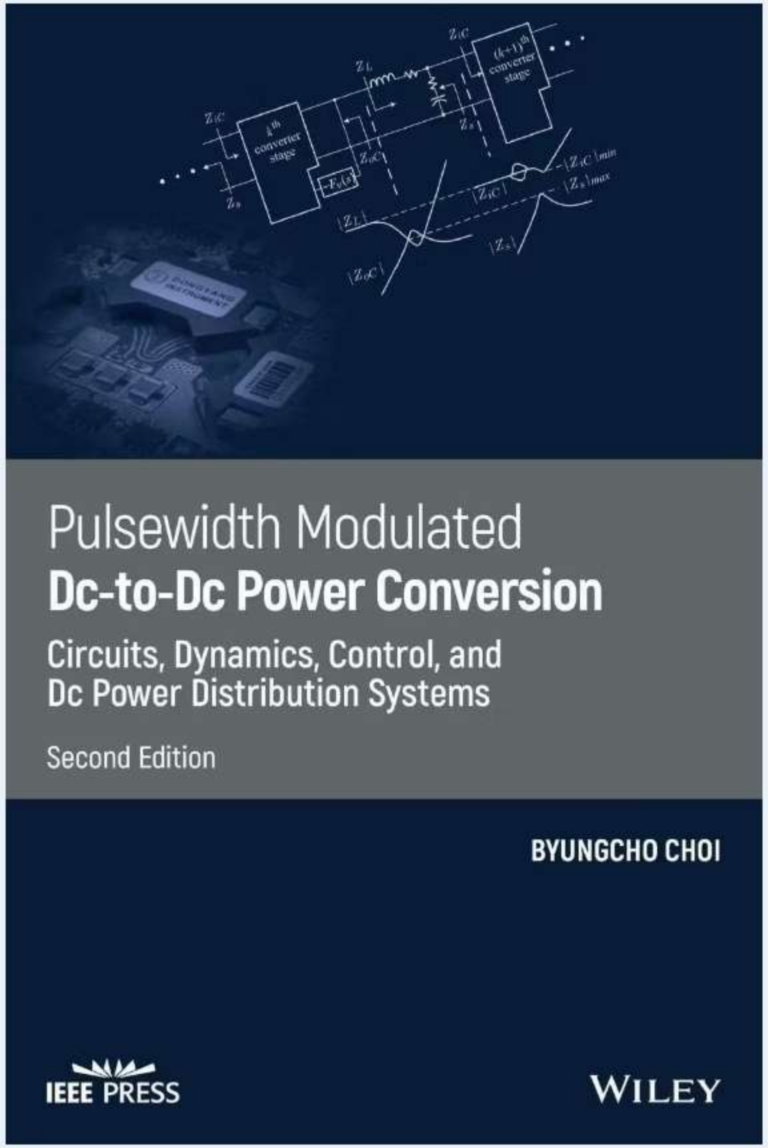
- Control:
  Understand the stability and dynamics of the control loop

- Output Impedance:
  Understand the interactions with the load

- Input Impedance:
  Ensure the interactions with the source will be stable

Let's model a converter

- What is the modeling process?
- Reference: Pulsewidth Modulated DC-to-DC Power Conversion by Dr. Byungcho Choi



Source: Byungcho Choi, Pulsewidth Modulated Dc-to-DC Power Conversion. Wiley IEEE Press, 2nd Edition.

Converter System Block Diagram

inputs

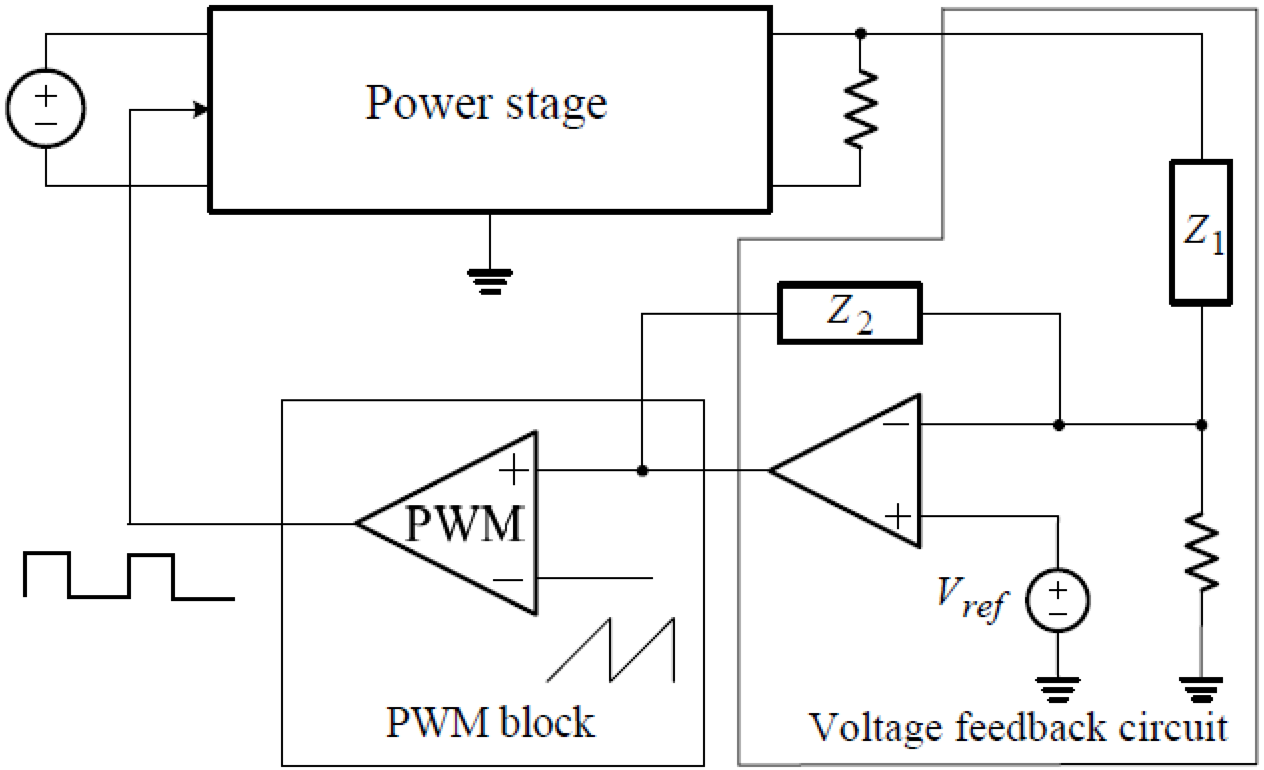
input voltage
*duty ratio
input current

DC-DC Converter

outputs

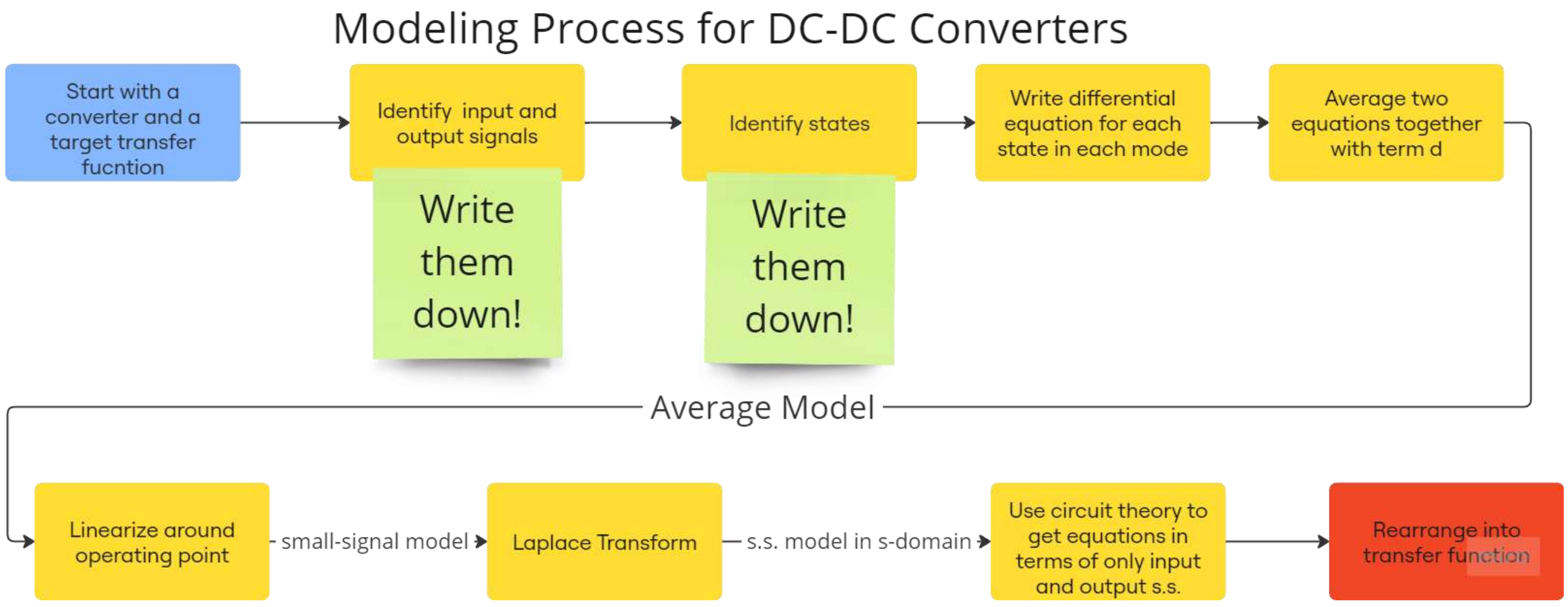
*output voltage
input voltage
input current

Example Power Converter with Feedback Control



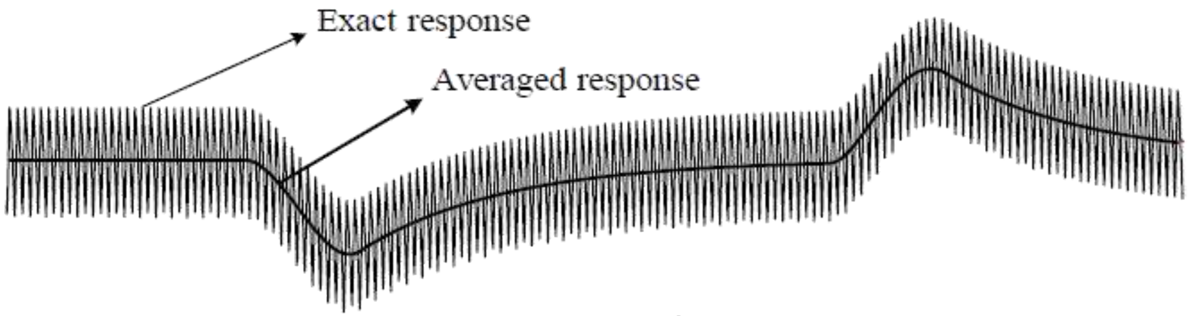
Source: Byungcho Choi, Pulsewidth Modulated Dc-to-Dc Power Conversion. Wiley IEEE Press, 2nd Edition.

Conventional Modeling Process

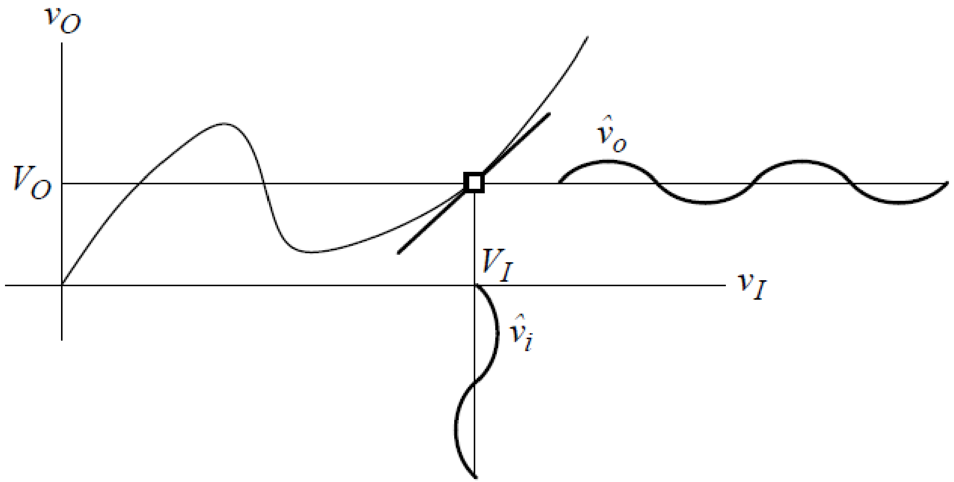


Two Essential Steps of Power Stage Modeling

- **Averaging** to remove the time-invariant from power stage dynamics

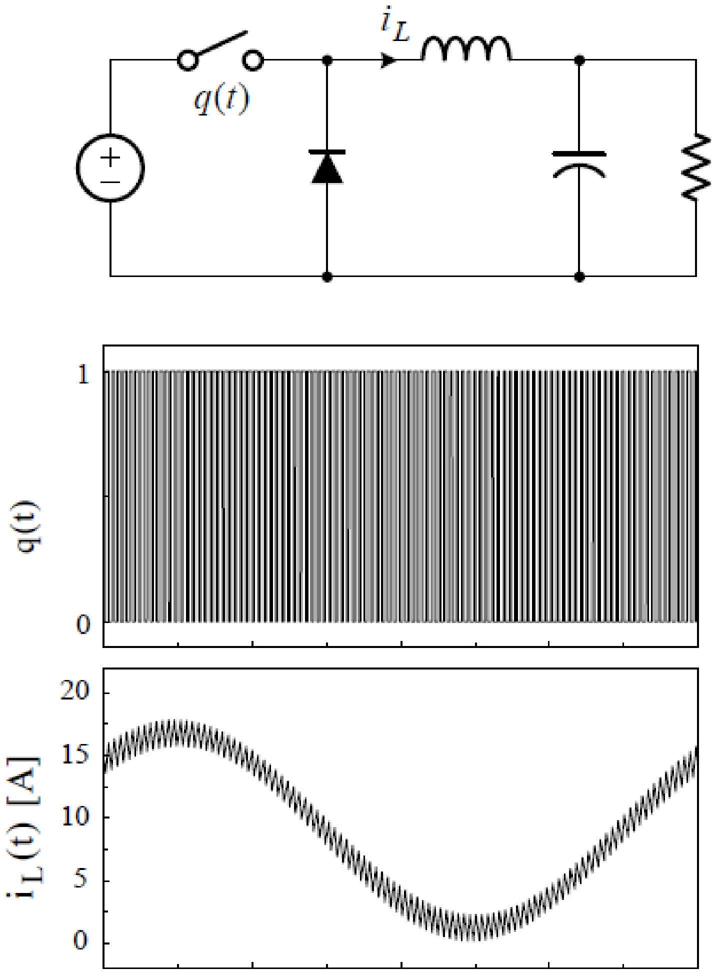


- **Linearization** to approximate a nonlinear function into a linear relationship under small-signal assumption

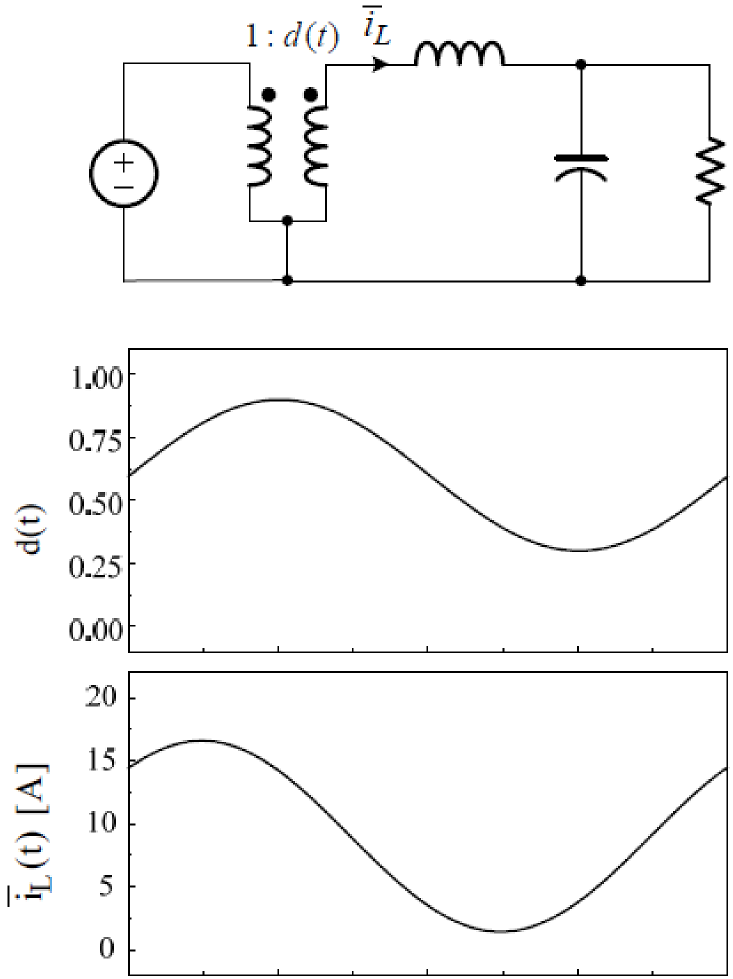


Source: Byungcho Choi, Pulsewidth Modulated Dc-to-DC Power Conversion. Wiley IEEE Press, 2nd Edition.

Steady-State Response of Switch Model and Average Model



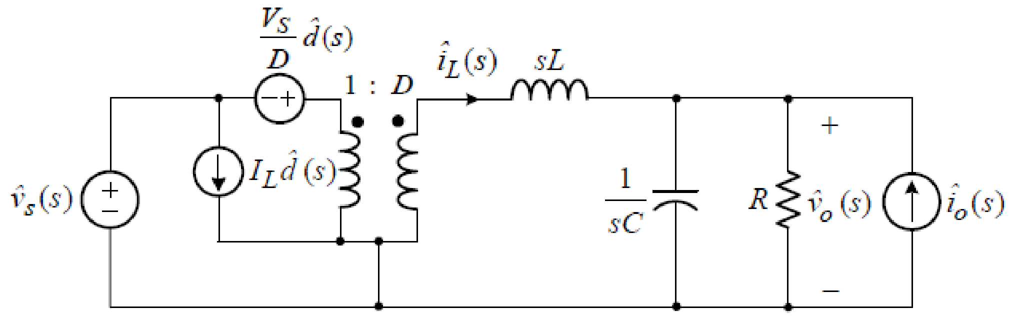
Switch Model Response



Average Model Response

Source: Byungcho Choi, Pulsewidth Modulated Dc-to-DC Power Conversion. Wiley IEEE Press, 2nd Edition.

Buck Converter Transfer Functions



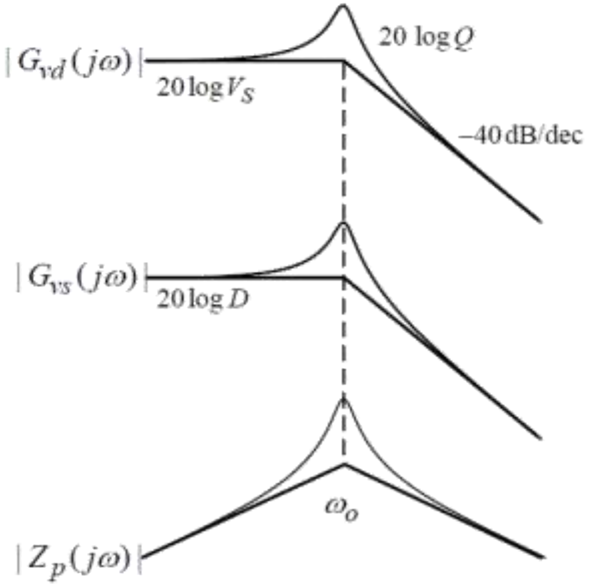
- Frequency response of transfer functions:

$$G_{vd}(s)=\frac{\hat{v}_o(s)}{\hat{d}(s)}=\frac{V_S}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}$$

$$Q=R\sqrt{\frac{C}{L}} \text{ and } \omega_o=\frac{1}{\sqrt{LC}}$$

$$G_{vs}(s)=\frac{\hat{v}_o(s)}{\hat{v}_s(s)}=\frac{D}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}$$

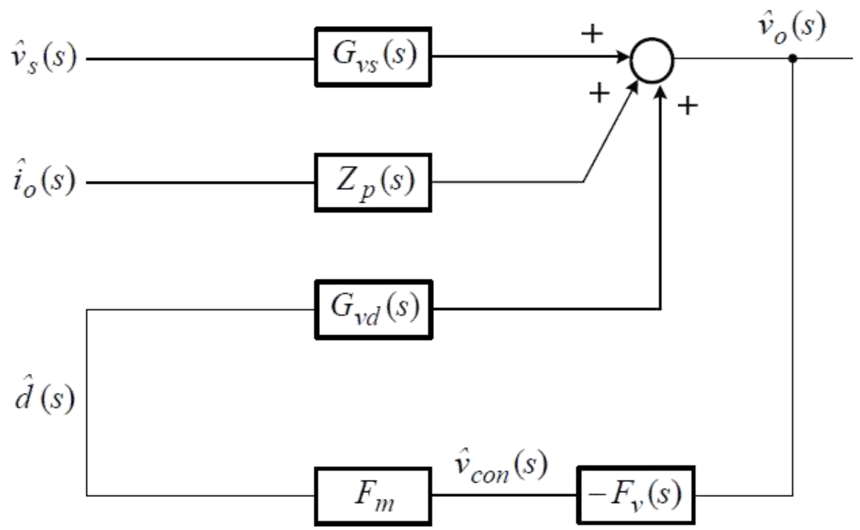
$$Z_p(s)=\frac{\hat{v}_o(s)}{\hat{i}_o(s)}=\frac{sL}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}$$



Frequency response

Small-Signal Model for Converters

- Block diagram representation



- Power stage transfer functions:

$$G_{vs}(s) = \left.\frac{\hat{v}_o}{\hat{v}_s}\right|_{\hat{i}_o = \hat{d} = 0} \quad \text{: input-to-output transfer function}$$

$$G_{vd}(s) = \left.\frac{\hat{v}_o}{\hat{d}}\right|_{\hat{v}_s = \hat{i}_o = 0} \quad \text{: duty ratio-to-output transfer function}$$

$$Z_p(s) = \left.\frac{\hat{v}_o}{\hat{i}_o}\right|_{\hat{v}_s = \hat{d} = 0} \quad \text{: load current-to-output transfer function}$$

Source: Byungcho Choi, Pulsewidth Modulated Dc-to-DC Power Conversion. Wiley IEEE Press, 2nd Edition.

Converter Modeling Summary

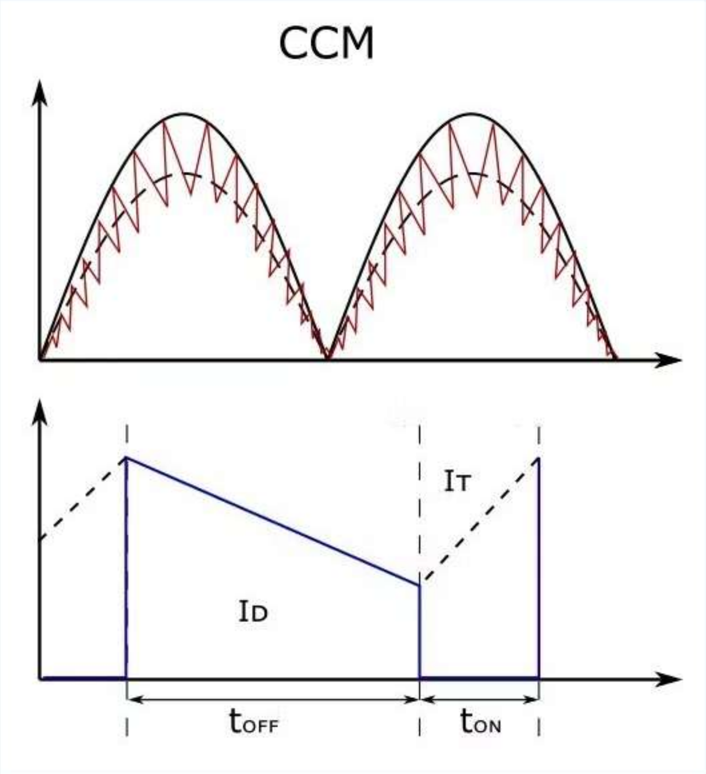
- Modeling Goal: Model DC-DC converters as a linear time-invariant (LTI) system
- Averaging: eliminate time variance from the power stage configuration
- Linearization: remove nonlinearities from the power stage dynamics and PWM process
- Small-signal model for PWM DC-DC Converters: used to build the complete small-signal model for closed-loop control

Outline

1. Data Centers Power Converter Architectures & Challenges
2. Power Factor Correction Basics
3. Modeling for DC-DC Converter Circuits
4. Modeling for PFC Circuits
5. Conclusion

Small-Signal Analysis of AC-DC Circuits

- The modeling process in not necessarily the same as standard DC-DC converters
- Averaging must be done over half the line cycle, not a switching period
- For PFCs, we are interested in Input Impedance (Zin), Output Impedance (Zout), and Control Loop
- Reference: https://www.monolithicpower.com/en/learning/resources/power-factor-correction



Simulation of AC-DC PFC Circuits

- AC Small-Signal Analysis: Outer Control Loop, Input Impedance, Output Impedance
- Circuit Simulation: often used to test and validate designs
- Long Simulation Time: becuase line-frequency period is much longer than converter-switching period
- Sometimes an AC source could be replaced by a DC source set to the AC RMS value and yield the same frequency response


IEEE Access

Received 1 October 2024, accepted 28 October 2024, date of publication 4 November 2024, date of current version 18 November 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3491299

METHODS

Simulation Technique and Mathematical Basis for Faster AC Analysis of Power Factor Correction Boost Converters

KATHERINE A. KIM[1], (Senior Member, IEEE), AND THOMAS G. WILSON JR.[2], (Member, IEEE)

[1]Department of Electrical Engineering, National Taiwan University, Taipei 10617, Taiwan

[2]SIMPLIS Technologies, Portland, OR 97240, USA

Corresponding author: Katherine A. Kim (kakim@ntu.edu.tw)

This work was supported in part by the National Science and Technology Council (NSTC) of Taiwan under Grant 113-2628-E-002-008, and in part by SIMPLIS Technologies.

ABSTRACT Power factor correction (PFC) boost converters are widely used for single-phase industrial ac-dc applications, where simulation is typically used for design and verification. However, running simulations with an ac source at the line frequency (50-60 Hz) can be time-consuming due to the long line period compared to the converter switching period. For PFC converters, the control loop, input impedance, and output impedance are critical to analyze the converter performance. We show that the ac analysis of the control loop and output impedance yields the same frequency response when using an ac and dc voltage source with the same rms value for a single-phase constant-frequency PFC boost converter operating in continuous conduction mode with a high power factor. The mathematical basis for this finding is derived based on a line-averaged rectified converter model. In contrast, for the ac analysis of the input impedance, an ac source must be used for the simulation. A mathematical derivation of this result is presented based on a line-averaged ac-side converter model. From these findings, the use of a dc source for ac analysis of the control loop and output impedance reduced the simulation time to less than 6.8% of that with an ac source.

INDEX TERMS AC analysis, boost converter, input impedance, outer control loop, output impedance, power factor correction, simulation techniques, small-signal modeling.

I. INTRODUCTION

Power factor correction (PFC) circuits in ac-to-dc converters are critical for modern appliances because they reduce the harmonics imposed on the grid by nonlinear electronic loads, such as computer power supplies and household appliances [1]. Since harmonic suppression limitations and maximum harmonic currents are regulated by international standards, such as IEC 61000-3-2 [2], commercial ac-to-dc converters with input power over 75 W are generally equipped with PFC circuits. The boost converters are the most common topology used to implement a PFC circuit because they have the advantages of a continuous input current and a straightforward design of the gate driver and control circuits [3].

The associate editor coordinating the review of this manuscript and approving it for publication was Jiaxing Lei.

More recently, higher-power applications in the kW power range are also incorporating PFC circuits, including data centers [4], electric vehicle charging [5] and induction heating systems [6]. The higher the power draw, the larger the potential effect on the power quality of the grid. For example, in applications such as data centers, where there are numerous PFC converters drawing power from the same point of common coupling (PCC) [7], low-frequency stability issues have been identified that are linked to the design of the PFC circuit [8]. The work in [9] showed mathematically that instability can occur after a certain number of PFC converters are connected in parallel to the same PCC. Another study in [10] shows the importance of input impedance analysis for PFC converters to avoid resonance problems when connected to the grid.

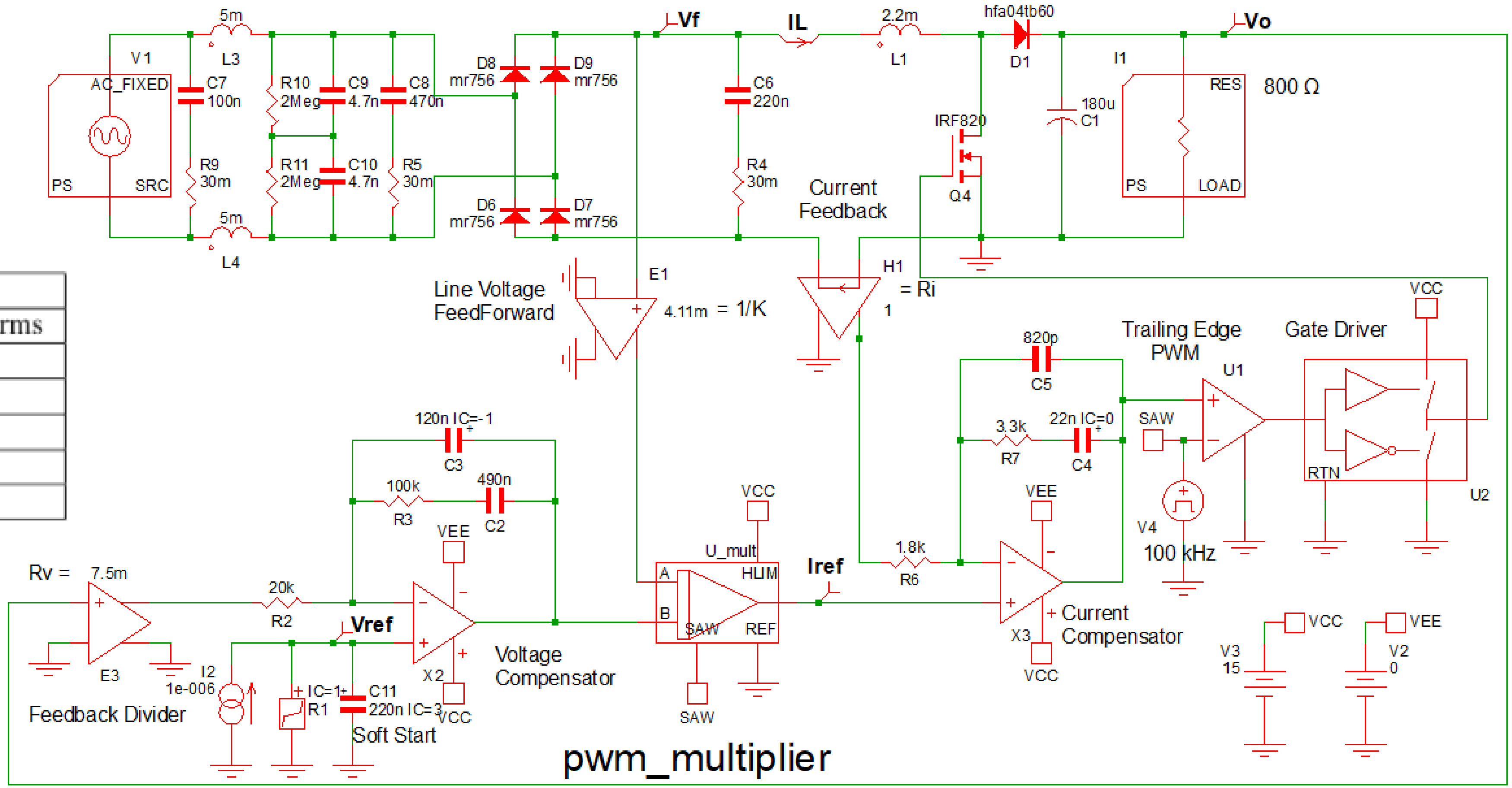
To characterize and validate the operation of a PFC converter, ac small-signal analysis (often referred to simply as

Recent Paper

K. A. Kim and T. G. Wilson, "Simulation Technique and Mathematical Basis for Faster AC Analysis of Power Factor Correction Boost Converters," in IEEE Access, doi: 10.1109/ACCESS.2024.3491299.

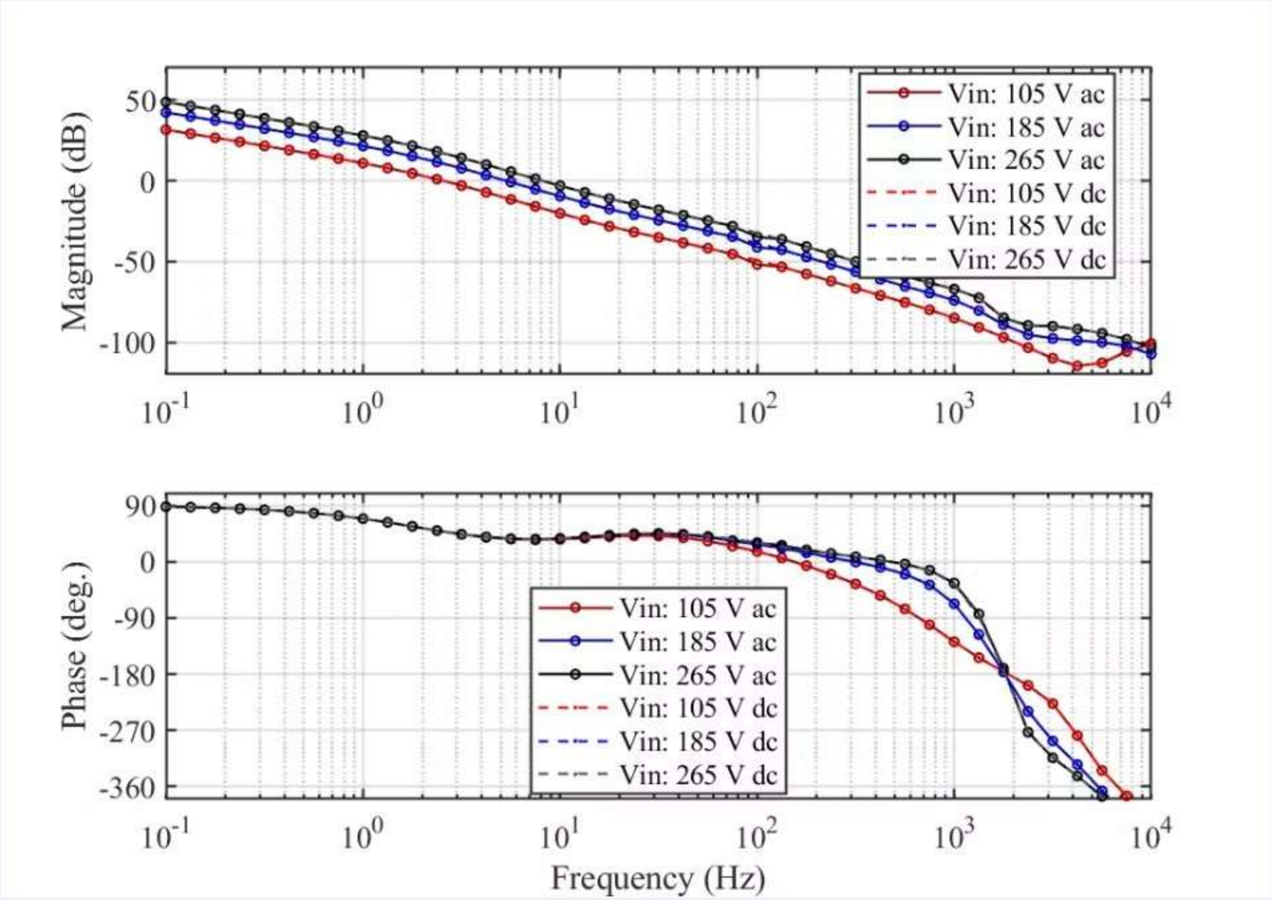
Source: K. A. Kim & T. G. Wilson, “Simulation Technique and Mathematical Basis for Faster AC Analysis of Power Factor Correction Boost Converters. IEEE Access, 2024.

PFC Boost Converter Schematic in SIMPLIS



Specification	Value
AC input voltage	105 - 265 V rms
AC line frequency	50 Hz
DC output voltage	400 V
DC output current	0.5 A
Output power	200 W
Switching frequency	100 kHz

Source: K. A. Kim & T. G. Wilson, “Simulation Technique and Mathematical Basis for Faster AC Analysis of Power Factor Correction Boost Converters. IEEE Access, 2024.



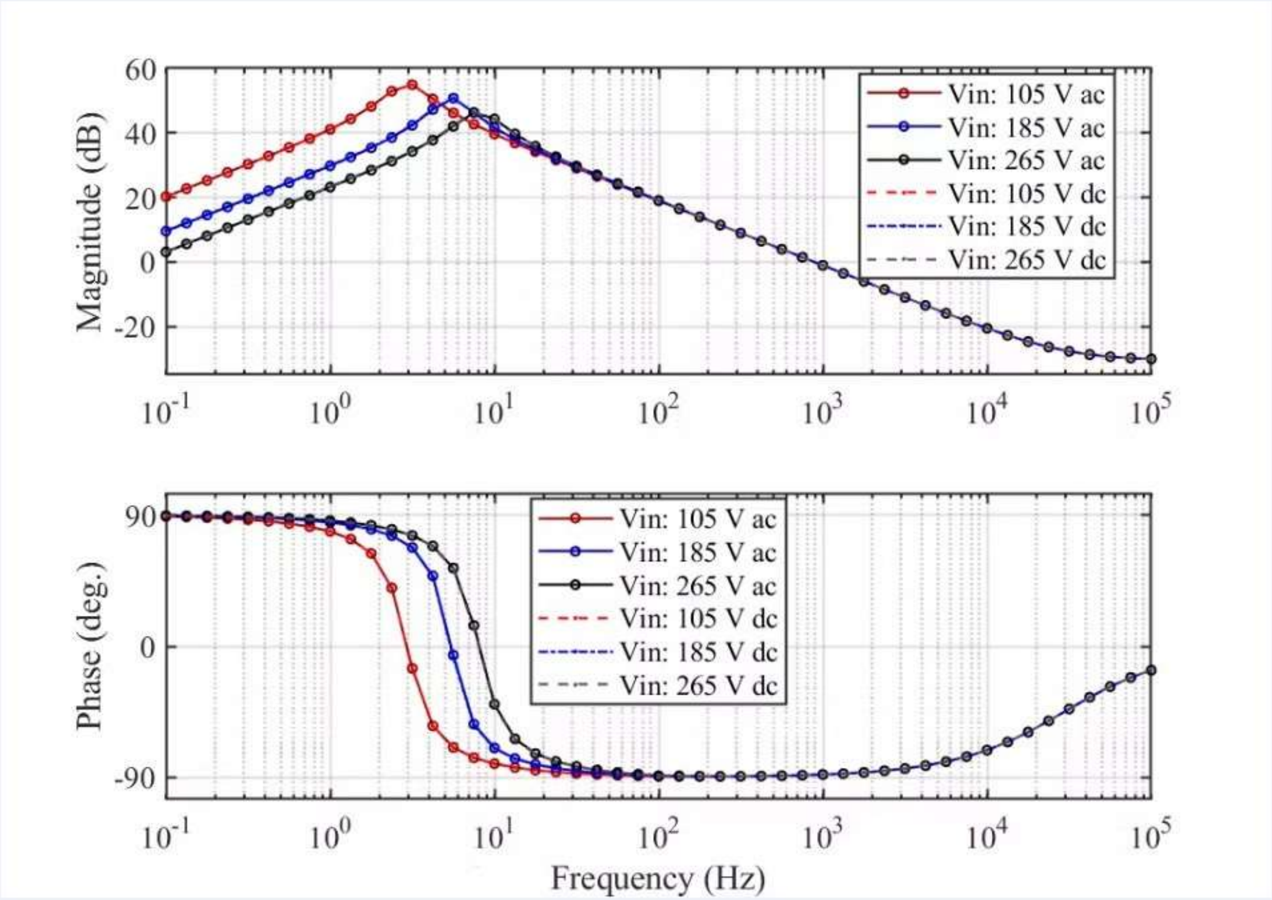
Source: K. Kim & T. Wilson, "Simulation Technique and Mathematical Basis..."

Control Loop Frequency Response

Simulation	AC Source (265 V rms)	DC Source (265 V)
Control Loop	4 min. 38 s	19 s 🙂
Output Impedance	4 min. 43 s	19 s
Input Impedance	5 min. 3 s	19 s

National Taiwan University 國立臺灣大學

PEARS LAB



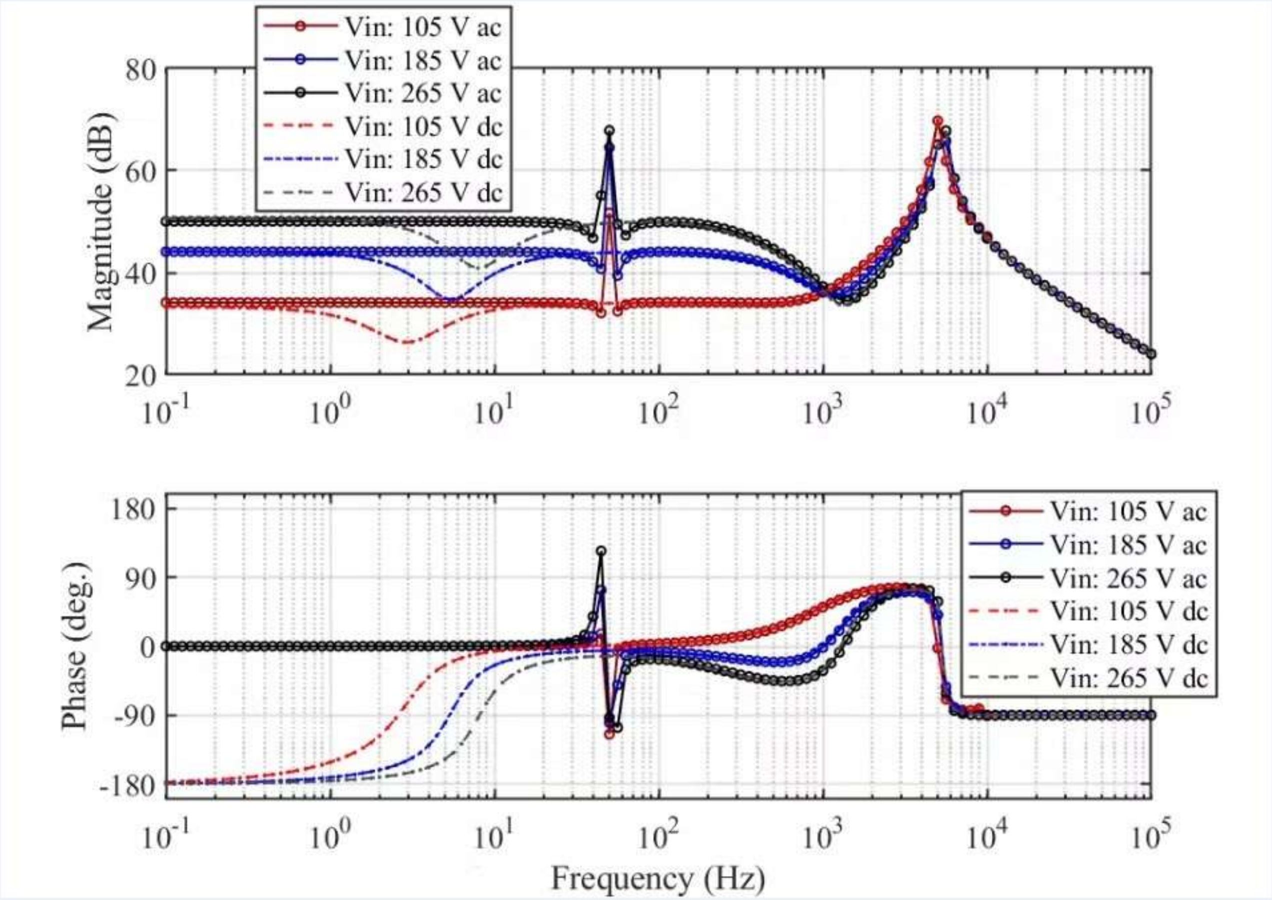
Source: K. Kim & T. Wilson, "Simulation Technique and Mathematical Basis..."

Output Impedance Frequency Response

Simulation	AC Source (265 V rms)	DC Source (265 V)
Control Loop	4 min. 38 s	19 s 🙂
Output Impedance	4 min. 43 s	19 s 🙂
Input Impedance	5 min. 3 s	19 s

National Taiwan University 國立臺灣大學

PEARS LAB



Source: K. Kim & T. Wilson, "Simulation Technique and Mathematical Basis..."

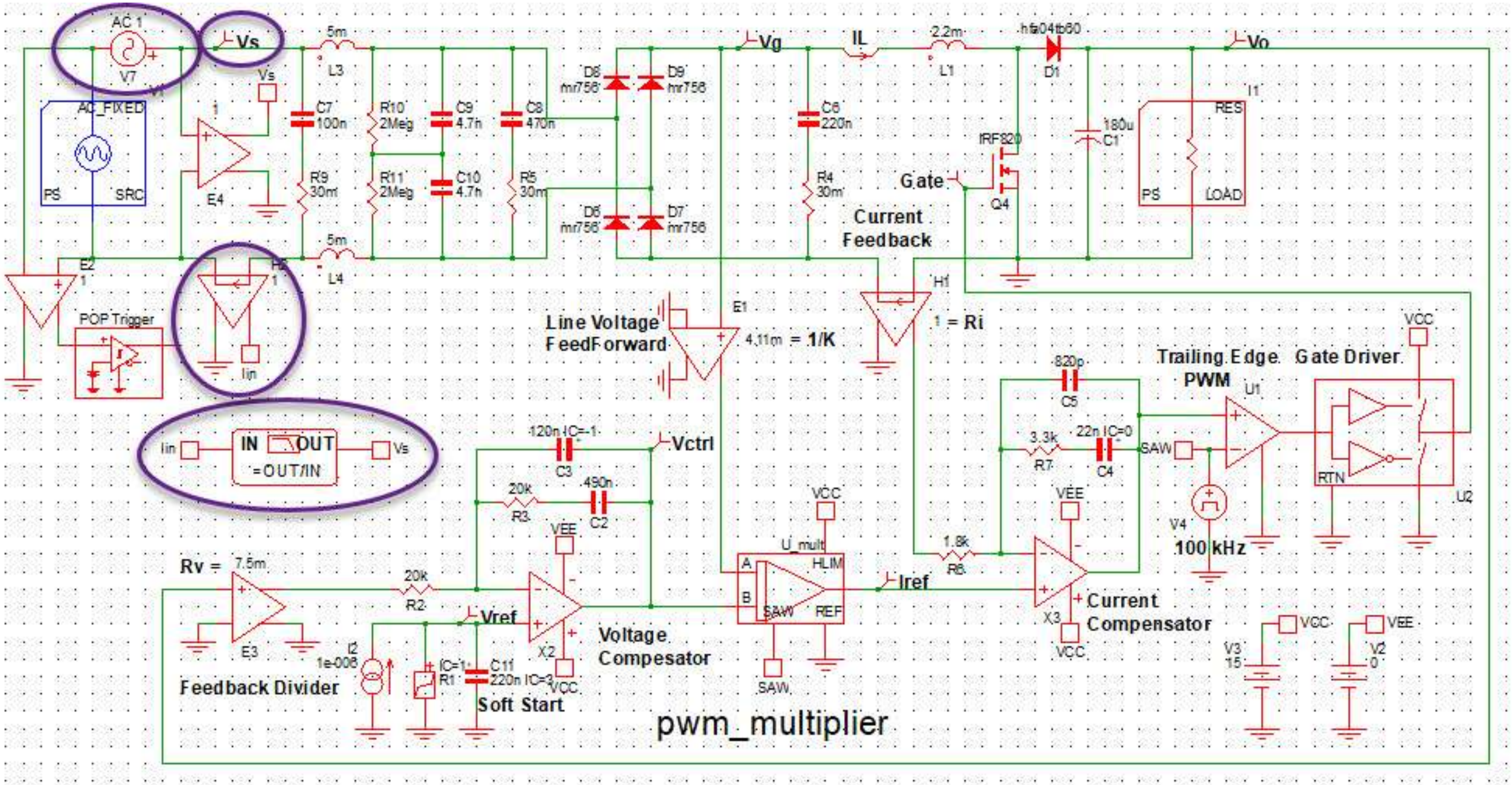
Input Impedance Frequency Response

Simulation	AC Source (265 V rms)	DC Source (265 V)
Control Loop	4 min. 38 s	19 s 🙂
Output Impedance	4 min. 43 s	19 s 🙂
Input Impedance	5 min. 3 s	19 s 🚫

National Taiwan University 國立臺灣大學

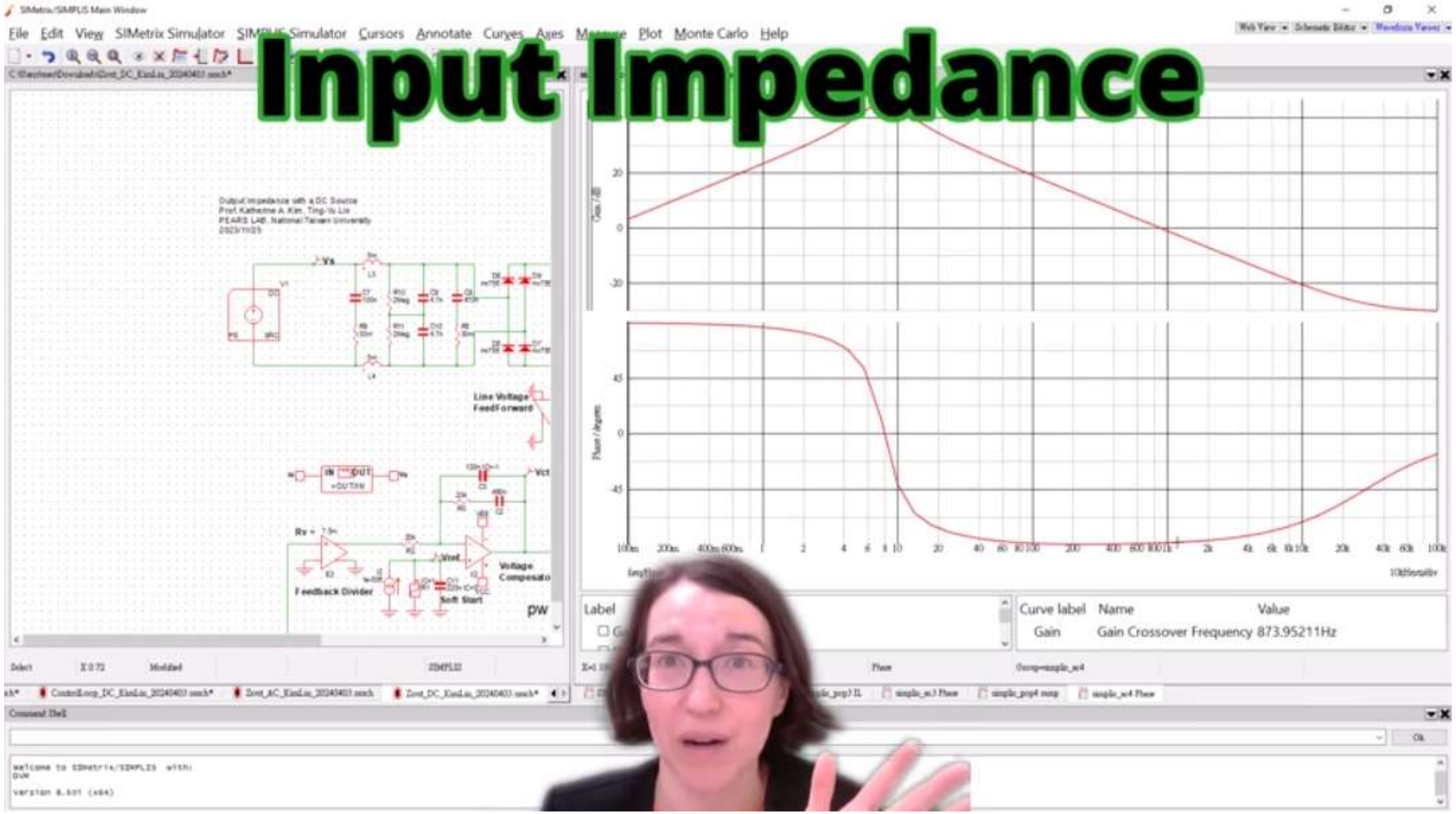
PEARS LAB

Measuring PFC Input Impedance in SIMPLIS



Source: K. A. Kim & T. G. Wilson, “Simulation Technique and Mathematical Basis for Faster AC Analysis of Power Factor Correction Boost Converters. IEEE Access, 2024.

Video: Simulation Technique for PFC Converter AC Analysis Using SIMPLIS



Watch: https://youtu.be/E8KGRb1CejQ?si=e3WuVp7L9UXIuREa

National Taiwan University 國立臺灣大學

PEARS LAB

Line-Averaged AC-Side Model

For Input Impedance

Assumptions

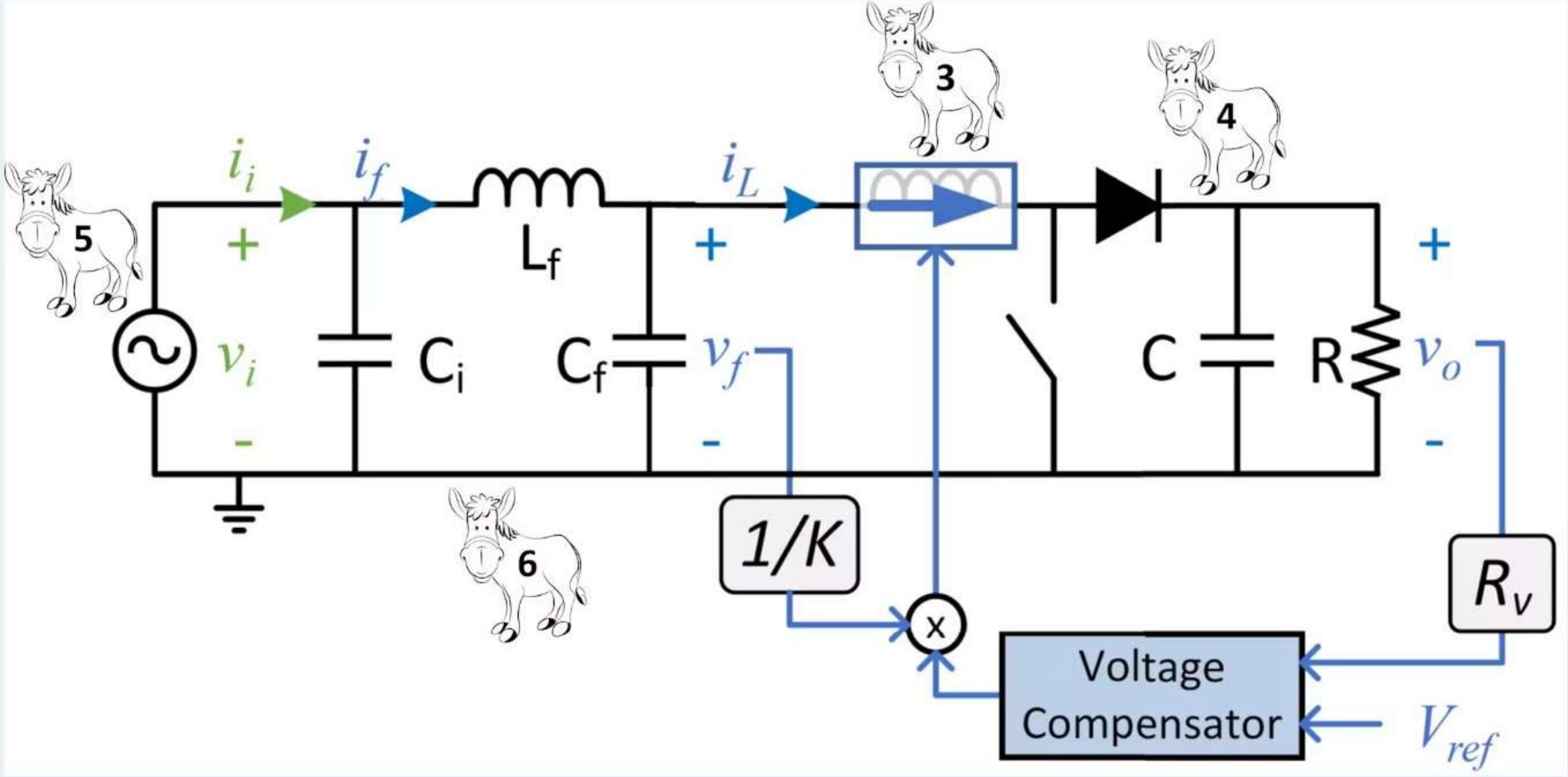
5. Input to boost converter is a (non-rectified) sine wave
6. Input filter simplified to an input C, series L, and parallel C
7. = 3. Inductor current perfectly matches the current reference
8. = 4. Boost converter operates in CCM with no losses

$$V_s = \sqrt{2} V_{rms} \sin(2\pi f_l t)$$

$$C_i = C_7$$
$$L_f = L_3 + L_4$$
$$C_f = C_6 + C_8$$

$$i_L = \frac{v_f}{K} v_{con} = i_{ref}$$

$$(1 - d) = \frac{v_f}{v_o}$$



Source: K. Kim & T. Wilson, "Simulation Technique and Mathematical Basis..."

Line-Averaged AC-Side Model: Input Impedance

$$C_f \frac{dv_f}{dt} = i_f - i_L$$

$$C_i \frac{dv_i}{dt} = i_i - i_f$$

$$L_f \frac{di_f}{dt} = v_i - v_f$$

$$C_f \frac{dv_f}{dt} = i_f - \frac{v_f}{K} v_{con}$$

1. Dynamic Equations

$$0 = V_s - V_f$$

$$\boxed{V_f = V_s}$$

$$\boxed{V_{con} = \frac{KV_o^2}{RV_s^2}}$$

2. Large-Signal Equilibrium Values

$$C_i \frac{d\hat{v}_i}{dt} = \hat{i}_i - \hat{i}_f$$

$$L_f \frac{d\hat{i}_f}{dt} = \hat{v}_i - \hat{v}_f$$

$$\hat{i}_L = \frac{V_{con}}{K} \hat{v}_f \qquad V_{con} = \frac{KV_o^2}{RV_s^2}$$

$$C_f \frac{d\hat{v}_f}{dt} = \hat{i}_f - \hat{i}_L$$

$$C_f \frac{d\hat{v}_f}{dt} = \hat{i}_f - \frac{V_o^2}{RV_s^2} \hat{v}_f$$

3. Linearization

$$C_i \frac{d\hat{v}_i}{dt} = \hat{i}_i - \hat{i}_f$$

$$L_f \frac{d\hat{i}_f}{dt} = \hat{v}_i - \hat{v}_f$$

$$\bar{V}_s^2 = V_{rms}^2$$

$$C_f \frac{d\hat{v}_f}{dt} = \hat{i}_f - \frac{V_o^2}{RV_{rms}^2}\hat{v}_f$$

4. Average over Half the Line Period

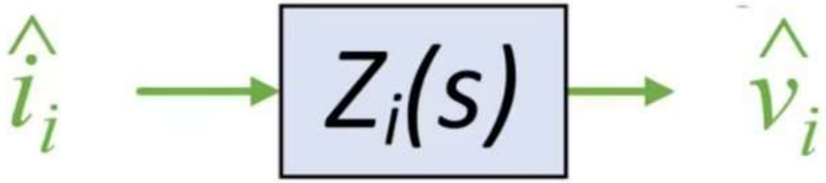
$$C_i s \hat{v}_i = \hat{i}_i - \hat{i}_f$$

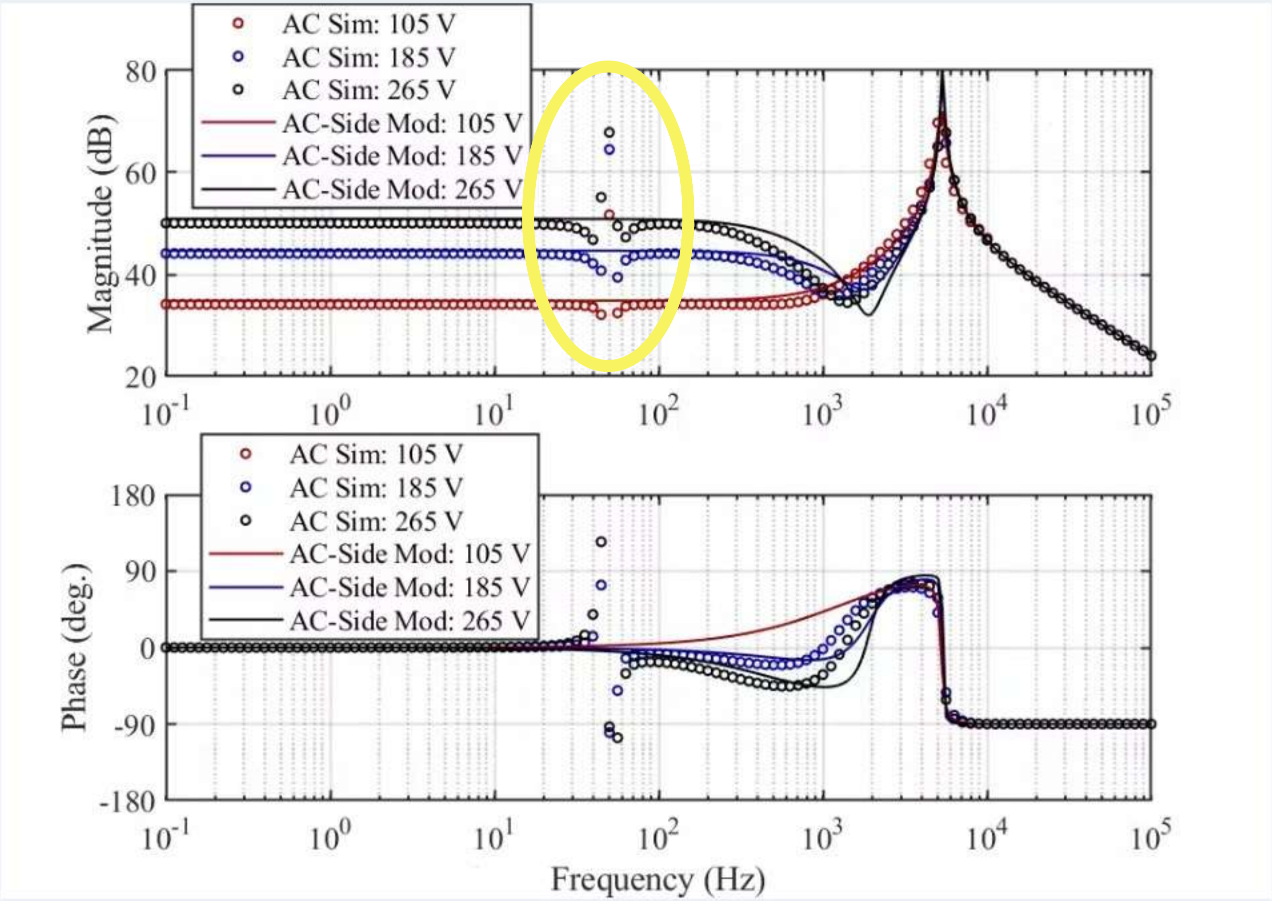
$$L_f s \hat{i}_f = \hat{v}_i - \hat{v}_f$$

$$\left(C_f s + \frac{V_o^2}{R {V_{rms}}^2} \right) \hat{v}_f = \hat{i}_f$$

$$\frac{\hat{v}_f}{\hat{i}_L} = R_{zi} = \frac{R {V_{rms}}^2}{V_o^2}$$

$$Z_i = R_{zi} \frac{L_f C_f s^2 + \frac{L_f}{R_{zi}} s + 1}{C_i L_f C_f R_{zi} s^3 + C_i L_f s^2 + (C_i + C_f) R_{zi} s + 1}$$





Problem:
Model does NOT capture the (double) line frequency interaction

Take-Away:
Must do a simulation or experimental measurement to confirm impedance characteristics

Source: K. Kim & T. Wilson, "Simulation Technique and Mathematical Basis..."

Input Impedance: Simulation vs. AC-Side Model

Source: K. A. Kim & T. G. Wilson, "Simulation Technique and Mathematical Basis for Faster AC Analysis of Power Factor Correction Boost Converters. IEEE Access, 2024.

Outline

1. Data Centers Power Converter Architectures & Challenges
2. Power Factor Correction Basics
3. Modeling for DC-DC Converter Circuits
4. Modeling for PFC Circuits
5. Conclusion

Conclusion

For a Boost PFC in Continuous Conduction Mode

- For the control loop and output impedance:
  - DC source set to the AC RMS value can be used
  - Simulation time can be significantly shortened
- For input impedance:
  - Line-averaged ac-side model can be used (derivation in paper)
  - Accurately captures all characteristics except around the line frequency
  - AC source must be used in simulation for accurate results
- In Data Centers:
  - Input impedance characteristics should be given extra attention to prevent instability in systems with many PFC converters connected to the same AC connection point

Acknowledgments

Thank you to:

Guan-Ru Li and Ting-Yu Lin: who contributed to the preliminary research for this work

Christophe Basso and Mauricio Cespedes: who gave feedback on the early article versions

Resources

SIMPLIS schematic and Matlab files: http://pearslab.net/pfc-boost/

PEARS

POWER ELECTRONICS FOR ADVANCED RENEWABLE SYSTEMS LAB