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Driving AI with Core Power: Key Technologies and Design Practices of Intermediate Bus Converters (IBC)

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ECIE Laboratory
Taipei, Taiwan

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Acknowledgement

I would like to sincerely thank **ROHDE & SCHWARZ** for the kind invitation to deliver a seminar. It is a great honor to share our research and technological insights under such a prestigious platform.

Some of the results presented in this talk are based on collaborative efforts with the research teams of Prof. Huang-Jen Chiu at National Taiwan University of Science and Technology (NTUST) and my team at National Taipei University of Technology (NTUT).

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Yun-Yen Chen, and Yu-Chen Chung from NTUST, as well as Yu-Chun Lee, Tuo-Chen Lin, Shang-Xun Wu, Yun-Shan Hsieh, Tzu-Chieh Hsu, Sheng-Chieh Lan, Kuan Yi Chen, Ya-Chih Hsiao, Rou-An Chen, and Li-Chen Yu from NTUT, for their outstanding contributions and commitment to advancing high-power-density module research.

I am also deeply grateful to our industry partners for their technical support and collaboration, and to the National Science and Technology Council (NSTC) of Taiwan for providing continuous funding and research support that has made this work possible.

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Presenter

- **Yu-Chen Liu** (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from the National Taiwan University of Science and Technology (NTUST), Taipei, Taiwan, in 2009 and 2015, respectively. He was a Visiting Researcher with the Future Energy Electronics Center, Virginia Tech., Blacksburg, USA, in 2014. From 2015 to 2016, he was a Project Assistant Professor at the Department of Electronic Engineering, NTUST. From 2016 to 2022, he was an Assistant Professor and then Associate Professor with the Department of Electrical Engineering, National Ilan University, Ilan, Taiwan. Since 2022, he has been an Associate Professor with the Department of Electrical Engineering, National Taipei University of Technology, Taipei, Taiwan. In 2024, he received the 2nd Delta Young Scholars in Power Electronics Technology Lecture Award. His research interests include analysis and design of zero-voltage-switching dc-dc converters, power factor correction techniques, redundant sever power supplies, and high efficiency converters.

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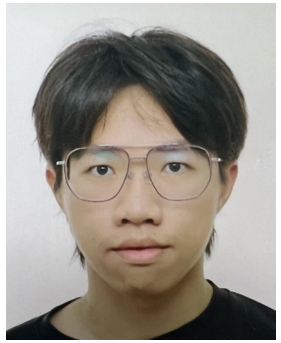
ECIE Team Members

Yun-Yen Chen was born in Taoyuan, Taiwan, R.O.C, in 1988. He received the M.S degree in electronic engineering from National Taiwan University of Science and Technology, Taipei, Taiwan, in 2020.

He is currently working toward the Ph.D. degree at the same university. His research interests include the analysis and design of zero-voltage-switching DC/DC converters, wide bandgap device application, high frequency converter implementation, and high efficiency magnetic component design.

Yu-Chen Chung received the B.S. and M.S. degrees in electrical engineering from the National Ilan University, Ilan, Taiwan, in 2019 and 2021, respectively. He is currently working toward a Ph.D. degree in electronic engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan.

His current research interests include High-frequency power conversion, analyzing and designing resonant DC/DC converters, wide bandgap device applications, and integrated magnetics design.



Yu-Chun Lee received his M.S. degree in Electrical Engineering from National Taipei University of Technology (Taipei Tech), Taipei, Taiwan, in 2024. He is currently pursuing a Ph.D. degree.

His current research focuses primarily on fixed conversion ratio 48V-to-12V DC-DC converters for server power supplies. His main areas of analysis include high-frequency magnetic component design, circuit topology analysis, and related techniques.

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Tuo-Chen Lin received his M.S. degree in Electrical Engineering from National Taipei University of Technology (Taipei Tech), Taipei, Taiwan, in 2024. He is currently pursuing a Ph.D. degree.

The focus of his current research focuses on converter topologies for medium-voltage AC/DC (MVAC/MVDC) systems and the magnetic component design of coupled inductors for interleaved power factor correction (PFC) circuits. His research interests include three-phase AC/DC converter design, multilevel power converter architectures, and digital control techniques using DSPs in power electronic systems.

Shang-Syun Wu received his B.Sc. in Electrical Engineering from National Ilan University in 2023 and is now pursuing an M.Sc. in Electrical Engineering (power electronics) at National Taipei University of Technology. His work focuses on high-frequency converter design, magnetic component analysis, and integrating magnetic, electric-field, and thermal simulations into power-electronic circuits.

His research focuses on DC–DC converters for server power supplies, with expertise in high-frequency magnetic component design, circuit topology analysis, and front-end simulation techniques. He has presented his work at IEEE APEC, S2PC, and the Taiwan Power Electronics Conference.

Tzu-Chieh Hsu received his B.Sc degree in Electrical Engineering from National Ilan University in 2023. He is currently pursuing a M.Sc. in Electrical Engineering at National Taipei University of Technology, specializing in power electronics.

His research focuses on power factor correction (PFC) for server power supplies, digital control design, interleaved topology, phase shedding and Triangular Current Mode (TCM). He is proficient in firmware development using C language on TI C2000 series DSPs, with solid experience in control algorithm design and system implementation.

In 2024, he received the Best Paper Award at the 13th ICRERA held in Nagasaki.

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Yun-Shan Hsieh received her B.Sc. degree in Electrical Engineering from National Ilan University in 2023 and is currently pursuing her M.Sc. in Electrical Engineering at National Taipei University of Technology, Taiwan, specializing in power electronics. Her primary research interests include core loss measurement, high-frequency magnetics, and the application of machine learning in power electronics.
She has been involved in collaborative research with Lite-On Technology on AC/DC magnetic core loss measurements, focusing on automated measurement systems and deep learning-based loss prediction. She has presented her work at events such as the IEEE MagNet Challenge, S2PC, and the Taiwan Power Electronics Conference, and has hands-on experience with circuit simulation (PSIM, SIMPLIS), magnetic modeling (Maxwell), and instrument automation (PyVISA, LabVIEW).

Ya-Chih Hsiao received her B.S. degree in Electrical Engineering from National Ilan University in 2024. She is currently pursuing her M.S. degree in the Graduate Institute of Electrical Engineering at National Taipei University of Technology, specializing in power electronics.

Her primary research interests include core loss measurement and magnetic component modeling using Ansys Maxwell.

Kuan Yi Chen received his B.S. degree in Electrical Engineering from National Ilan University in 2024. He is currently pursuing his M.S. degree at the Graduate Institute of Electrical Engineering, National Taipei University of Technology, with a specialization in power electronics.

His undergraduate research focused on the control theory and simulation of permanent magnet synchronous motors (PMSM) using PLECS. Currently, his research involves high-voltage electric field simulation and high-voltage transformer design using Ansys Maxwell, where he also evaluates the parasitic capacitance of transformers through simulation

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Sheng-Chieh Lan is a master's student in Electrical Engineering at National Taipei University of Technology.

His work focuses on LLC resonant converters, with experience in circuit simulation and magnetic modeling.

Li-Chen Yu B.S. in Electrical Engineering from National Taipei University of Technology, Taiwan, expected 2025.

He was a finalist and third-place winner in the 2024 IEEE International Future Energy Challenge (IFEC). His research interests include power electronics, resonant converters, high-frequency converters, and radio frequency power amplifiers.

Rou-An Chen is an undergraduate student in electrical engineering at National Taipei University of Technology, Taiwan.

Experience includes power supply design during an internship at WTG Technology, participation in the 2024 IEEE IFEC audio amplifier project, and a paper presented at the 21st Taiwan Power Electronics Conference.

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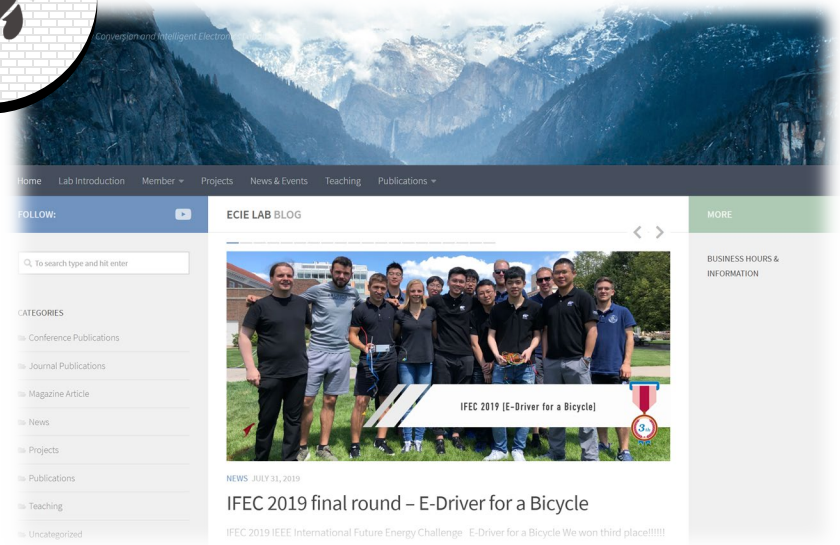

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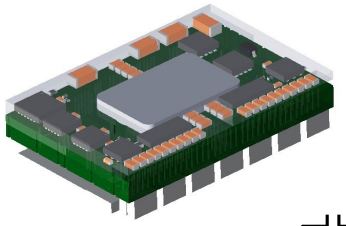
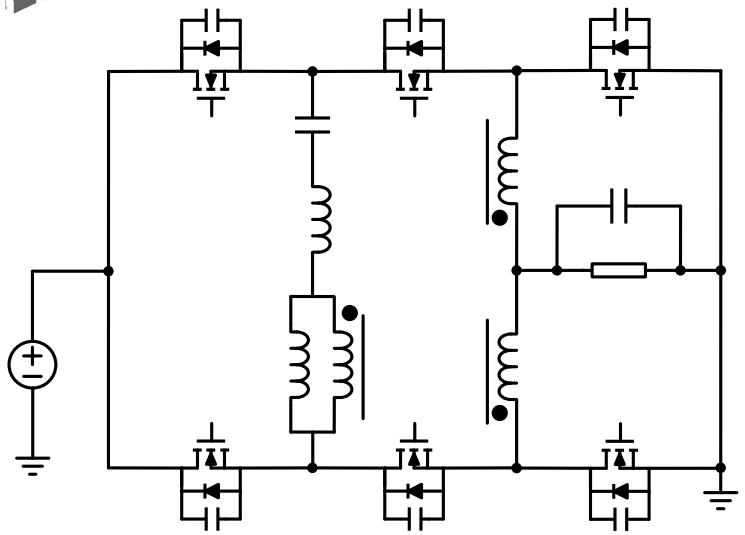
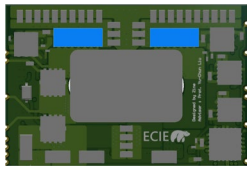
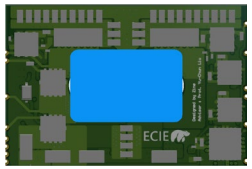
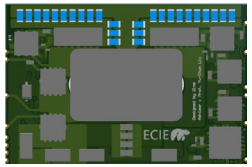
Key Technologies for High-Power-Density Modules











- **Semiconductor (GaN, SiC etc.)**
  - Conduction loss $P_{cond} = I^2 R_{eq}$
  - Switching loss $P_{sw} = \frac{1}{2} VI(t_{on} + t_{off}) f_{sw}$
  - Body diode loss $P_{diode} = I * V_f * t_d * f_{sw}$
  - Integrated driver
- **Magnetics**
  - Core loss
    - Core Material
    - Core structure
  - **Copper loss**
    - Winding arrangement
    - PCB manufacturing capability
- **Capacitors**
  - ESR loss

How to Reduce Conduction Loss

1. Select Devices with Low On-Resistance

- Use low R_{DSon} switches:
  Conduction loss is proportional to the square of the current. Therefore, choosing switching devices with lower on-resistance can significantly reduce conduction loss.
- Adopt wide bandgap devices (e.g., SiC / GaN):
  These components maintain extremely low on-resistance even under high voltage and high-frequency conditions, making them ideal for high power density applications.

2. Parallel Switching Devices

- Connecting multiple switches in parallel can share current and reduce the equivalent on-resistance.
- However, ensure even current distribution; otherwise, thermal imbalance or overload may occur.

3. Switch Selection and Thermal Management

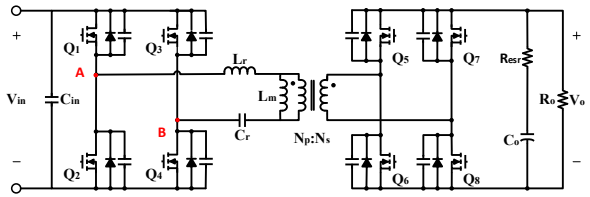
- Evaluate R_{DSon} variation with temperature:
  The on-resistance of MOSFETs increases with temperature. A good thermal design helps mitigate this increase and keeps conduction losses low.
- Check the datasheet R_{DSon} at 125°C, not just at room temperature, to ensure reliable performance under actual conditions.

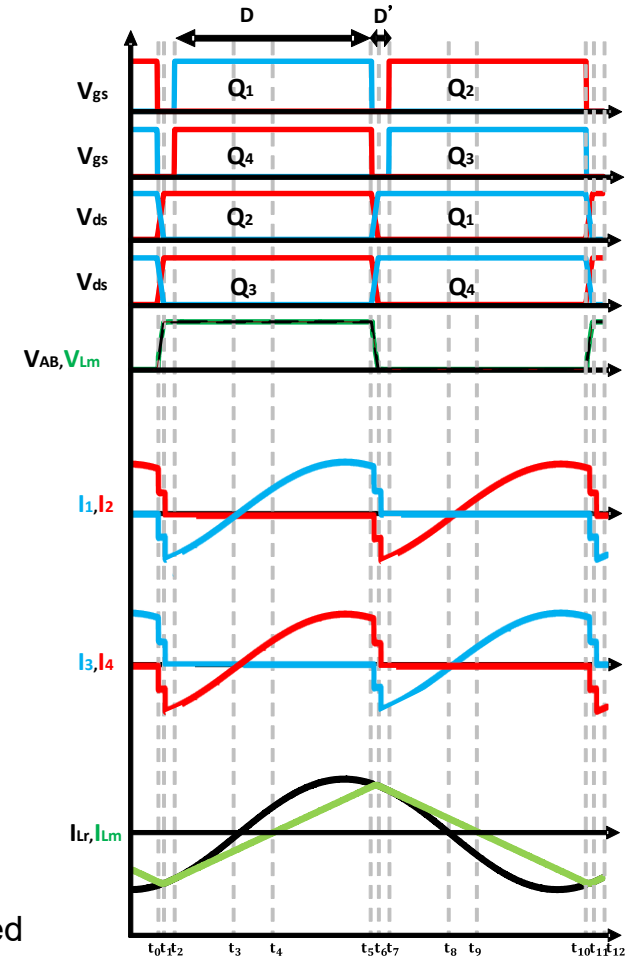
How to Reduce Conduction Loss (Continued)

4. Consider Circuit Topology Effects on Switch RMS Current

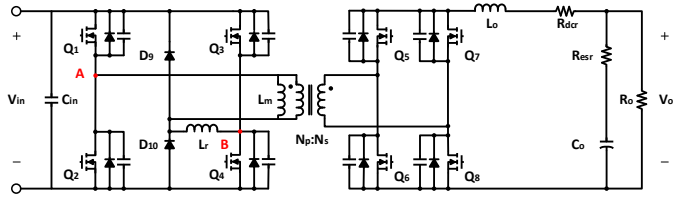
- Different converter topologies result in different switch current waveforms and RMS values. Even with the same average current, conduction losses may vary significantly.
- Example:
  - In an LLC resonant converter, the switch current is close to a sinusoidal waveform, resulting in lower RMS current and thus lower conduction loss.
  - In a Phase-Shifted Full-Bridge (PSFB) converter, the switch current is typically a rectangular waveform, leading to a higher RMS current and consequently greater conduction loss.

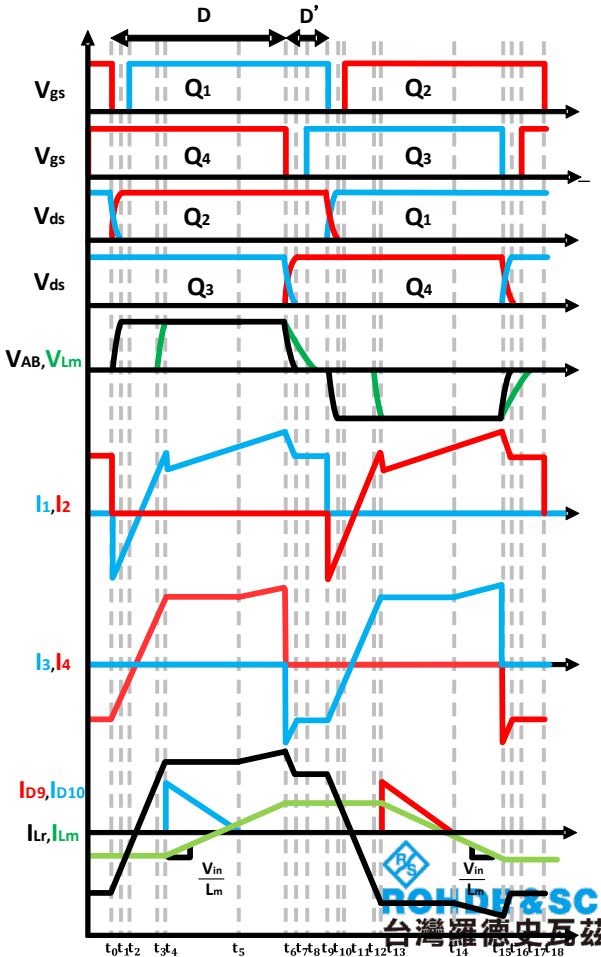
LLC resonant converter





PSFB converter





How to Reduce Conduction Loss (Continued)

Conduction Loss Source	Cause / Description	Reduction Methods & Design Strategies
MOSFET / Switch RDS(on) Loss	Power loss due to on-resistance during conduction: $P = {I_{rms}}^2 \times R_{dson}$	- Use low RDS(on) devices- Use wide bandgap devices (SiC, GaN)- Parallel switches to share current
Diode Forward Voltage Drop	Fixed voltage drop times current during conduction: $P = V_F \times I_{avg}$	- Replace diodes with synchronous rectifiers (MOSFETs)- Use Schottky or low Vf diodes
Transformer / Inductor Winding DCR	Winding resistance causes I^2R loss during current conduction	- Use thicker wires or multiple parallel strands- Reduce mean length per turn (MLT)- Use Litz wire at high frequency
PCB Trace Resistance	Copper trace resistance causes I^2R loss, especially under high current	- Widen traces or use heavier copper- Use multiple layers for current sharing- Shorten trace length
High RMS Current	Even with same average current, higher waveform RMS causes more loss	- Use topologies with smoother current waveforms (e.g., LLC)- Optimize control strategy to minimize RMS
Temperature-Related Resistance Rise	Conductor resistance increases with temperature: $R(T) = R_o(1 + \alpha(T - T_0))$	- Improve cooling design- Place components away from heat sources- Use materials with better temp. stability
Unbalanced Current Sharing	In parallel FETs or phases, current imbalance causes local overheating and increased loss	- Use current balancing resistors- Match gate resistors and layout symmetry- Apply active current sharing control
Long Conduction Path / High Loop Impedance	Extended current paths add resistance and inductance	- Optimize PCB layout- Use compact magnetic designs- Place high-current components close together

Conclusion:

The key to reducing conduction loss in switching devices lies in optimal component selection, parallel design, control strategy, and thermal management. In high-current applications, conduction loss often becomes a major efficiency bottleneck—careful design and simulation are essential early in the process.

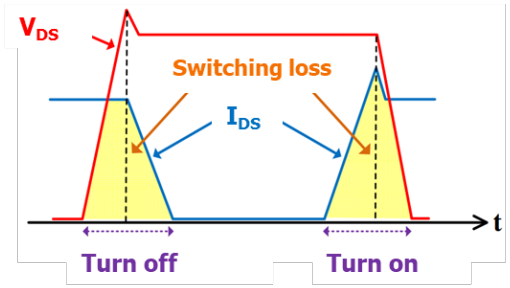
How to Reduce Switching Loss

1. Choose High-Performance Switching Devices

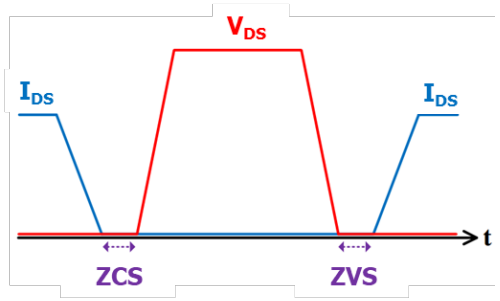
- Adopt Wide Bandgap Semiconductors (e.g., SiC/GaN MOSFETs):
  - Faster switching speeds
  - Lower on-resistance and switching capacitance
- Optimize Gate Driver Circuits:
  - Use dedicated driver Ics
  - Precisely control gate voltage to shorten charge/discharge time and reduce switching loss

2. Implement Soft Switching Techniques

- Zero Voltage Switching (ZVS) / Zero Current Switching (ZCS):
  - Ensure voltage or current is near zero during switching transitions to minimize energy loss
- Use Resonant Converters (e.g., **LLC Resonant Converters**):
  - Allow switches to operate under resonant conditions
  - Reduce voltage-current overlap during switching and minimize losses



Hard Switching



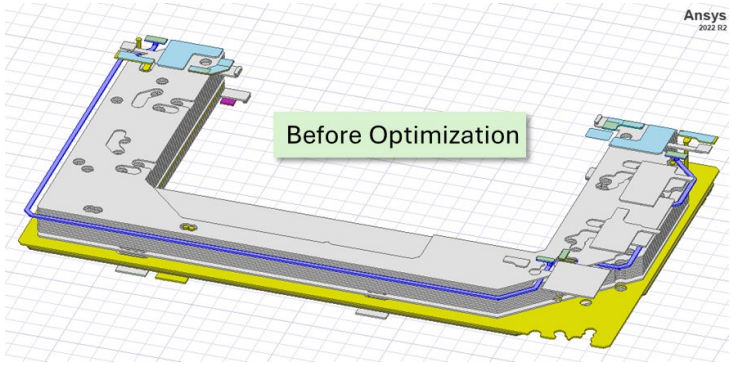
Soft Switching

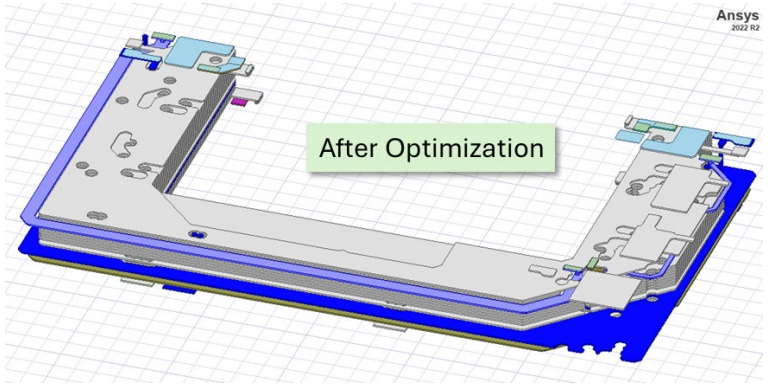
$$P_{QA,switch\_on} = \frac{1}{2} \cdot V_D \cdot I_{peak} \cdot T_{f\_\max} \cdot f_s$$

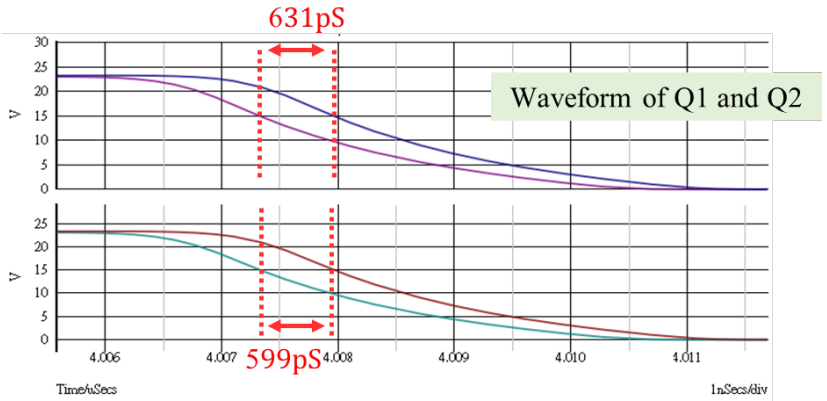
$$P_{QA,switch\_off} = \frac{1}{2} \cdot V_D \cdot I_{peak} \cdot T_{r\_\max} \cdot f_s$$

Tutorial at ICPE 2019 – ECCE Asia in Busan, Korea.
High Frequency Power Converter Design: Magnetics, Gate Driver, Control, and EMI
Jeehoon Jung, Yu-Chen Liu, Ching-Jan Chen,and Katherine A. Kim

How to Reduce Switching Loss (Continued)







4. Improve Circuit Design and Layout

- Minimize Parasitic Effects:
  - Shorten PCB traces to reduce parasitic inductance and capacitance
  - Use low-impedance PCB layout and shielding techniques to suppress ringing and EMI

5. Thermal Management

- Ensure adequate cooling (e.g., heat sinks or fans) to prevent overheating, which can increase losses and reduce component lifespan

Conclusion:

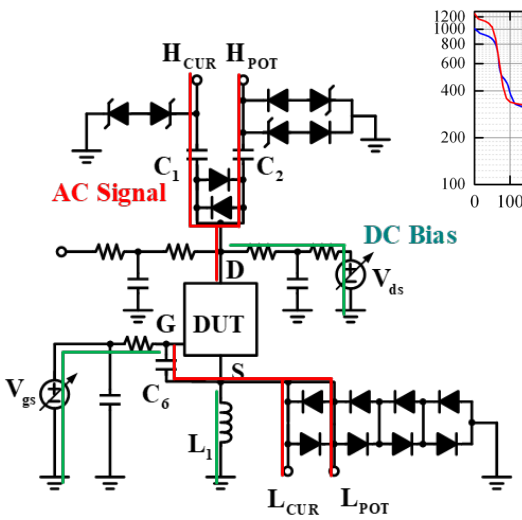
Reducing switching losses requires a multi-faceted approach, including component selection, circuit and layout optimization, control strategy refinement, and system-level integration. Each solution should be tailored to the specific application scenario to maximize efficiency and reliability.

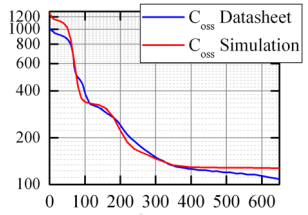
How to Reduce Switching Loss (Continued)

Switching Loss Source	Cause / Description	Reduction Methods & Design Strategies
Turn-on / Turn-off Loss	Voltage and current overlap during switching transition: $P = \frac{1}{2} V \cdot I \cdot t_{sw} \cdot f$	- Use fast switching devices (e.g., SiC/GaN)- Optimize gate driver strength- Reduce parasitic inductance
Output Capacitance Loss (Coss)	Energy to charge/discharge output capacitance every cycle: $E = \frac{1}{2} \cdot C_{oss} \cdot V^2$	- Choose devices with low Coss- Use ZVS techniques- Optimize dead time
Gate Charging Loss	Loss due to charging/discharging gate capacitance: $P = Q_g \cdot V_g \cdot f$	- Use gate driver with adaptive turn-on profile- Reduce gate charge Qg- Minimize gate voltage swing
Body Diode Reverse Recovery Loss	Reverse recovery current during body diode conduction and turn-off	- Use fast body diode MOSFETs (or SiC MOSFETs)- Avoid body diode conduction (use synchronous operation)- Add soft recovery snubbers
Parasitic Ringing Loss	Resonance between device parasitics causes high-frequency ringing and loss	- Use snubber circuits- Reduce PCB loop inductance- Apply damping techniques or ferrite beads
High Switching Frequency Loss	Switching loss scales with frequency; higher frequency increases energy per second	- Find optimal switching frequency (trade-off between size and loss)- Use soft-switching topologies (e.g., LLC, ZVS, ZCS)
Hard Switching Loss in High Voltage/Current	Large overlap of Vds and Id during transitions causes substantial power loss	- Use soft-switching techniques- Control timing to align ZVS/ZCS- Use resonant converters
Driver Undershoot / Overshoot	Improper gate driver behavior causes incomplete switching or oscillation	- Tune gate resistance- Add gate clamp / Zener diodes- Use gate driver with miller clamp

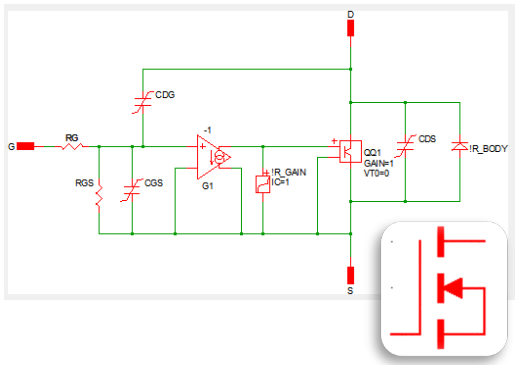
Switching Loss Modeling Flow

Parasitic Parameter Measurement	Power switch modeling	Double Pulse Test (DPT) Circuit	Circuit Simulation
Measurement of Parasitic Capacitance Characteristics.	Import measured non-ideal switching characteristics into SIMPLIS device model.	A DPT test was implemented in SIMPLIS to evaluate switching losses.	Applying the switching model to the simulation of the actual circuit.

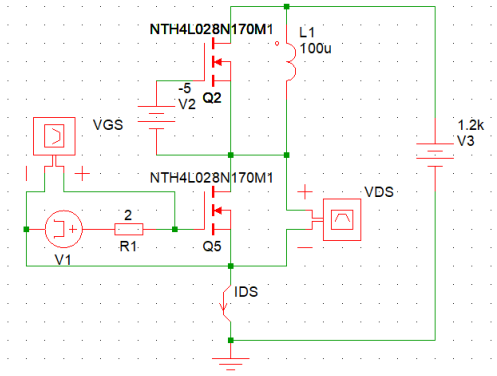




SIMPLIS TECHNOLOGIES



SIMPLIS TECHNOLOGIES



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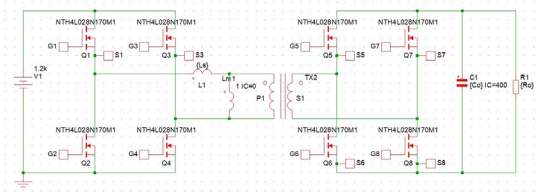

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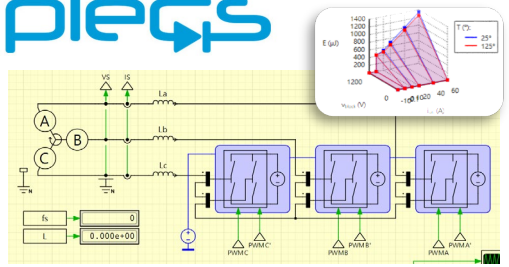

C_{oss} Measurement Circuit | **Simplis Level-3 Model** | **DPT Circit** | **Used in circuit**

Ref: T. Funaki, N. Phankong, T. Kimoto and T. Hikihara, "Measuring Terminal Capacitance and Its Voltage Dependency for High-Voltage Power Devices," in IEEE Transactions on Power Electronics, vol. 24, no. 6, pp. 1486-1493, June 2009

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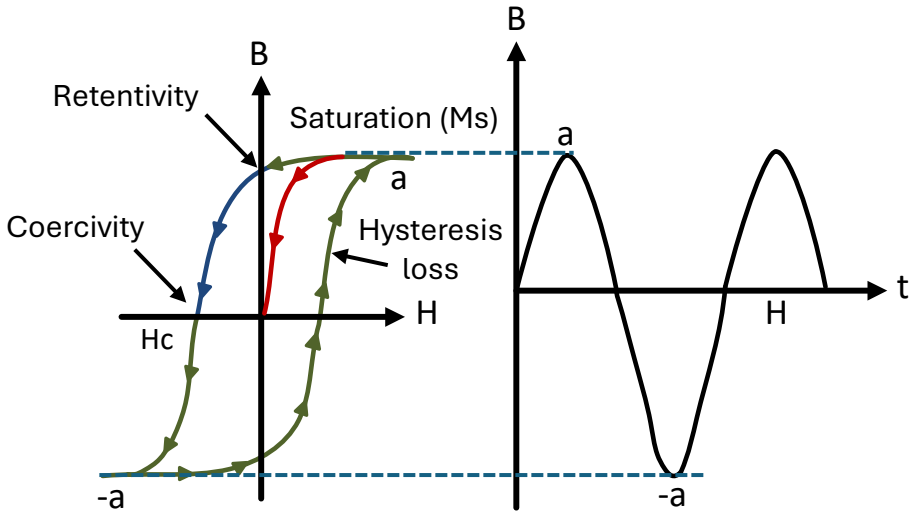
How to Reduce Core Loss?

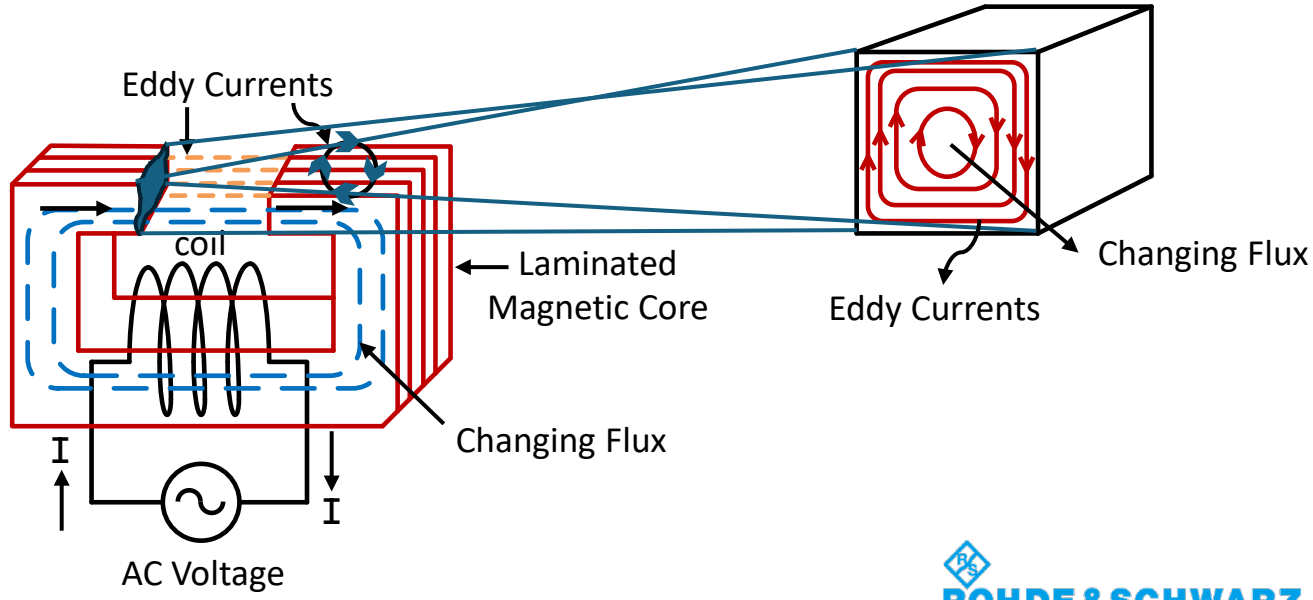
- Core loss in magnetic components primarily consists of two parts:

  Hysteresis Loss: Caused by the repeated magnetization and demagnetization cycles within the magnetic material.

  Eddy Current Loss: Generated by circulating currents induced by time-varying magnetic fields inside the core, resulting in heat dissipation.

- Core loss generally increases with **frequency (f)**, **flux density (B)**, and **core volume**.





How to Reduce Core Loss? (Continued)

1. Select Appropriate Low-Loss Core Materials

- **Ferrite**: Ideal for high-frequency applications (hundreds of kHz to MHz); exhibits low hysteresis and eddy current losses.
- **Amorphous and Nanocrystalline Materials**: Suitable for medium-frequency and high-power applications; offer high saturation flux density and low core loss.
- **Powdered Iron**: Tolerant to DC bias but generally has higher losses; should be used selectively based on application needs.

2. Control Peak Flux Density (B_{max})

- Avoid core saturation by keeping B_{max} below the recommended limits for the chosen material.
- For high-frequency ferrites, it's common to keep B_{max} below **0.2–0.3 T** to minimize losses.
- Flux density design depends on power density, operating temperature, and efficiency targets.

3. Reduce Switching Frequency

- Core loss typically increases nonlinearly with frequency.
- Use parametric design approaches to find an optimal trade-off between efficiency and converter size.

4. Optimize Core Geometry and Winding Layout

- Use core shapes that provide a short magnetic path and compact volume while meeting the required inductance.
- **Magnetic flux cancellation through winding design:** Techniques such as symmetrical or reverse winding can help reduce localized core loss.
- **Integrate external inductance into the magnetic structure:** For example, combining leakage inductance into transformer design improves power density and reduces heat concentration.

How to Reduce Core Loss? (Continued)

5. Use Air Gaps and Laminated Structures Wisely

- **Air gaps** help prevent saturation, especially in energy storage inductors. However, fringing fields around the gap can increase localized loss.

6. Employ Multiphysics Simulation for Design Validation

- Use tools like **Maxwell, COMSOL, or ANSYS** to simulate:
  - Magnetic field distribution
  - Hotspots of thermal dissipation
  - Effects of frequency and temperature on core behavior

7. Temperature Management

- Core loss is temperature-dependent:
  - Hysteresis loss tends to **decrease** with rising temperature.
  - Eddy current loss typically **increases** with temperature.
- A robust **thermal management design** (e.g., thermal paste, heat sinks, forced air cooling) is essential to maintain performance.

8. Use Accurate Core Loss Models

- Use Steinmetz equation for sinusoidal conditions:$P_{core} = k \cdot f^{\alpha} \cdot B_{max}^{\beta}$
- Since datasheet loss curves are often based on sinusoidal excitation, for real waveforms:
  - **iGSE (Improved Generalized Steinmetz Equation)**: Accurate for arbitrary waveforms.
  - **EEL (Extended Epstein Loss Model)**: Models multiple nonlinear regimes across varying frequencies and flux densities for better accuracy.

How to Reduce Core Loss? (Continued)

9. Key Techniques for Core Loss Measurement

Accurate measurement is critical to validate simulations and core loss models. Common methods include:

- **Calorimetric Method**: Measures temperature rise to estimate loss; suitable for low-loss or high-frequency cores.
- **Two-Winding Method**: Uses excitation and sensing windings with waveform integration to calculate flux and power.

10. Consider the Effect of DC Bias on Core Loss

DC bias shifts the operating point of the magnetic core, resulting in asymmetric B-H loop operation and increased loss:

- **Expanded hysteresis area**, leading to more energy loss per cycle
- Some materials (e.g., powdered iron) maintain stable magnetic behavior under high DC bias

Conclusion

To effectively reduce core loss in power converters, designers should:

- Select low-loss magnetic materials
- Optimize flux density and switching frequency
- Design efficient core geometry, gapping, and thermal paths
- Apply accurate simulation and modeling tools
- Consider real-world conditions like **DC bias**, **temperature**, and **non-ideal flux paths**

Core Loss Type	Cause / Description	Reduction Methods & Design Strategies
Hysteresis Loss	Energy loss during repeated magnetization and demagnetization cycles. Related to flux swing and frequency.	- Use low-loss materials (e.g., ferrite, nanocrystalline)- Keep Bmax within recommended range (e.g., ≤ 0.3 T)
Eddy Current Loss	Losses from circulating currents induced by changing magnetic fields; increases with frequency^2 and core volume.	- Use high-resistivity materials (e.g., ferrite)- Laminate the core or use powdered cores- Lower operating frequency or Bmax
High-Frequency Loss	Significant increase in loss at high switching frequencies (hundreds of kHz to MHz).	- Select materials optimized for high frequency (e.g., MnZn ferrite, nanocrystalline)- Combine with Litz wire to reduce heating
Temperature-Dependent Loss	Core loss behavior changes with temperature—especially conductivity and hysteresis loop shape.	- Ensure good thermal design- Use thermally stable materials (e.g., nanocrystalline, amorphous alloy)
DC Bias-Induced Loss	DC magnetization shifts the B-H operating point off-center, increasing asymmetry and loss.	- Use DC-bias-tolerant materials (e.g., powdered iron, High Flux)- Simulate magnetic behavior under bias; design air gap properly
Fringing / Leakage Loss	Magnetic flux escaping near core gaps or openings causes localized eddy currents and heating.	- Optimize air gap structure and position- Use magnetic shielding or magnetic covers- Keep windings away from air gaps
Non-Sinusoidal Excitation Loss	Real-world flux waveforms (e.g., triangular or trapezoidal) differ from ideal sinusoidal assumptions.	- Use advanced models (e.g., iGSE, EEL) to estimate loss- Simulate using actual excitation waveforms
Core Geometry / Volume Impact	Poor core shape or excessive path length increases average magnetic path and saturation risk.	- Use compact core shapes with short magnetic paths (e.g., PQ, ER, planar cores)- Reduce MLT and cross-sectional flux imbalance
Improper Air Gap Design	Large or poorly placed air gaps cause excessive fringing flux and localized heating.	- Use distributed air gaps- Balance air gap length and winding placement- Add non-conductive barriers around the gap

How to Reduce Copper Loss?

Copper loss refers to the **I^2R loss** caused by current flowing through conductors (e.g., PCB traces, winding wires, busbars).

- **In power converters:** Includes losses in MOSFET/IGBT interconnects, PCB traces, connectors, etc.
- **In magnetic components:** Includes losses in transformer or inductor windings due to **DC resistance** and **AC (skin/proximity effect)** resistance.

Area	Technique
Power Stage PCB	Wider traces, heavier copper, shorter layout
Transformer/Inductor	Use Litz wire, interleaved windings, reduce MLT
High-frequency AC	Address skin/proximity effect, simulate AC resistance
System Design	Reduce RMS current, use multiphase/interleaved topology
Thermal Management	Lower operating temperature to reduce copper resistance

By combining **electrical design**, **geometric optimization**, and **thermal management**, copper loss can be significantly reduced—leading to higher efficiency, better thermal performance, and longer component lifespan.

How to Reduce Capacitor Loss?

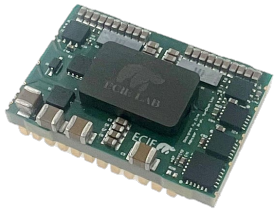
Copper loss refers to the **I^2R loss** caused by current flowing through conductors (e.g., PCB traces, winding wires, busbars).

In power converters: Includes losses in MOSFET/IGBT interconnects, PCB traces, connectors, etc.

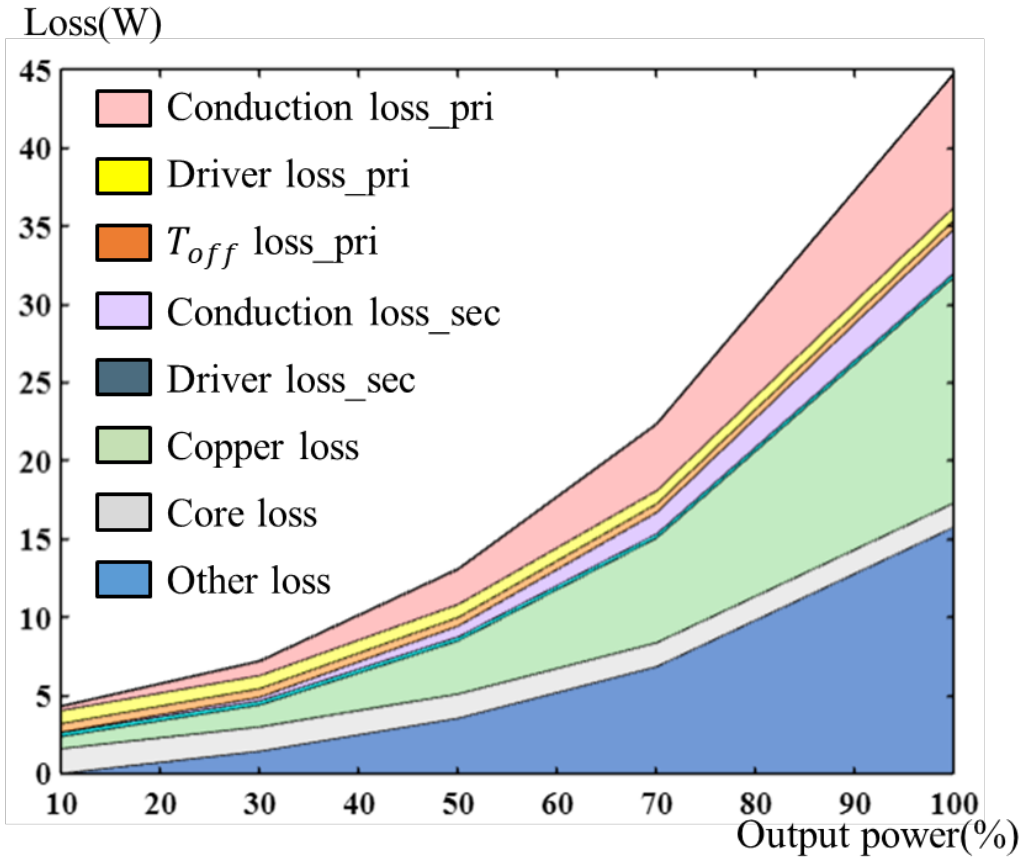
In magnetic components: Includes losses in transformer or inductor windings due to **DC resistance** and **AC (skin/proximity effect)** resistance.

Loss Type	Reduction Method
ESR Loss	Use low-ESR caps, parallel configuration, good layout
Dielectric Loss	Use high-quality dielectrics (C0G, film, polymer)
ESL-Induced Loss	Place close to switches, minimize loop area
Thermal Effect	Improve cooling, derate properly

Limitations in Efficiency Optimization of High-Power Power Converters:



- Spec: 1.2kW , 48V/12V
- Fsw : 1.08MHz
- Peak Eff. : 98.11%



Switching Loss

1. Adopting a ZVS (Zero-Voltage Switching) topology helps eliminate switching loss during turn-on.
2. Wide Bandgap (WBG) devices (e.g., GaN, SiC) offer significantly lower turn-off losses, enabling higher efficiency at high switching frequencies.

Conduction Loss

1. Conduction loss in switching devices depends on their on-resistance Rds_{on} and the specific device selection.
2. A trade-off must be made between low conduction loss and thermal handling capability.

Winding Conduction Loss

1. Limited space constrains the conductor cross-section and layout, making it difficult to minimize resistance.
2. At high frequencies, skin and proximity effects increase AC losses in windings.

Passive Component Limitations (Magnetics & Inductors)

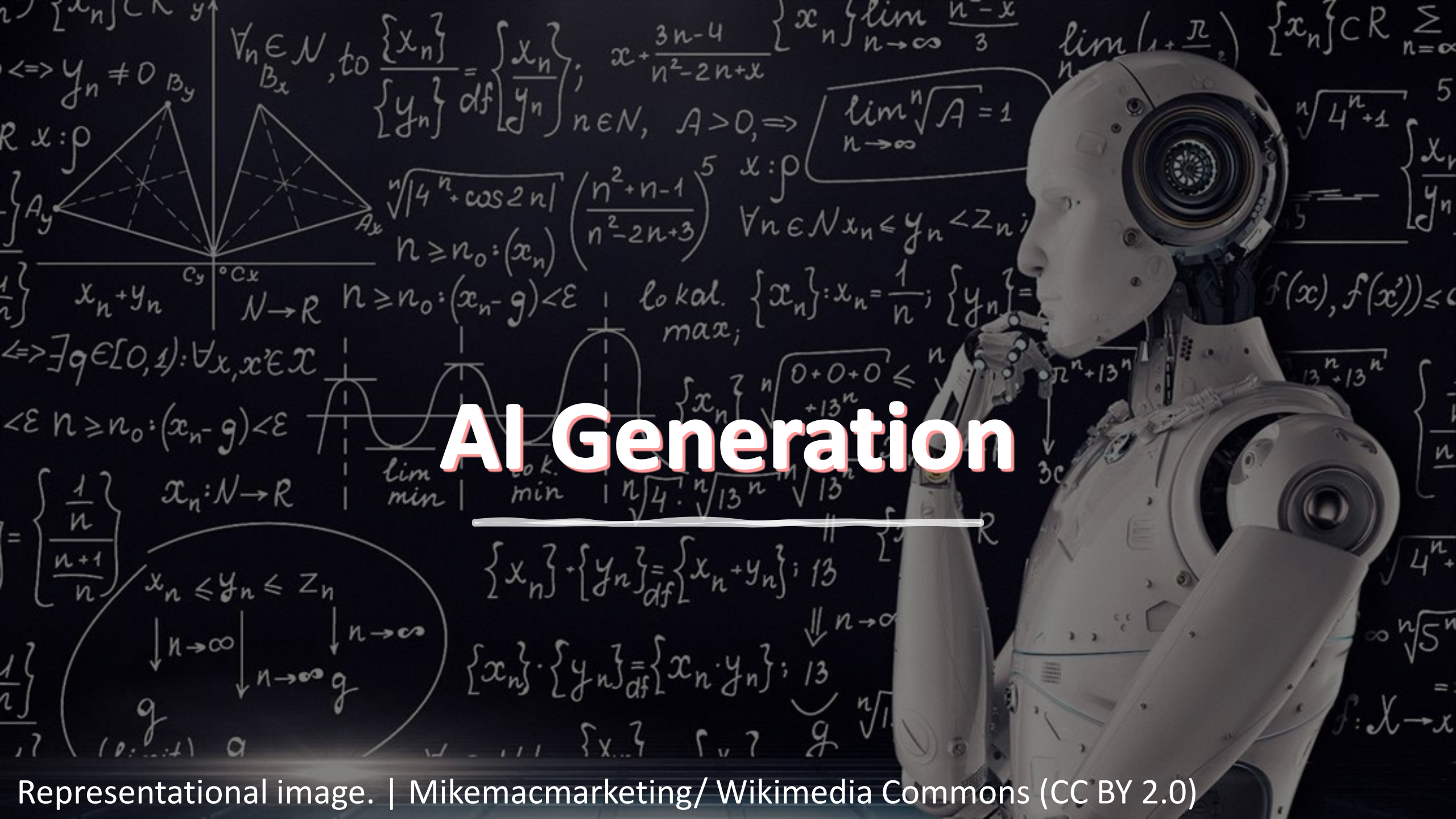
1. There is still room for optimization in the design of transformers and inductors, including magnetic core material selection and geometric layout.
2. Magnetic flux distribution, leakage inductance control, and thermal design all affect overall system efficiency.

Physical Integration and Thermal Management

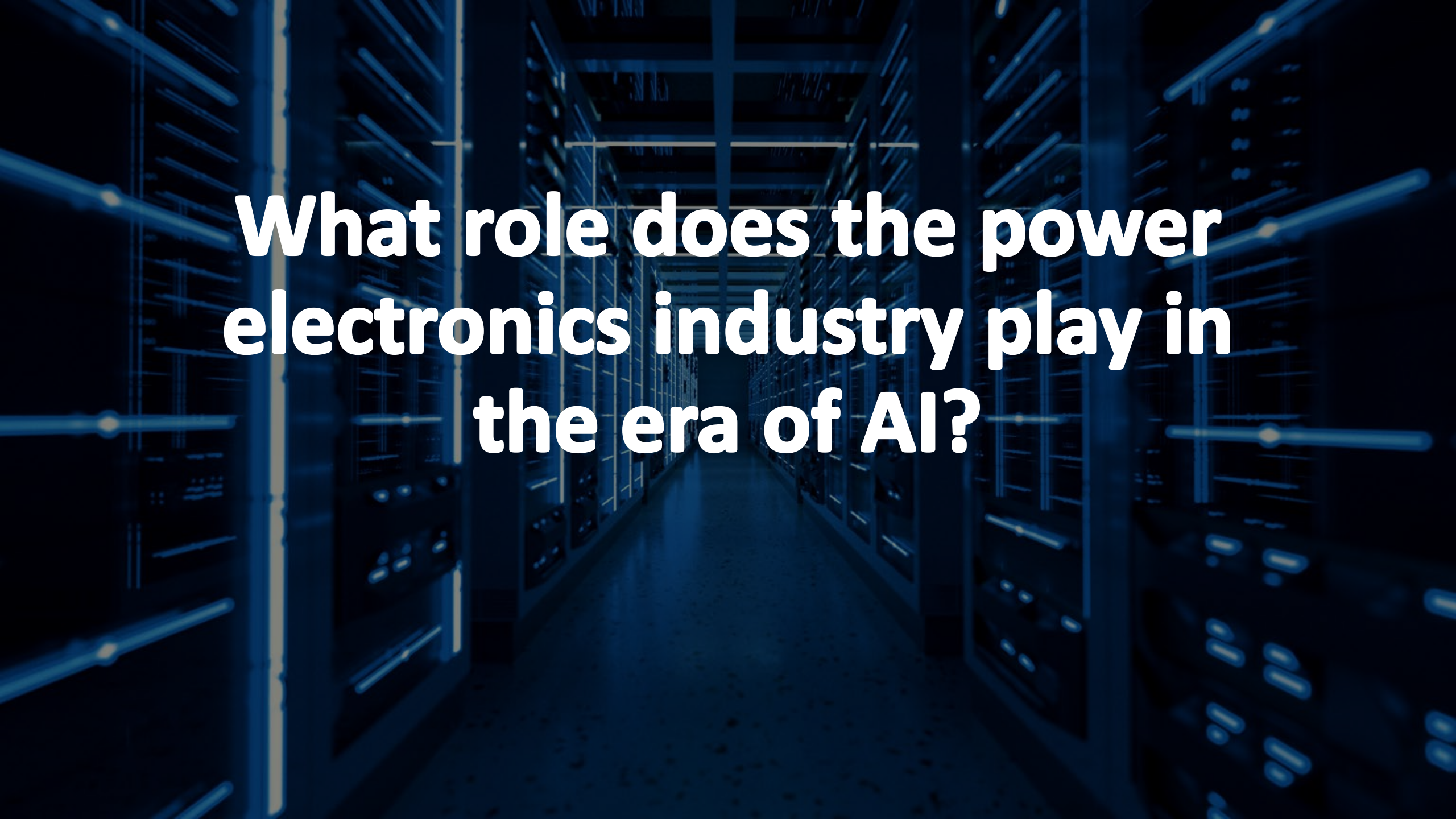
1. Power module packaging size limits available space for heat dissipation and component routing, which constrains layout and performance.
2. High power density designs require careful planning of heat conduction and thermal pathways.

Passive components play a key role in high-frequency applications.

This image was generated by ChatGPT (OpenAI) based on a user-provided concept. The characters and setting are fictional and designed to illustrate the technical challenges faced by wide-bandgap devices (such as GaN and SiC) in meeting the power demands of modern AI systems, particularly the limitations posed by magnetic components. This image is intended for educational, research, or creative non-commercial use.



Representational image. | Mikemacmarketing/ Wikimedia Commons (CC BY 2.0)

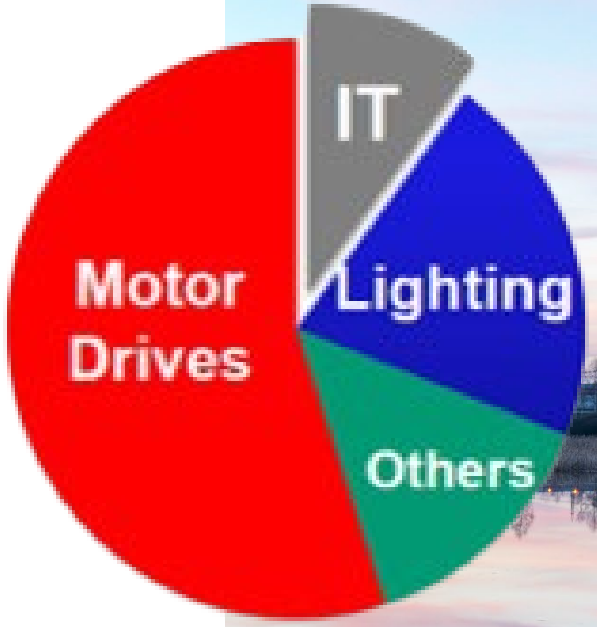

What role does the power electronics industry play in the era of AI?

ChatGPT's power consumption is extremely high, using over **500,000 kilowatt-hours per day**, which is **more than 17,000 times the electricity used by an average American household**.

According to a report in **The New Yorker**, OpenAI's popular chatbot ChatGPT may consume over 500,000 kilowatt-hours of electricity daily to respond to approximately 200 million user requests. In comparison, the average American household uses about 29 kilowatt-hours of electricity per day. By dividing ChatGPT's daily electricity usage by that of a typical household, it is found that ChatGPT uses more than 17,000 times the electricity of an average household each day.

– Total electricity consumption in 2012:
20,000 TWh*

(IT: 10% - 2,000 TWH)



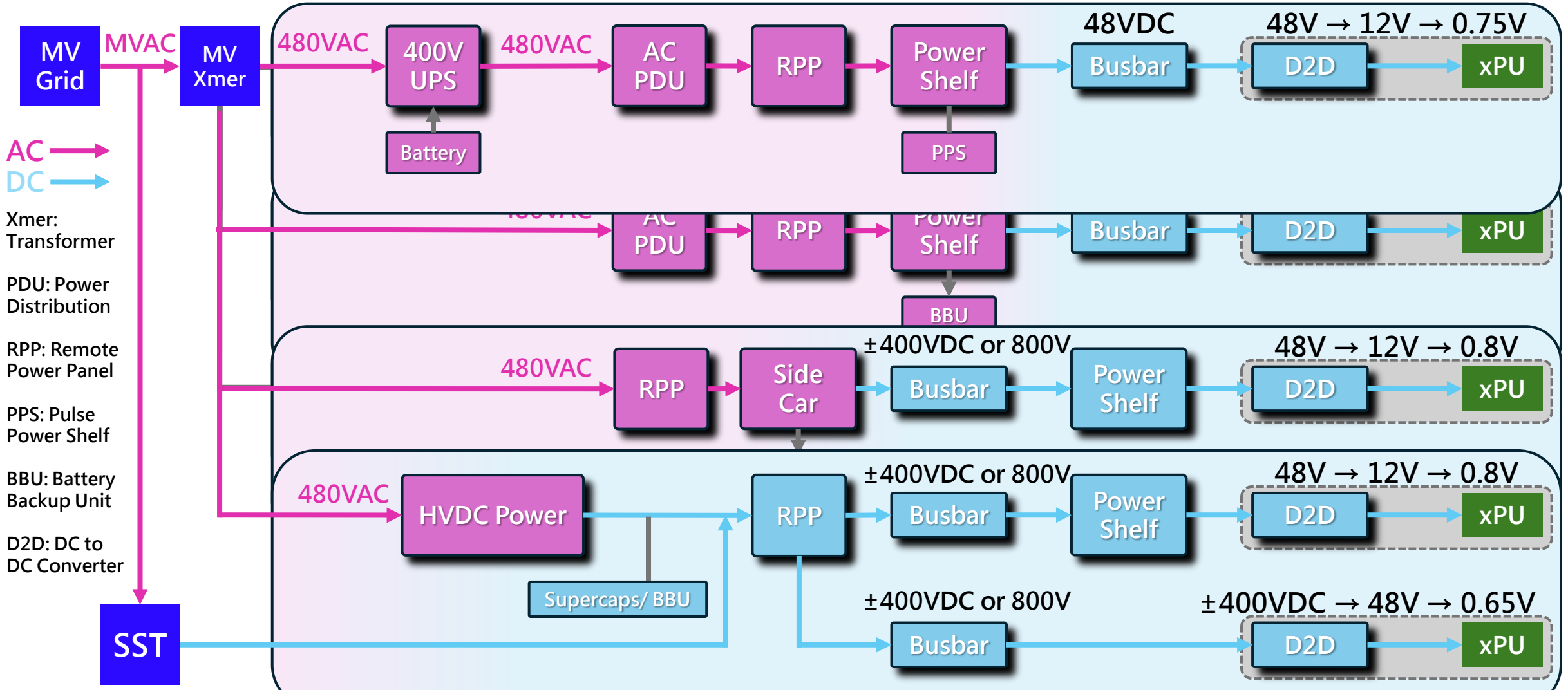
1% efficiency improvement of power supplies in IT equipment?

20 TWH saving = 3 Nuclear Power Plants
Average of 1GW capacity at 7 TWH annual output

Ref: http://www.eia.gov/cfapps/ipdbproject/IEDIndex3.cfm?tid=44&pid=44&aid=2

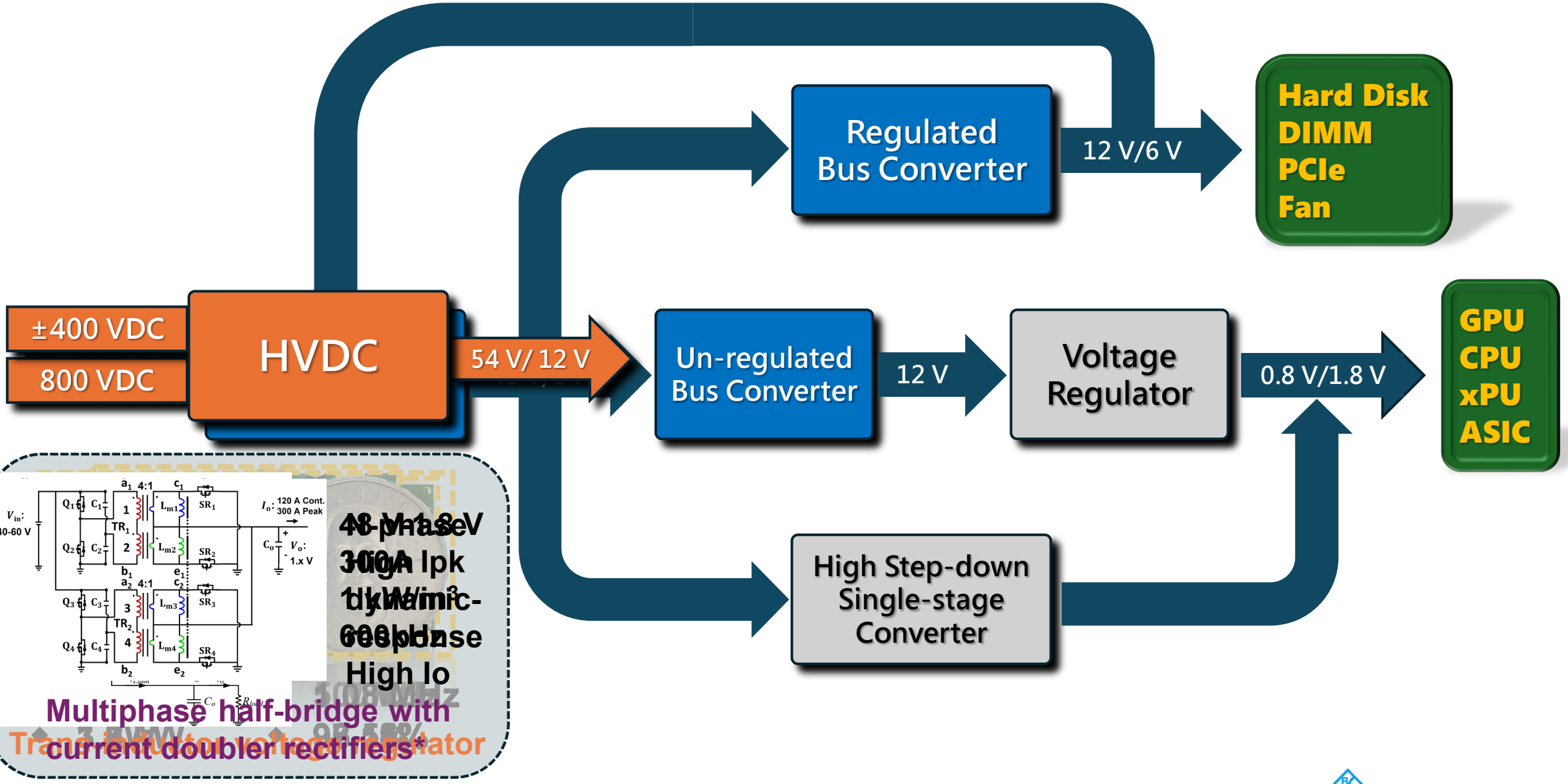
Issues Related to Winding Operation at High Frequencies

Grid: 10~35k V_{AC} → Chip: 1.x~0.6 V_{DC}



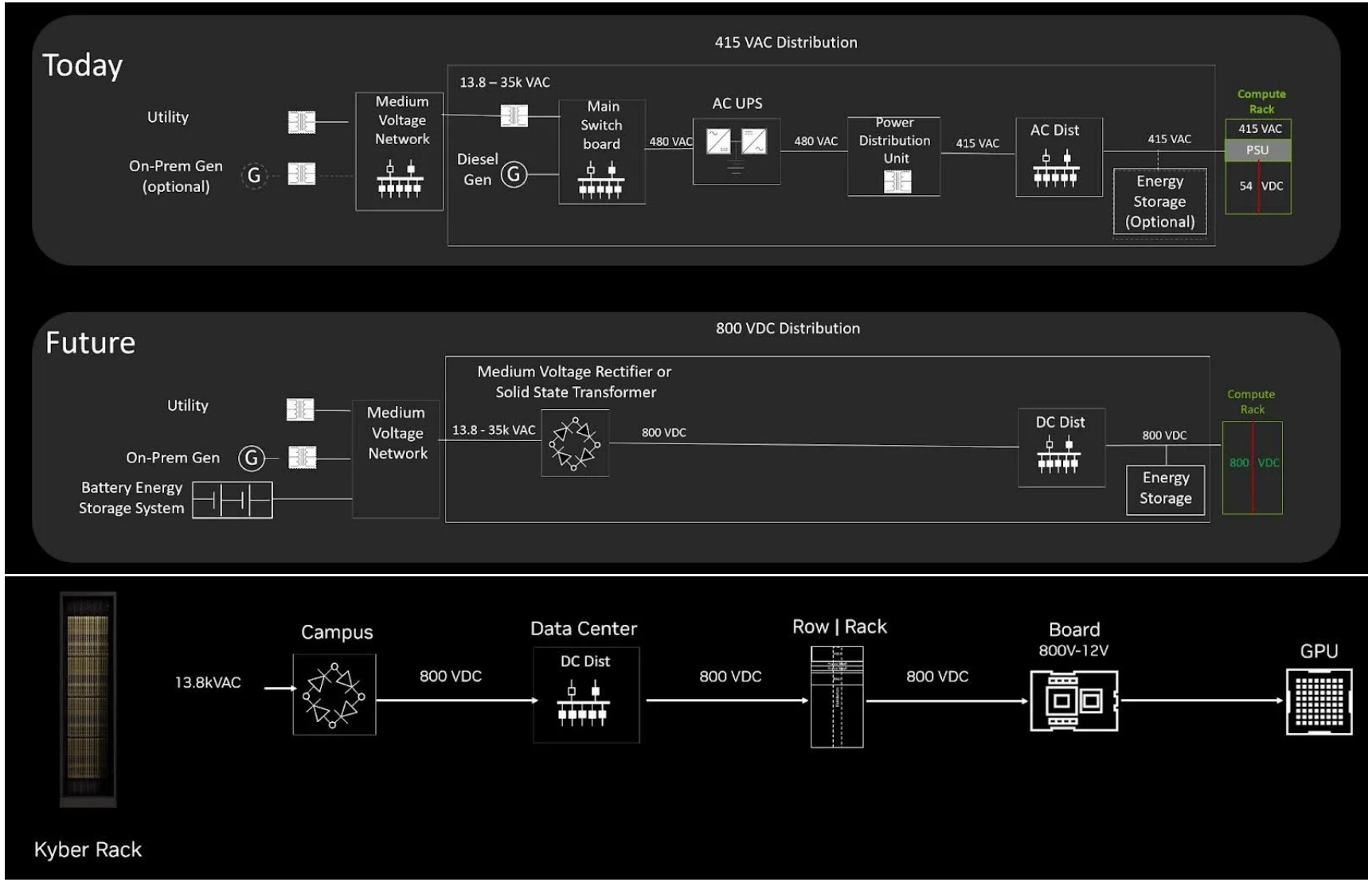
[Ref] Solid state transformer in datacenter applications, Rudy Wang, APEC2025.

Server Power



[Ref] X. Lou and Q. Li, "Single-Stage 48 V/1.8 V Converter With a Novel Integrated Magnetics and 1000 W/in3 Power Density," in IEEE Transactions on Industrial Electronics.

Building the 800 VDC Ecosystem for Efficient, Scalable AI Factories



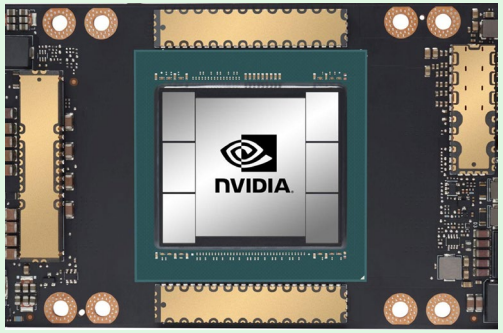
https://developer.nvidia.com/blog/building-the-800-vdc-ecosystem-for-efficient-scalable-ai-factories/

Trend of GPU Power Demand

2020 (Ampere) → (Ampere) → 2022 (Hopper) → (Ada Lovelace) → 2024 (Blackwell)

Datacenter & AI

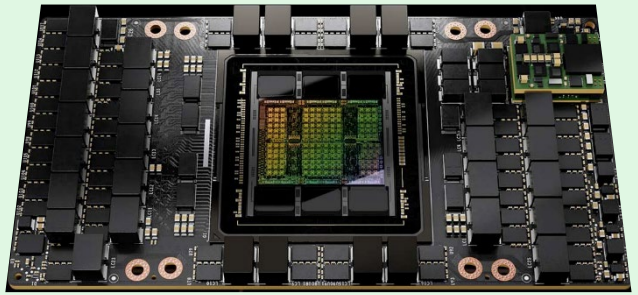
A100



- TDP: 400 W
- Die size: 826 mm²

GA102、GA104、GA106...

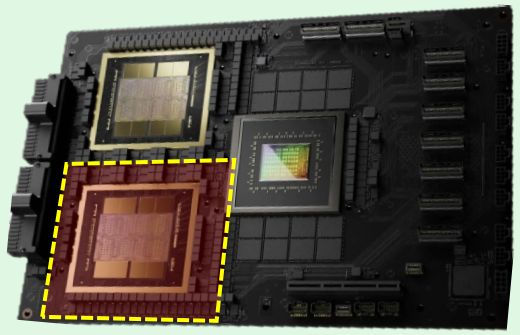
H100



- TDP: 700 W
- Die size: 814 mm²

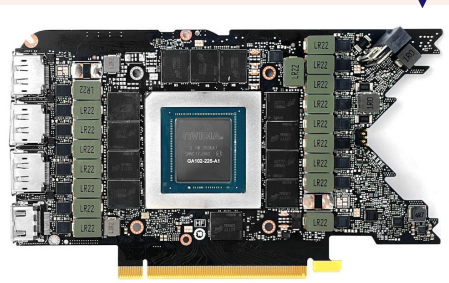
AD102、AD103、AD104...

GB200

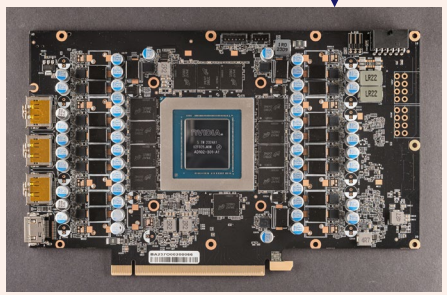


- TDP: 1000 W (*Single B200)
- Die size: 761.56 mm²

Gaming and Creator



GeForce RTX 3080 Ti
- TDP: 350 W



GeForce RTX 4090 FE
- TDP: 450 W

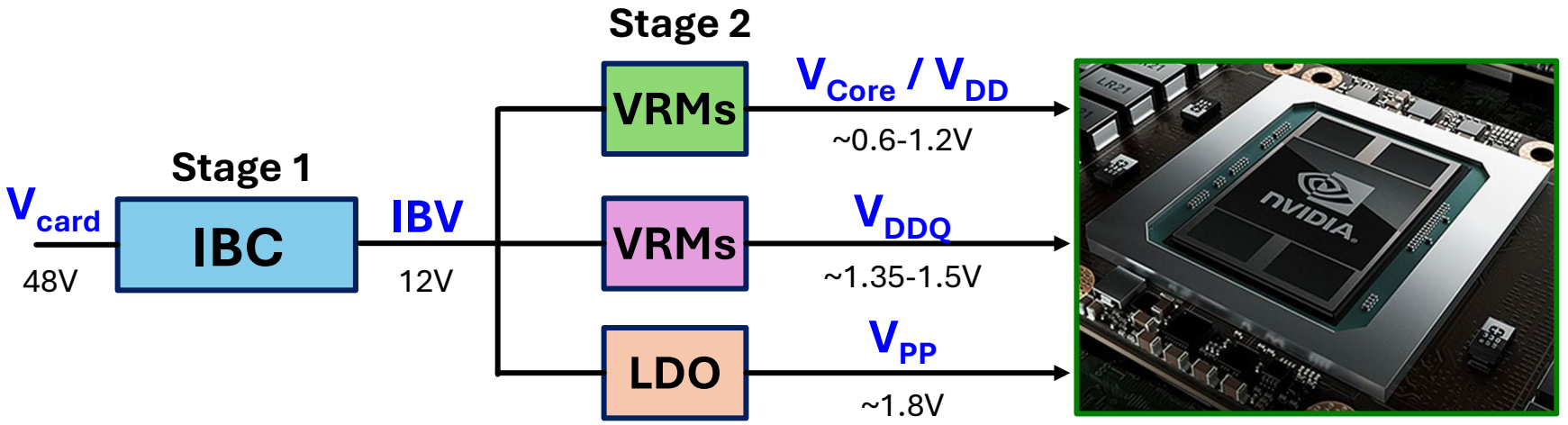
TDP: Max Thermal Design Power

Power requirement of the GPU is keep increasing

[Ref] https://www.nvidia.com/zh-tw/?ncid=no-ncid

68

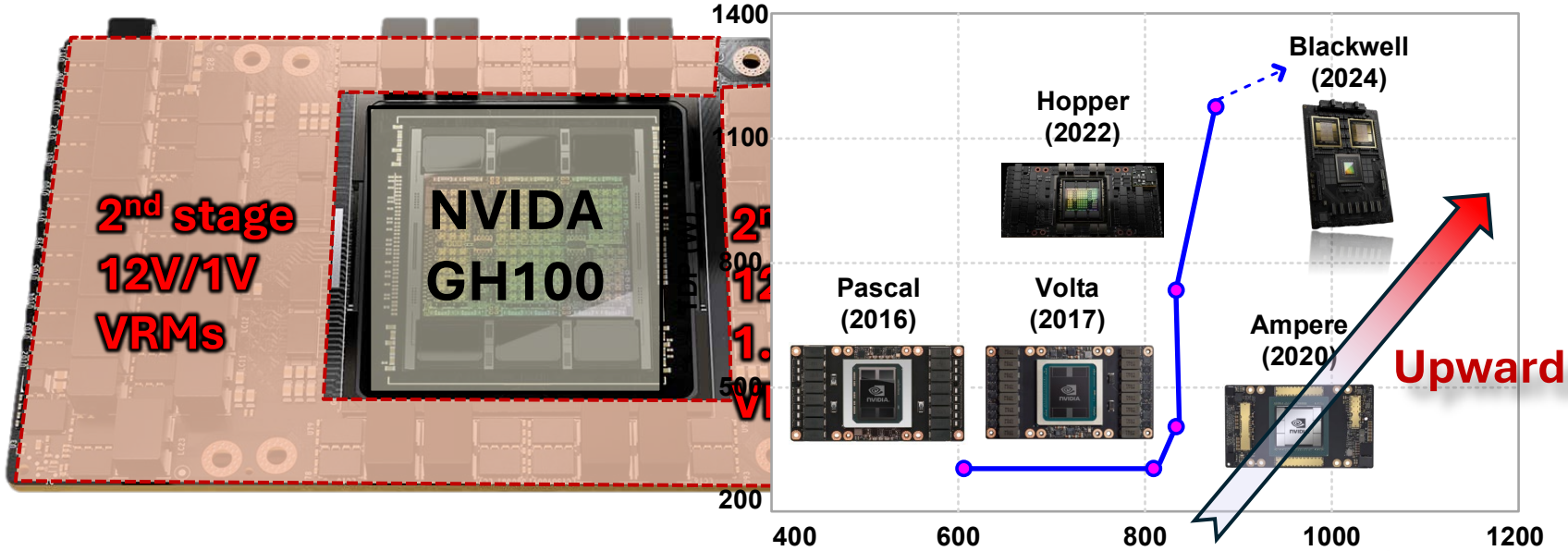
Peripheral Power Circuitry for the GPUs



IBC: Intermediate bus converter

IBV: Intermediate bus voltage

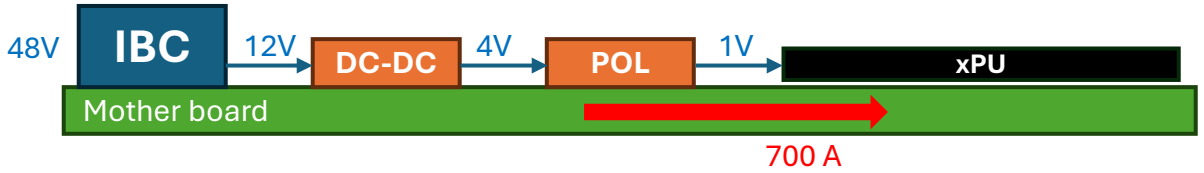
2-stage approach: Versatile for GPUs with different voltage domains

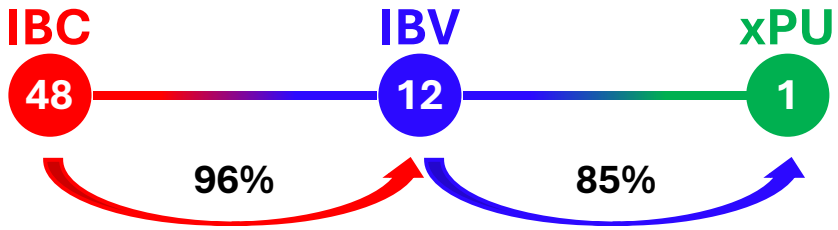


[Ref] Y. Liang, P. R. Prakash, A. Nabih and Q. Li, "Design Optimization of a 3.3 V Bus Converter for Vertical Power Delivery in Next-Generation Processors," 2024 IEEE Energy Conversion Congress and Exposition (ECCE), Phoenix, AZ, USA, 2024

Tradeoff between IBC and System Density

LATERAL Power delivery

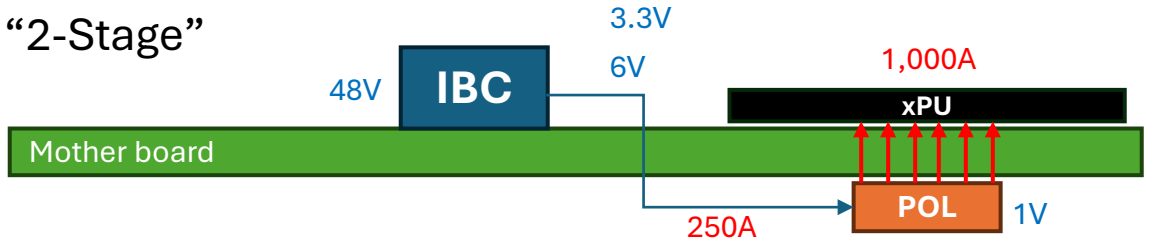


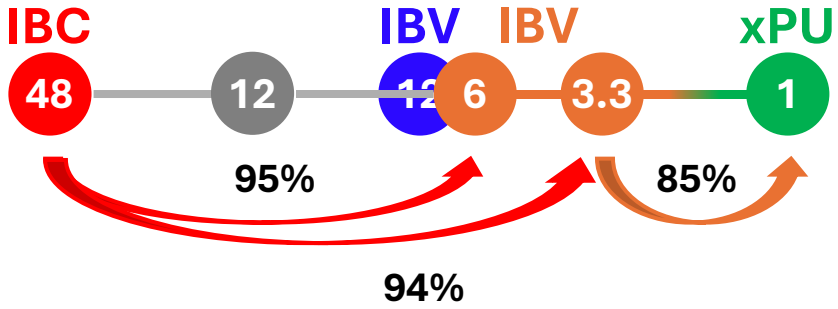


= 80%

VERTICAL Power delivery

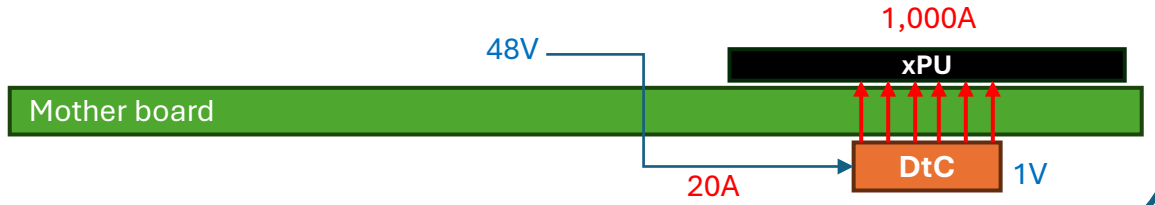
"2-Stage"

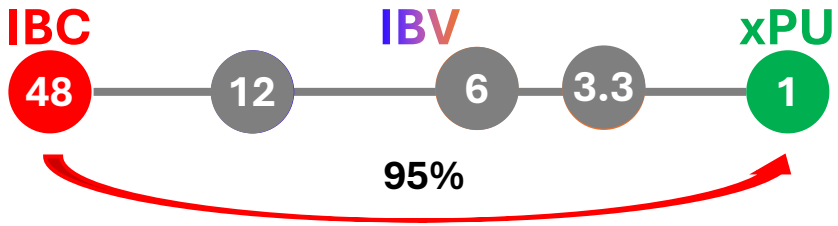




= 80%

"Direct to Chip"

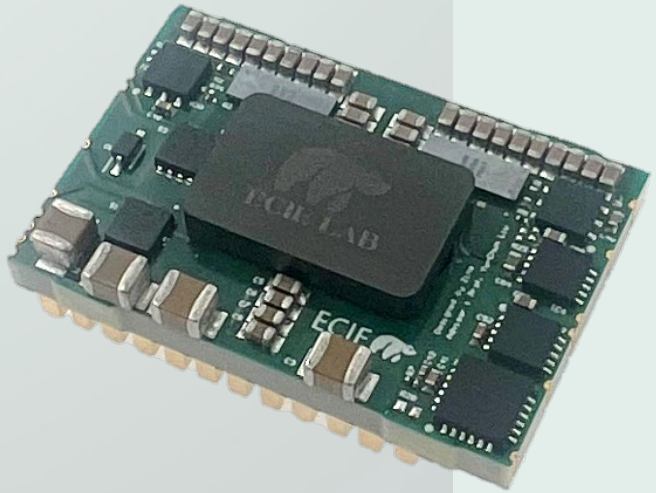




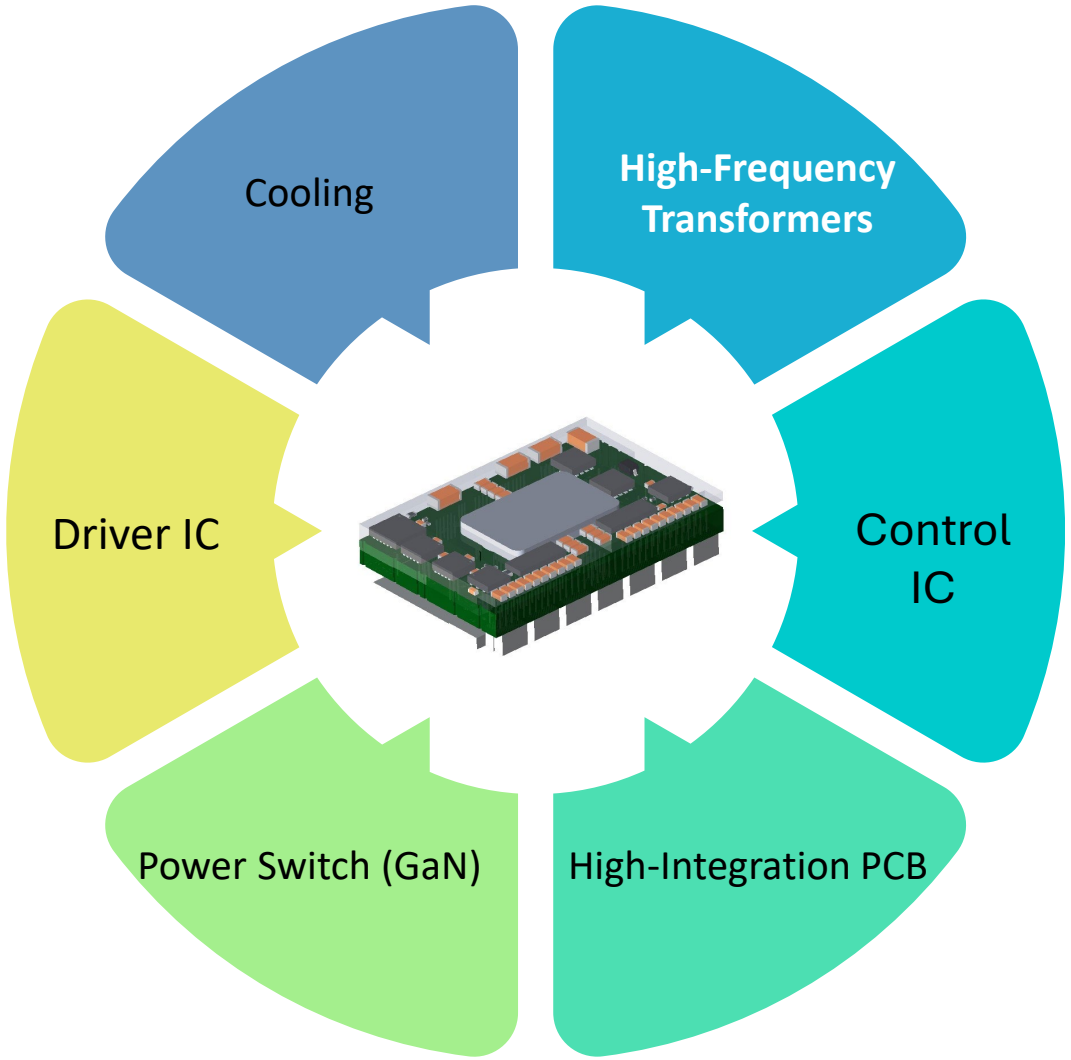
= 95%

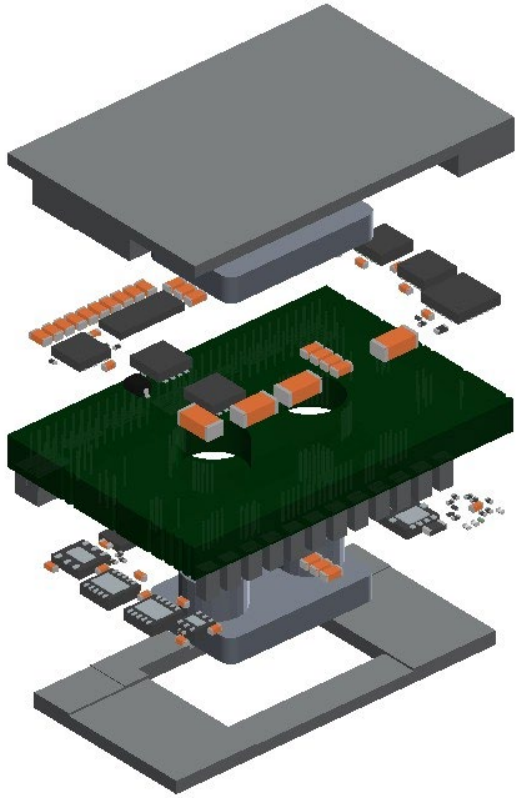
[Ref] Direct to chip (DtC) DC-DC converters for AI chips, José A. Cobos, APEC2025.

Design and Implementation of a 1-kW High-Frequency High-Efficiency Intermediate Bus Converter for AI Server Applications



48V/12V 1kW Non-Isolated LLC converter





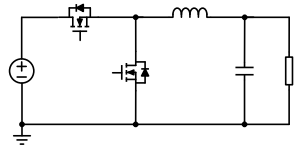
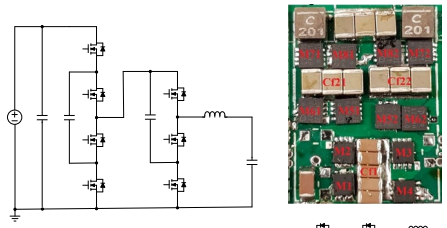
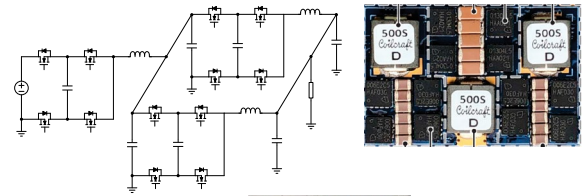
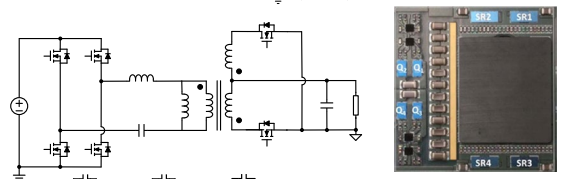
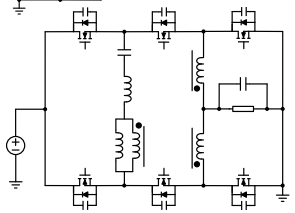
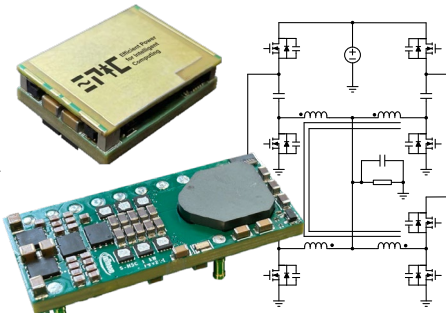
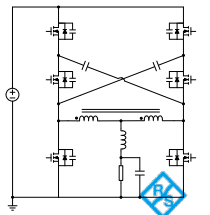
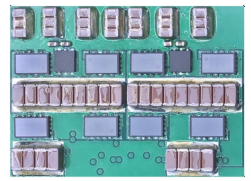
- Efficiency
- High Gain
- Gain regulation
- A/μs
- Flatness
- Cost

48V-12V Topology Comparison

- Transformer-less topologies are dominated by conduction loss and often require 10 or more parallel switches to achieve high efficiency.

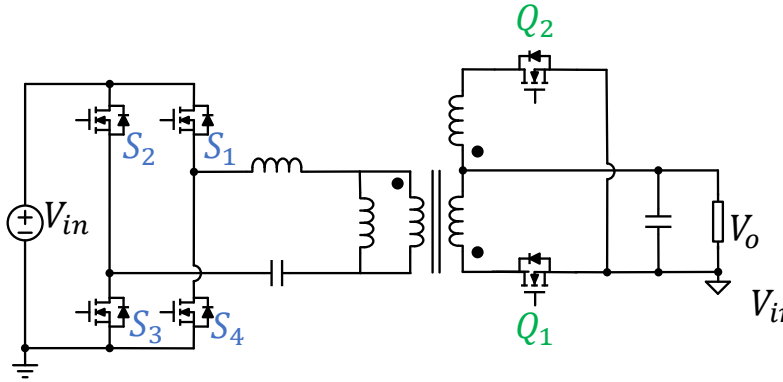
48V-12V topology

- without transformer
  - Buck converter [1][2]
  - Zero-Inductor Voltage Converter[3][4][5]
  - Resonant Switched-Capacitor Converter[6][7][8]
- with transformer
  - LLC Converter[9][10]
  - Non-isolate LLC Converter [11][12][13]
  - Symmetric Hybrid Switched capacitor Converter(SHSC)[14]
  - Switched Capacitor Buck Converter (SCB)[15][16][17]

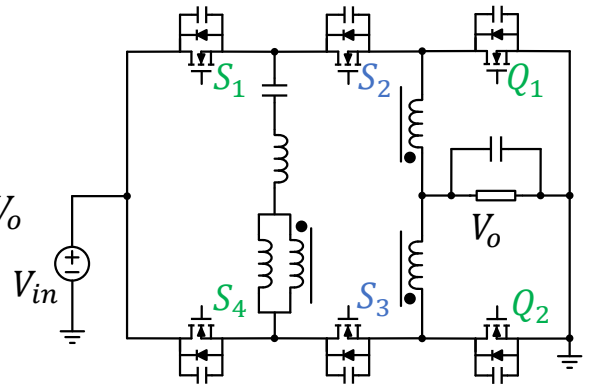









Analysis Summary-Voltage stress comparison

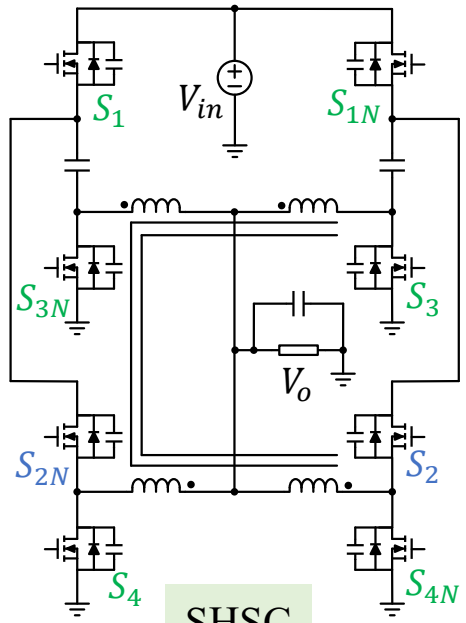
- The design targets 48V input and 12V output.
- Except for the LLC, the other three topologies have similar switch stress.



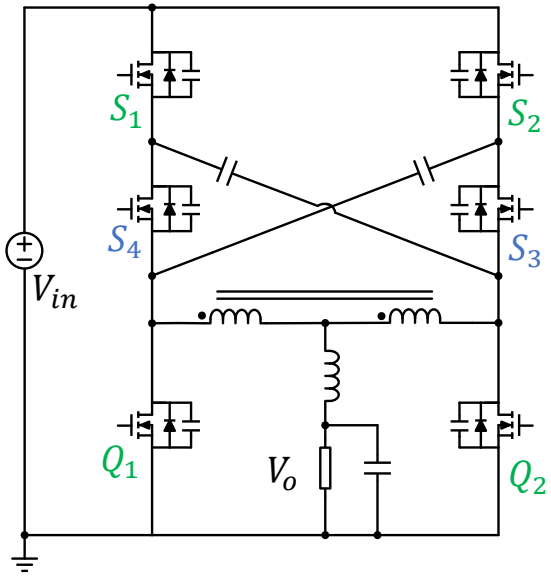
LLC



Non-isolate LLC



SHSC



SCB

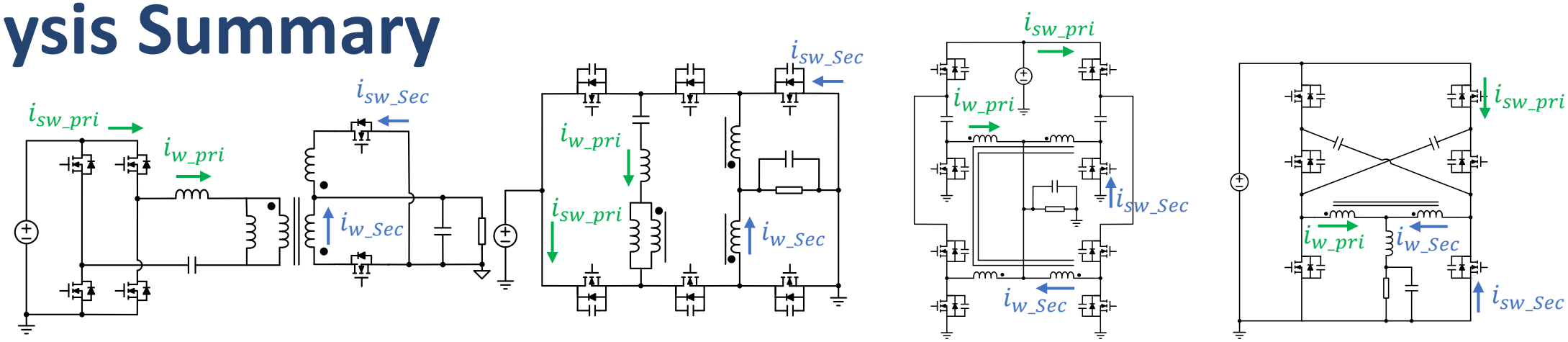
Parameters	Voltage Stress
$S_1 \sim S_4$	V_{in}
Q_1/Q_2	$\frac{V_{in}}{2}$
Number of switches	6

Parameters	Voltage Stress
S_1/S_2	$\frac{V_{in}}{2}$
S_3/S_4	V_{in}
Q_1/Q_2	$\frac{V_{in}}{2}$
Number of switches	6

Parameters	Voltage Stress
S_1/S_{1N}	$\frac{V_{in}}{2}$
S_2/S_N	V_{in}
S_3/S_{4N} S_3/S_{4N}	$\frac{V_{in}}{2}$
Number of switches	8

Parameters	Voltage Stress
S_1/S_2	$\frac{V_{in}}{2}$
S_3/S_4	V_{in}
Q_1/Q_2	$\frac{V_{in}}{2}$
Number of switches	6

Analysis Summary

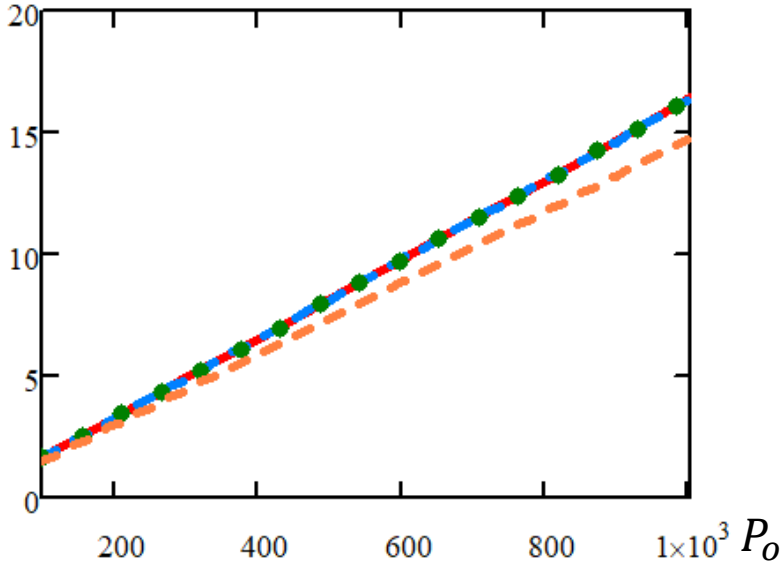


Topology Name	LLC	Non-isolate LLC	SHSC	SCB
Primary switch current i_{sw_pri}(RMS)	$\frac{I_{o\_AVG}\pi\frac{N_1}{N_P}}{4}$	$\frac{I_{o\_AVG}\pi}{4\,(\frac{N_P}{N_1}+2)}$	$\frac{I_{o\_AVG}\pi}{8\frac{N_2}{N_1}+8}$	$\frac{I_{o\_AVG}}{2\sqrt{2}(\frac{N_1}{N_2}+1)}$
Secondary Switch Current i_{sw_sec}(RMS)	$\frac{I_{o\_AVG}\pi}{4}$	$\frac{I_{o_{AVG}}\pi(\frac{N_P}{N_1}+1)}{4(\frac{N_P}{N_1}+2)}$	$\frac{I_{o\_AVG}\pi}{4\frac{N_2}{N_1}+4}$	$\frac{I_{o\_AVG}(\frac{N_1}{N_2}+\frac{1}{2})}{\sqrt{2}(\frac{N_1}{N_2}+1)}$
Primary winding current i_{w_pri}(RMS)	$\frac{I_{o\_AVG}\pi\frac{N_1}{N_P}}{2\sqrt{2}}$	$\frac{I_{o\_AVG}\pi}{2\sqrt{2}(\frac{N_P}{N_1}+2)}$	$\frac{I_{o\_AVG}\pi}{\sqrt{2}(4\frac{N_2}{N_1}+4)}$	$\frac{I_{o\_AVG}}{\frac{N_1}{N_2}+1}$
Secondary winding current i_{w_sec}(RMS)	$\frac{I_{o\_AVG}\pi}{4}$	$\frac{\pi\sqrt{{I_{o\_AVG}}^2(2{N_1}^2+2N_1N_P+{N_P}^2)}}{8(2N_1+N_P)}$	$\frac{I_{o\_AVG}\pi}{\sqrt{2}(4\frac{N_2}{N_1}+4)}$	$\frac{I_{o\_AVG}}{\frac{N_1}{N_2}+1}$
All switch ZVS	yes	yes	yes	no

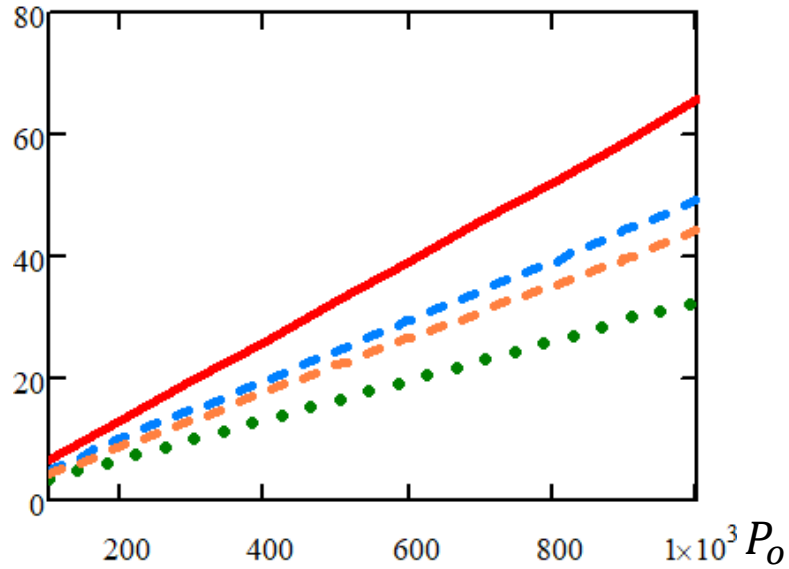
Topology comparison

- Under the condition of a 12V output voltage, the RMS currents of switches and windings in four topologies are compared.
- In switch current comparison, the SHSC performs better.
- In winding current comparison, the SHSC topology also shows superior performance.

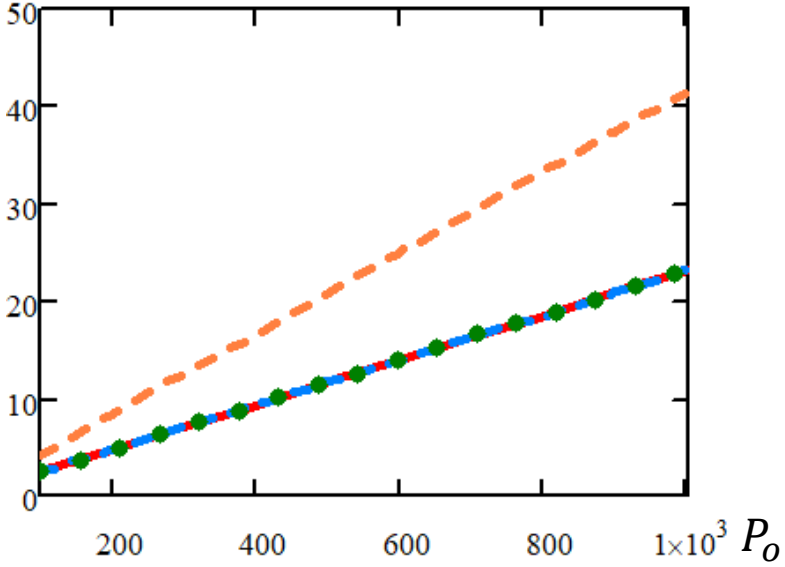
Primary switch current RMS value(A)



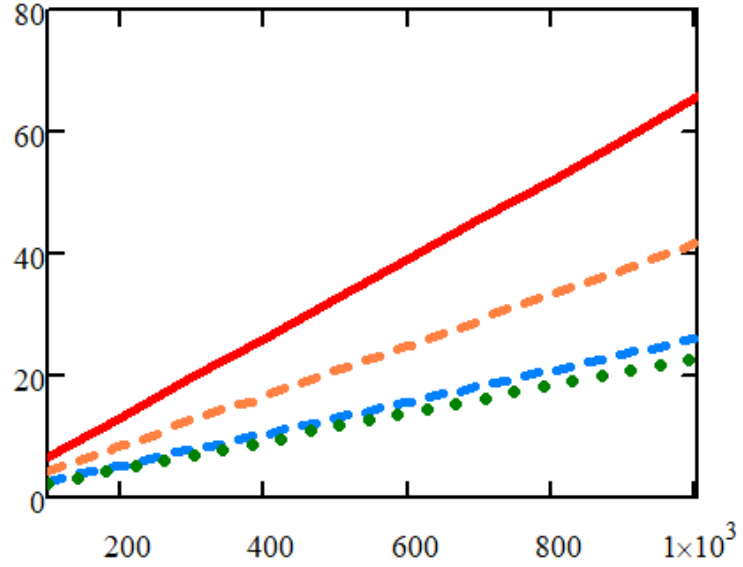
Secondary switch current RMS value(A)

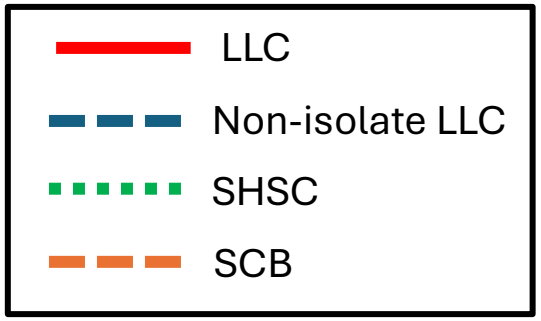


Primary winding current RMS value(A)



Secondary winding current RMS value(A)

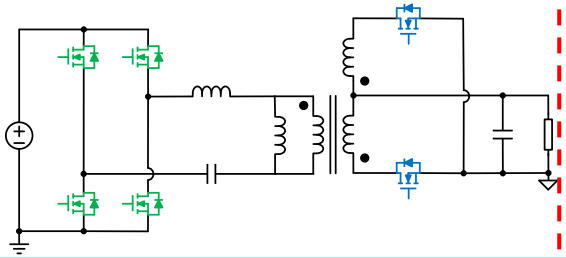


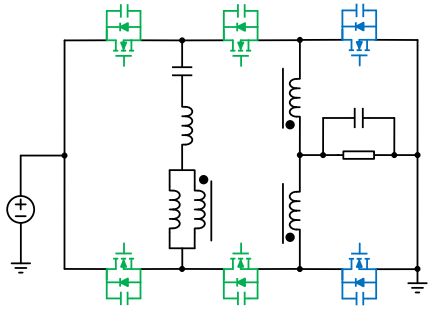


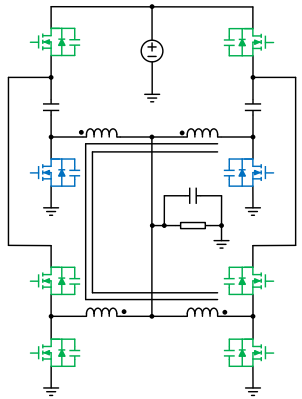
Topology comparison

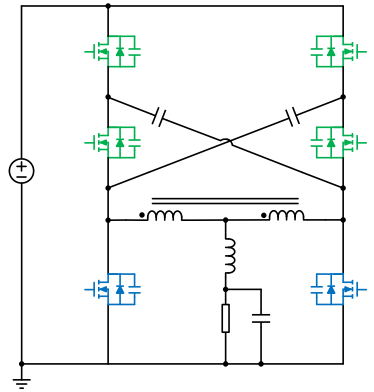
- To achieve high power density, a higher frequency is needed to reduce transformer size. Due to varying input voltage requirements, architecture Non-isolate LLC was chosen for this design.

Primary switch
Secondary switch





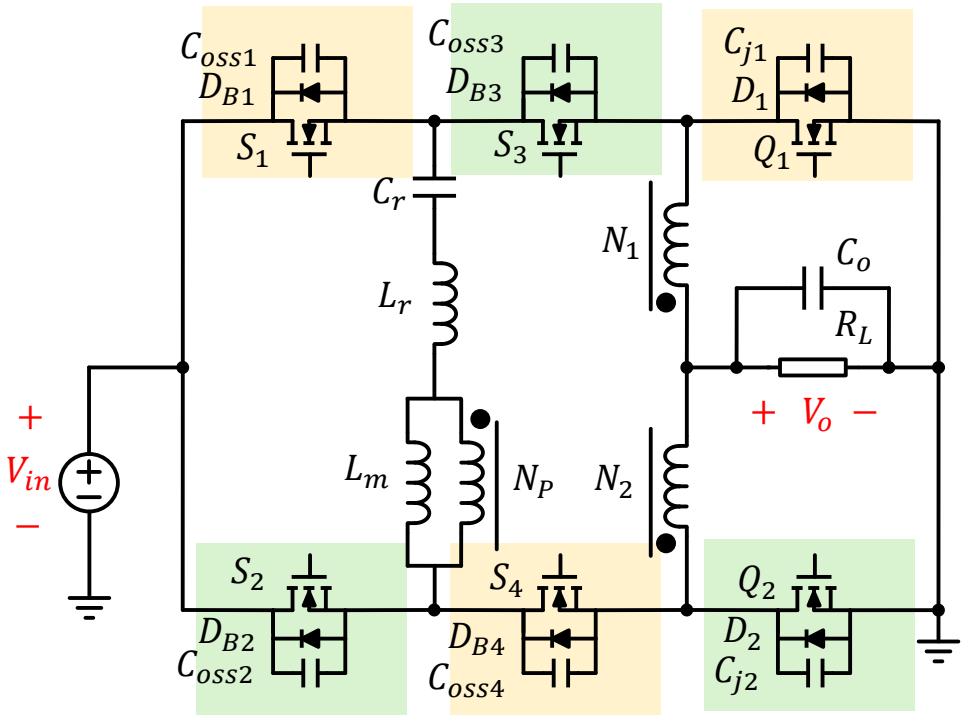




Topology	LLC	Non-isolate LLC	SHSC	SCB
Benefit	• All switches ZVS • Secondary switches ZCS • Primary-secondary isolation	• All switches ZVS • Secondary switches ZCS • Lower secondary switch/winding current stress than LLC	• All switches ZVS • Partial ZCS for all switches • Minimal switch/winding current stress • Minimal transformer turns	• Secondary switches ZVS • Winding current is near DC, reducing AC losses • Output inductor allows voltage regulation • Minimal transformer turns
Drawback	• Higher switching/winding losses • Max transformer turns	• unrealistic ZCS condition • More transformer turns	• Resonant capacitors have DC bias	• Larger primary side current stress (square wave) • No ZVS on primary switch • No ZCS on secondary switch

Topology comparison

- By analyzing and calculating these losses, the appropriate switches can be identified
- Adjusting dead time or resonance frequency prevents body diode conduction, so its loss are ignored.

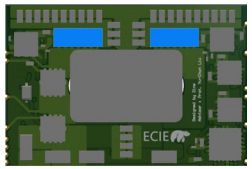


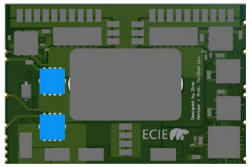
Item	Equation
Conduction loss	$I_{sw\_RMS}{}^2 \cdot R_{ds\_on}$

Item	Equation
T_{off} loss	$\frac{V_{stress}\frac{N_P I_{Lm\_max}}{N_P+N_2}}{2}\left(\frac{Q_{\mathrm{gd}}}{V_{plt}}+C_{iss}\ln\frac{V_{plt}}{V_{\mathrm{th}}}\right)R_g f_s$

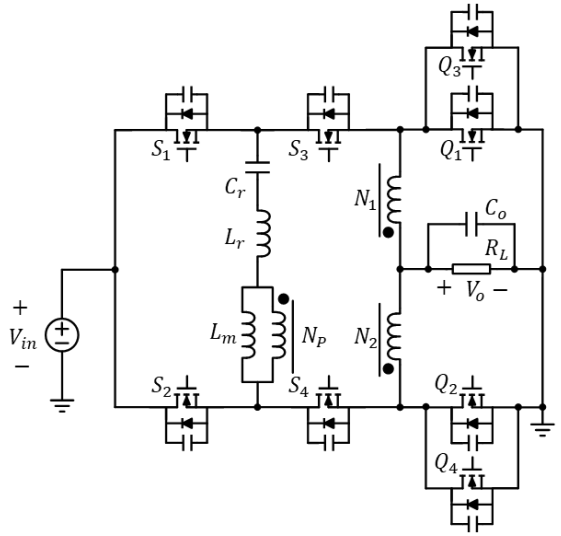
Item	Equation
Driver loss	$\frac{1}{2}Q_g V_{DRV} f_s$

Topology comparison

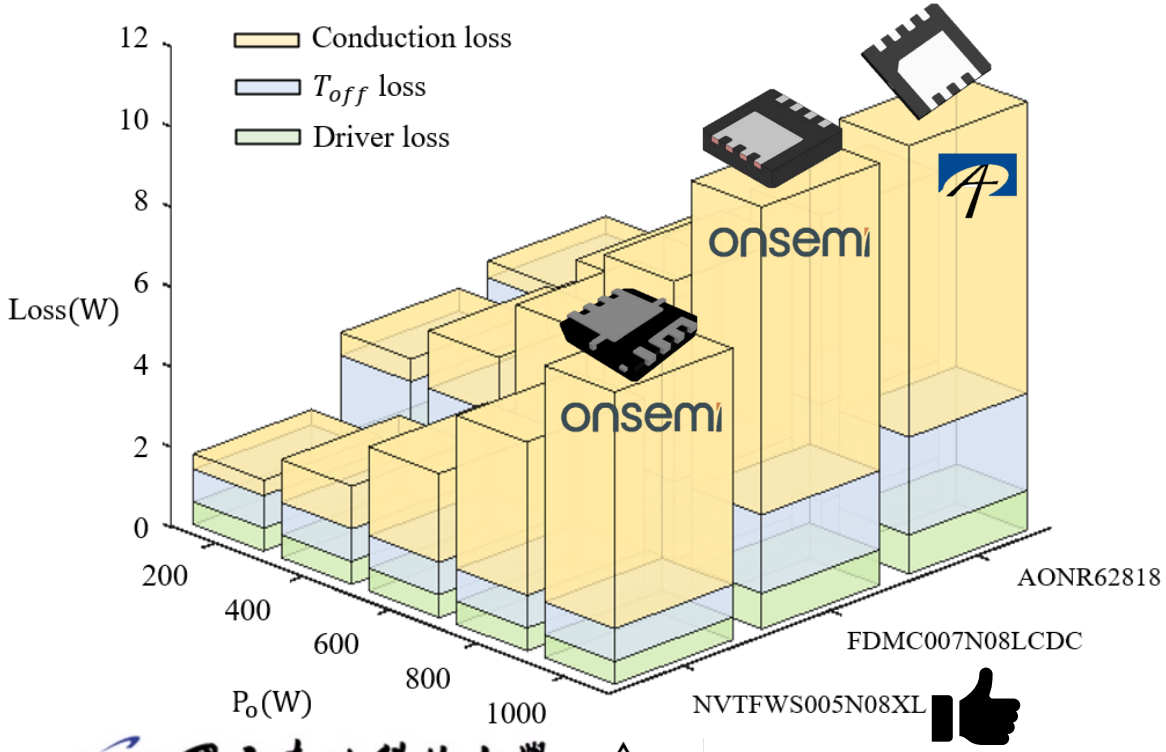




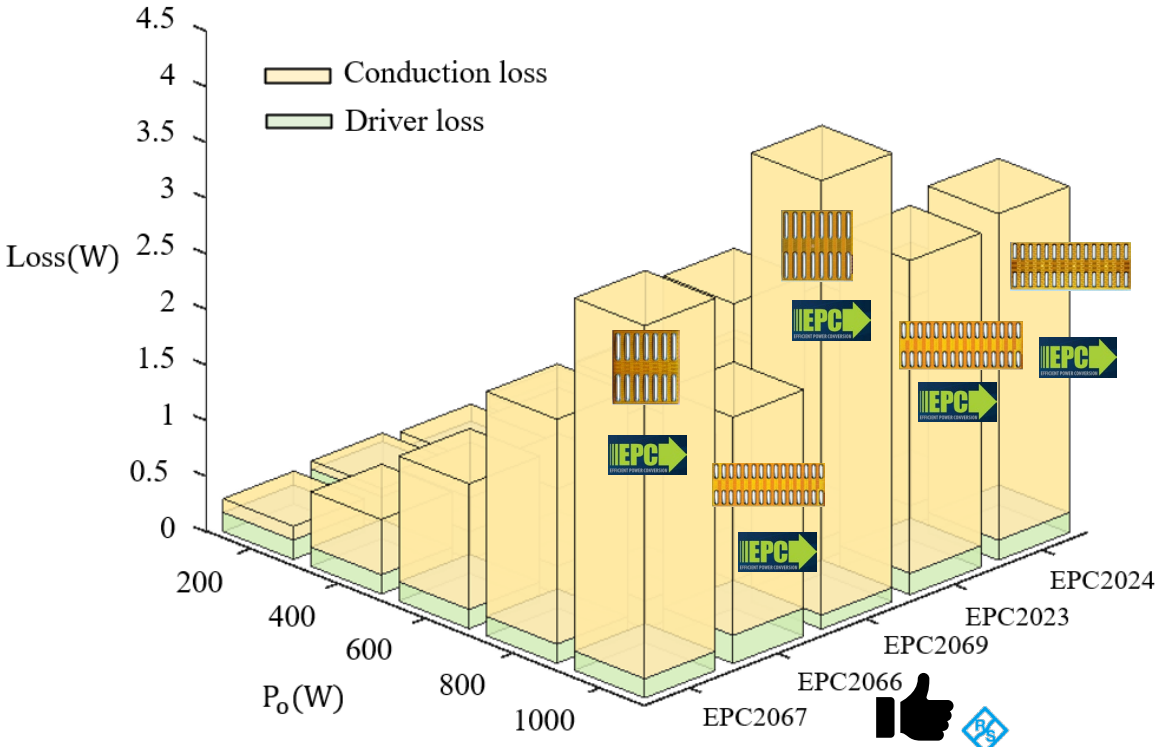
- Since switches S_3 and S_4 experience higher voltage stress, switches with higher voltage stress ratings are chosen for the primary-side switches.
- Secondary-side switches Q_1 and Q_2 with higher current ratings are chosen and connected in parallel to reduce conduction loss.



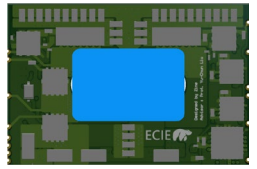
Comparison of Losses in Switches S_1 to S_4



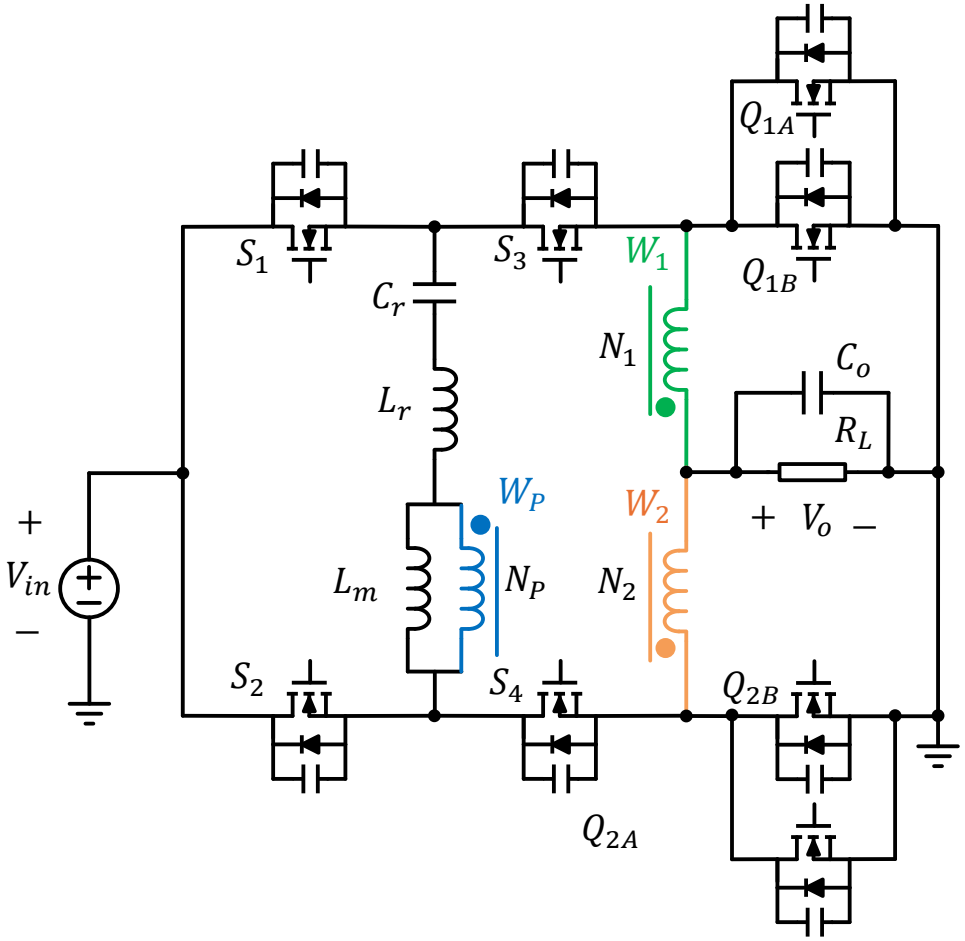
Comparison of Losses in Switches Q_1 to Q_4



PCB Winding Design



- The transformer turns ratio can be determined by the power conversion ratio.
- A two-legs core is used as the basis for PCB winding design.



$$\frac{V_{in}}{V_o} = n + 2$$

$$n = \frac{N_P}{N_1} = \frac{N_P}{N_2}$$

$$N_P : N_1 : N_2 = 2 : 1 : 1$$

Winding W_P diagram

Winding W_1 diagram

Winding W_2 diagram

PCB Winding Design

X_P	10	8	6	4	2
X_1	3	4	5	6	7
X_2	3	4	5	6	7
Equivalent $R_{WP}(R_{dc})$	0.4	0.5	0.66	1	2
Equivalent $R_{W1}(R_{dc})$	0.33	0.25	0.2	0.17	0.14
Equivalent $R_{W2}(R_{dc})$	0.33	0.25	0.2	0.17	0.14
RMS current of winding $W_P(I_{rms})$			1		
RMS current of winding $W_1(I_{rms})$			1		
RMS current of winding $W_2(I_{rms})$			3		
Winding W_P R_{dc} loss	0.4	0.5	0.66	1	2
Winding W_1 R_{dc} loss	0.33	0.25	0.2	0.17	0.14
Winding W_2 R_{dc} loss	3	2.25	1.8	1.5	1.29
Total winding R_{dc} loss	3.73	3	2.66	2.66	3.43

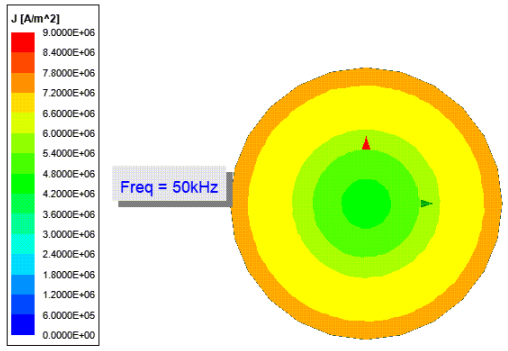
- To achieve high power density, a 16-layer PCB is used to distribute current stress. The parallel layers for windings W_P, W_1, and W_2 being X_P, X_1, and X_2 , respectively.
- Normalized values are used to compare losses under different conditions.
- For the integrated resonant capacitor design, placing the primary winding on the top outer layer is preferred. Considering via usage may reduce its integrity, a 6/5/5 winding configuration is adopted.

PCB Winding Design

- High-frequency current causes skin and eddy effects, concentrating current near the conductor surface.
- Proximity effect causes current to concentrate on adjacent surfaces of two conductors, increasing losses.

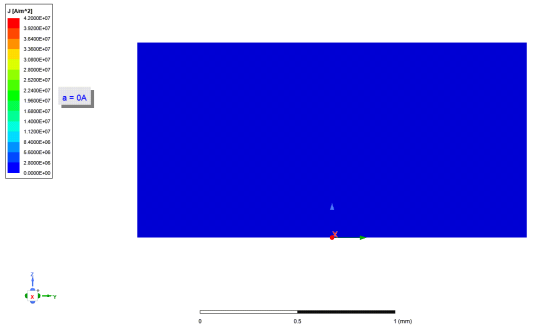
➢ Skin effects

Frequency variation : 50k~1KHz



Items	Spec.
Wire radius	0.5 mm
Wire length	1 mm
Current	5 A

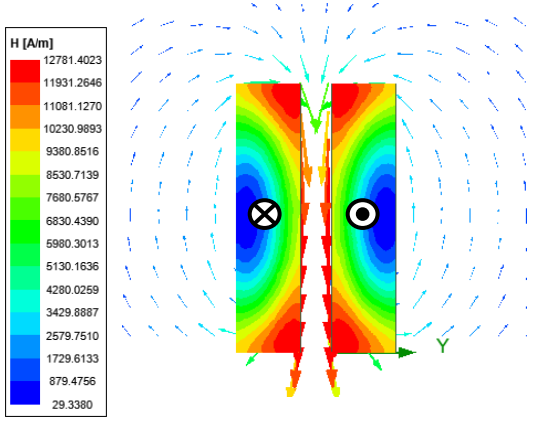
Current Variation : 0~10 A



Items	Spec.
Wire radius	0.5 mm
Wire length	1 mm
frequency	500 kHz

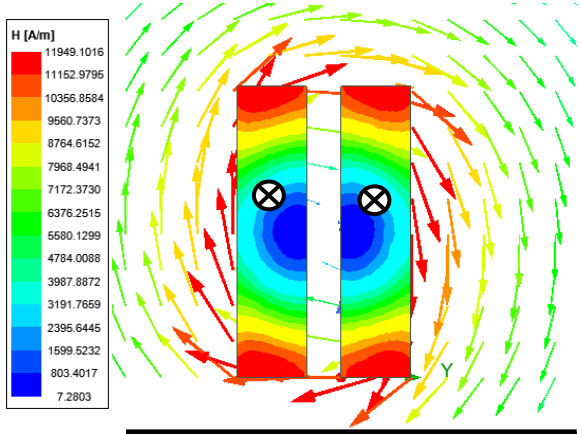
➢ Proximity effects

Different directions of current



Items	Spec.
Current	5 A
frequency	1M Hz

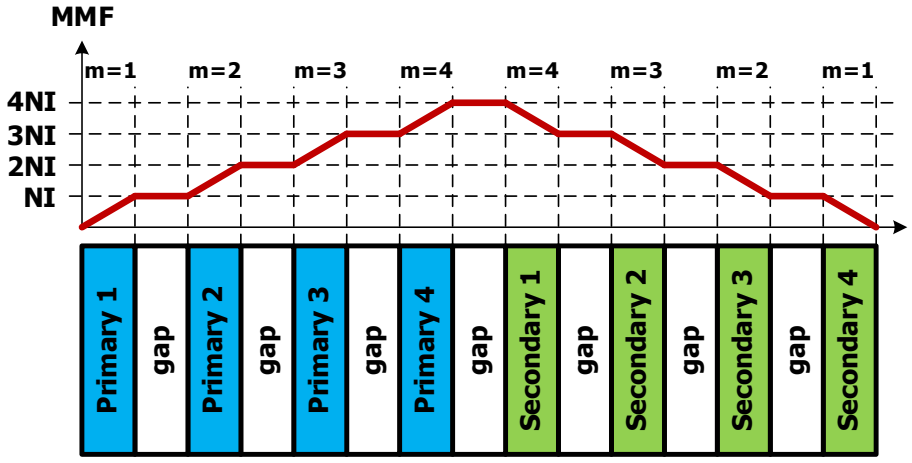
Same directions of current



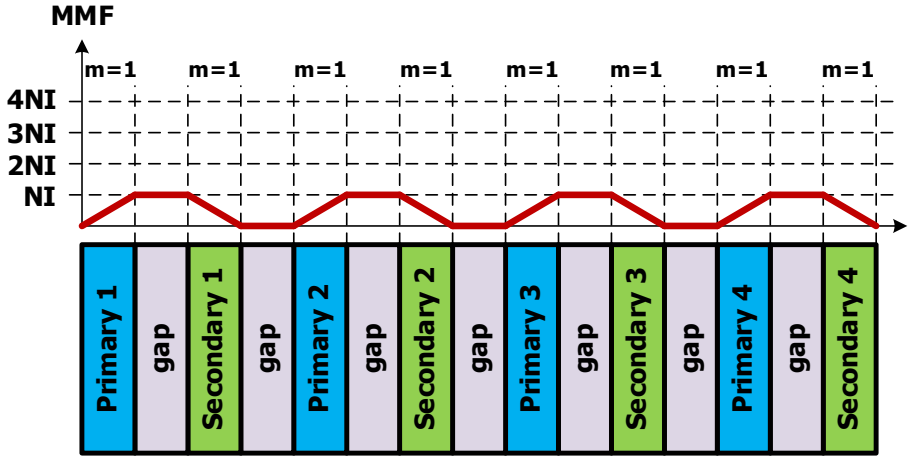
Items	Spec.
Current	5 A
frequency	1M Hz

PCB Winding Design

- Interleaved windings can effectively reduce AC resistance



Non-Interleaved Windings



Interleaved Windings

$$\delta = \frac{1}{\sqrt{\frac{\pi f_s \mu}{\rho}}} \qquad \zeta = \frac{h}{\delta}$$

h : Conductor thickness

δ : Skin depth

$$\text{MMF} = NI = Hl$$

$$m = \left| \frac{\text{MMF}(e)}{\text{MMF}(e) - \text{MMF}(e-1)} \right|$$

$\text{MMF}(e)$: Final value

$\text{MMF}(e-1)$: Starting value

$$R_{ac\_skin} = \frac{\zeta}{2} \frac{\sinh(\zeta) - \sin(\zeta)}{\cosh(\zeta) + \cos(\zeta)} R_{dc}$$

$$R_{ac\_proximtty}(m) = (2m-1)^2 \frac{\zeta}{2} \frac{\sinh(\zeta) - \sin(\zeta)}{\cosh(\zeta) + \cos(\zeta)} R_{dc}$$

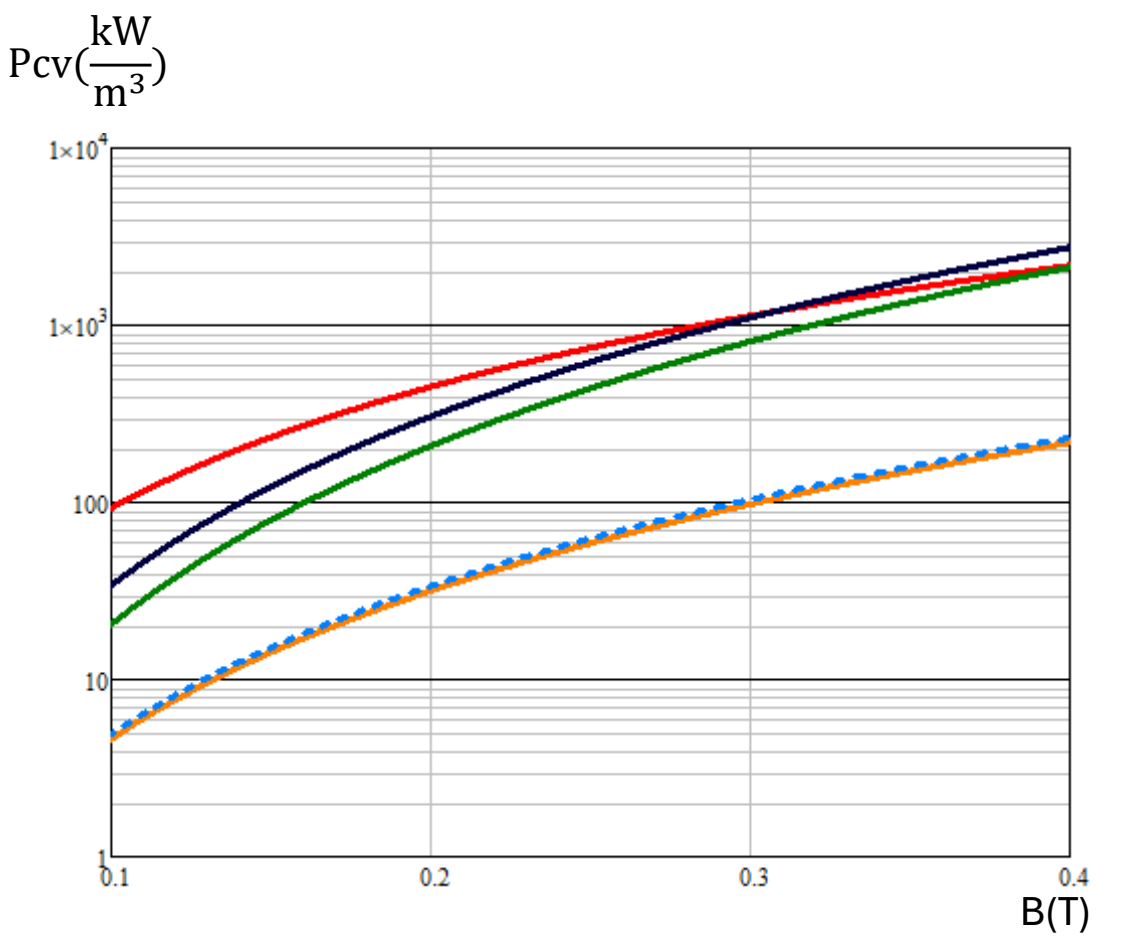
R_{ac_skin} : AC resistance due to the skin effect

$R_{ac\_proximtty}$: AC resistance due to the proximity effect

Total AC resistance $R_{ac\_total} = R_{ac\_skin} + R_{ac\_proximtty}$

R_{ac} loss $= R_{ac\_total} \cdot {I_{rms}}^2$

Transformer Core Design



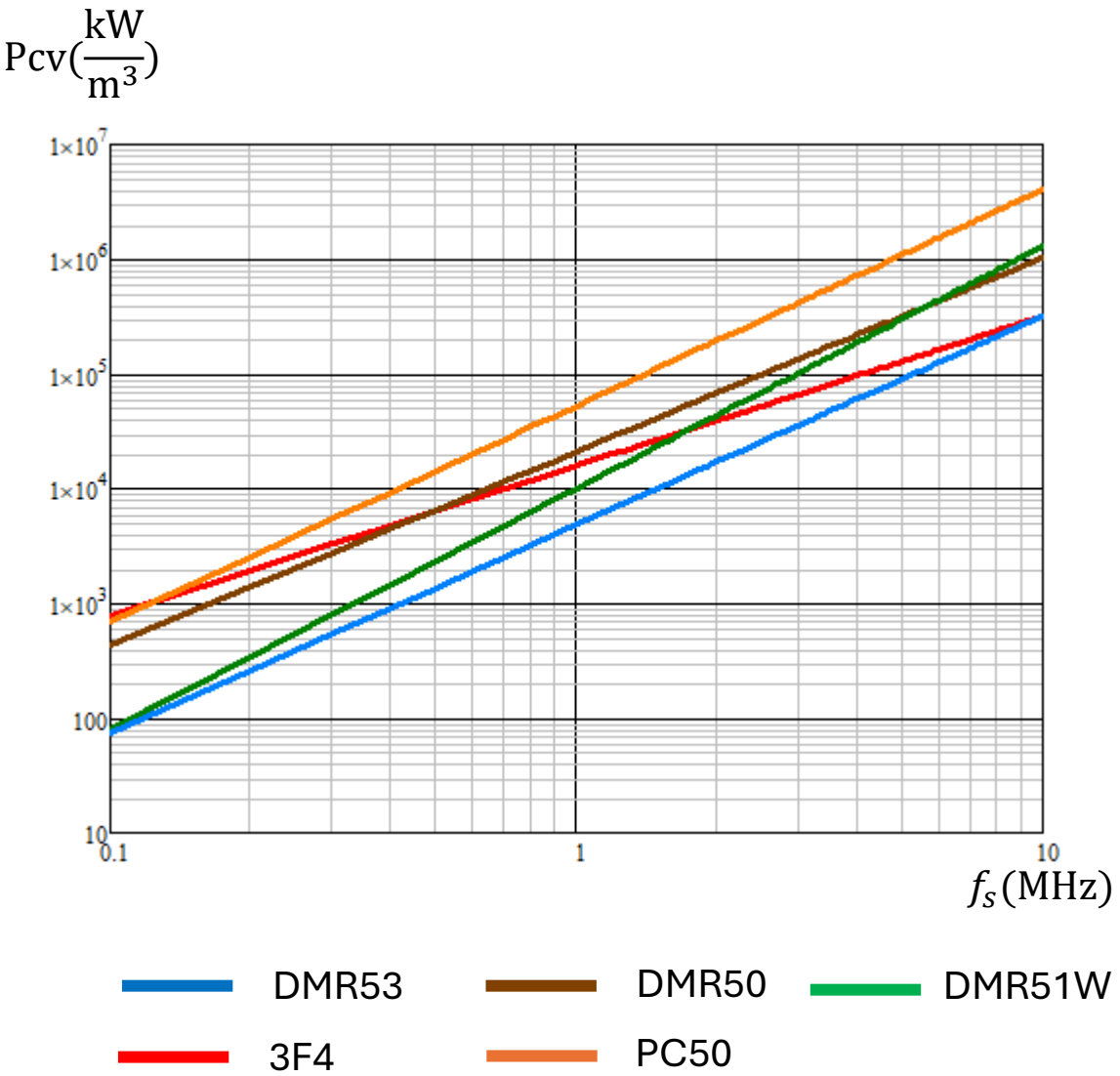
- By comparing the PCV curves of different core materials, the appropriate material can be selected
- Under the calculation condition of a 1 MHz switching frequency, DMEGC's material DMR53 was selected

DMR53 材料特性

DMR53 Material Characteristics

特性 CHARACTERISTICS	测试条件 CONDITIONS		典型值 VALUE
初始磁导率 μi Initial Permeability	10kHz，<0.25mT	25°C	900±25%
饱和磁感应强度 Bs (mT) Saturation Magnetic Flux Density	50Hz，1194A/m	25°C	560
		100°C	460

Transformer Core Design



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DMR53 材料特性

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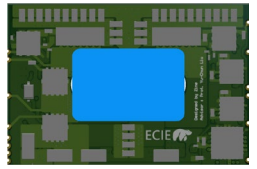
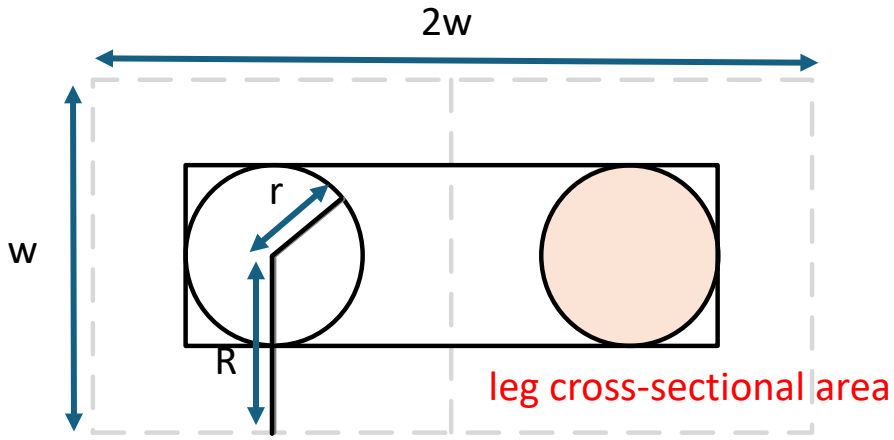
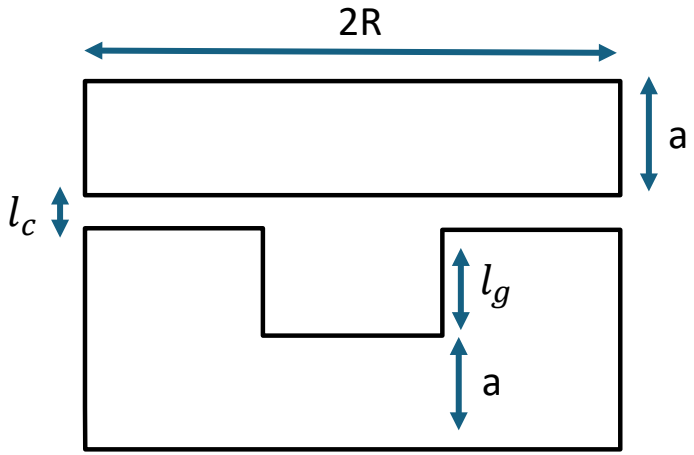
Transformer Core Design





Top view of the UI core



Front view of the UI core

r : Center leg radius R : Winding range l_g : Center leg high

a : Core base thickness l_c : air gap

- Define the relationship Q between the winding range R and the cylinder radius r

$$R = rQ$$

$$w = 2R = 2rQ$$

- To avoid partial saturation of the magnetic flux, the cross-sectional area at the top and bottom of the core must be equal to the cross-sectional area of the cylinder

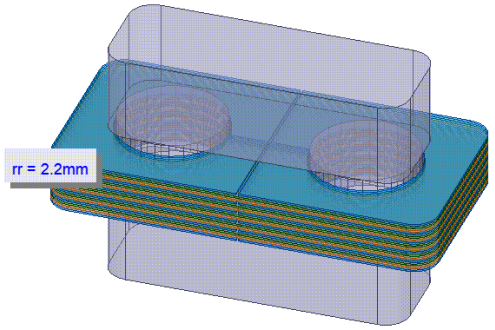
leg cross-sectional area $A_e = \pi r^2 = 2ar$

$$\rightarrow \pi r^2 = a2r$$

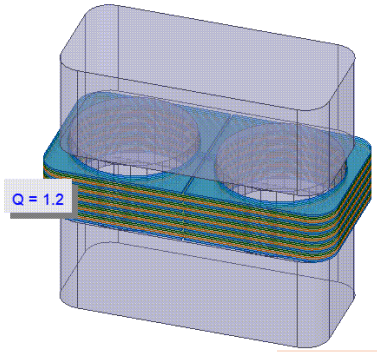
$$\rightarrow a = \frac{\pi r}{2}$$

Transformer Core Design

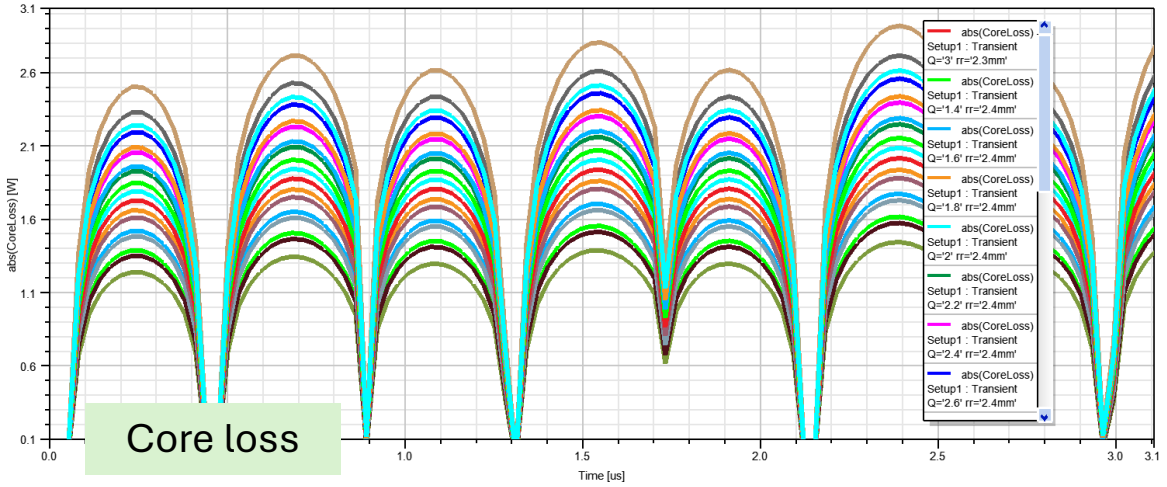
- After optimizing the core to reduce its volume, reparametrize to simulate copper loss and core loss



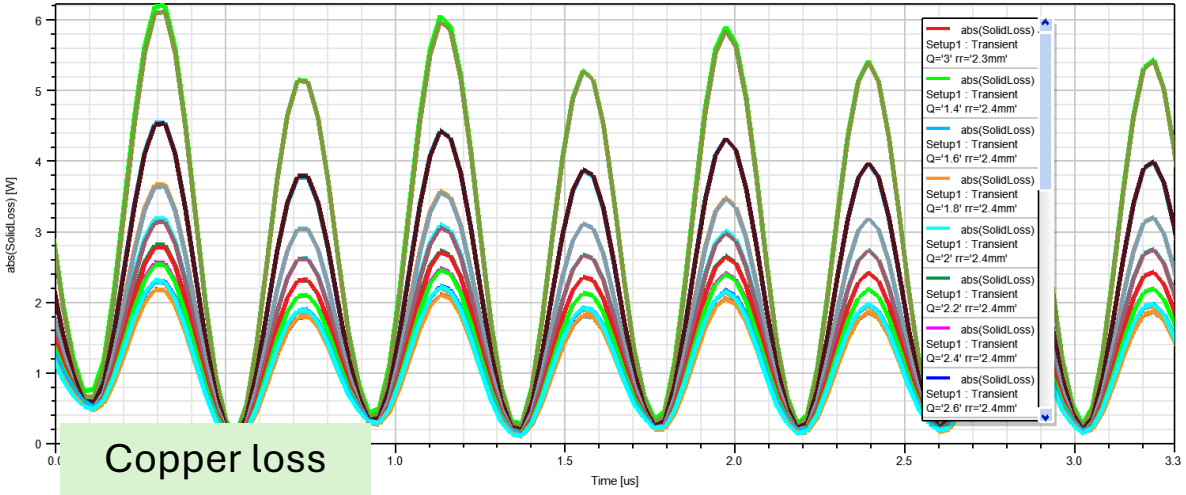
r = 2.2m ~ 3mm



Q = 1.2m ~ 3mm



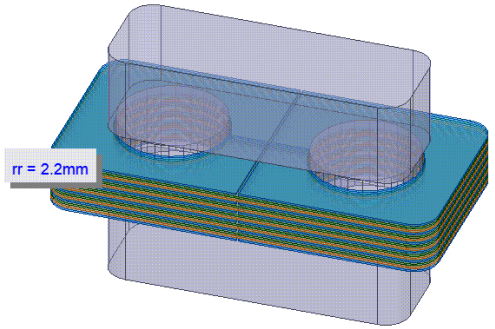
Core loss



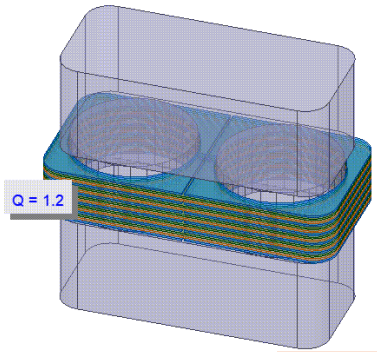
Copper loss

Transformer Core Design

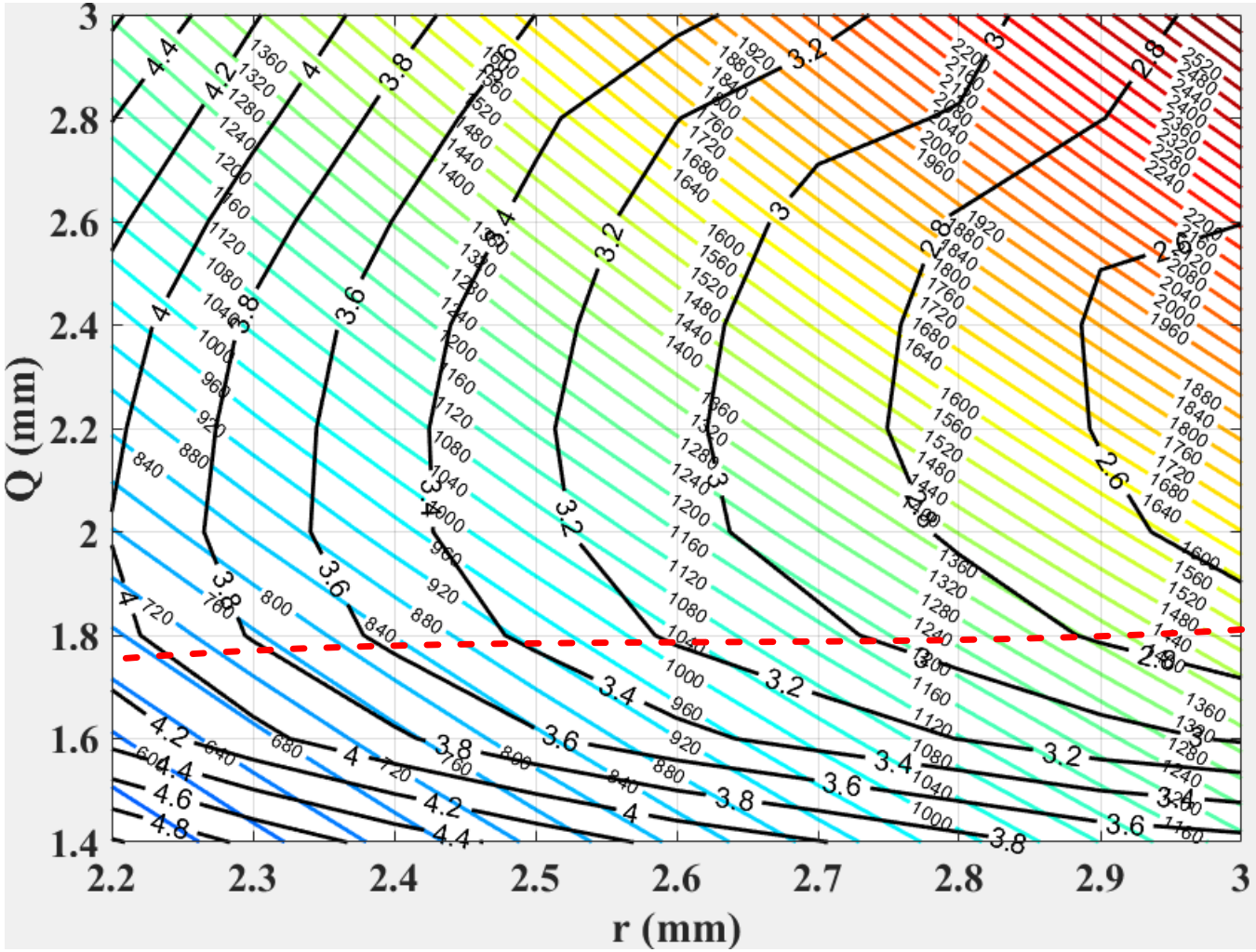
- Use MATLAB to plot the simulated loss results from Maxwell as a contour map corresponding to the volume.



r = 2.2m ~ 3mm

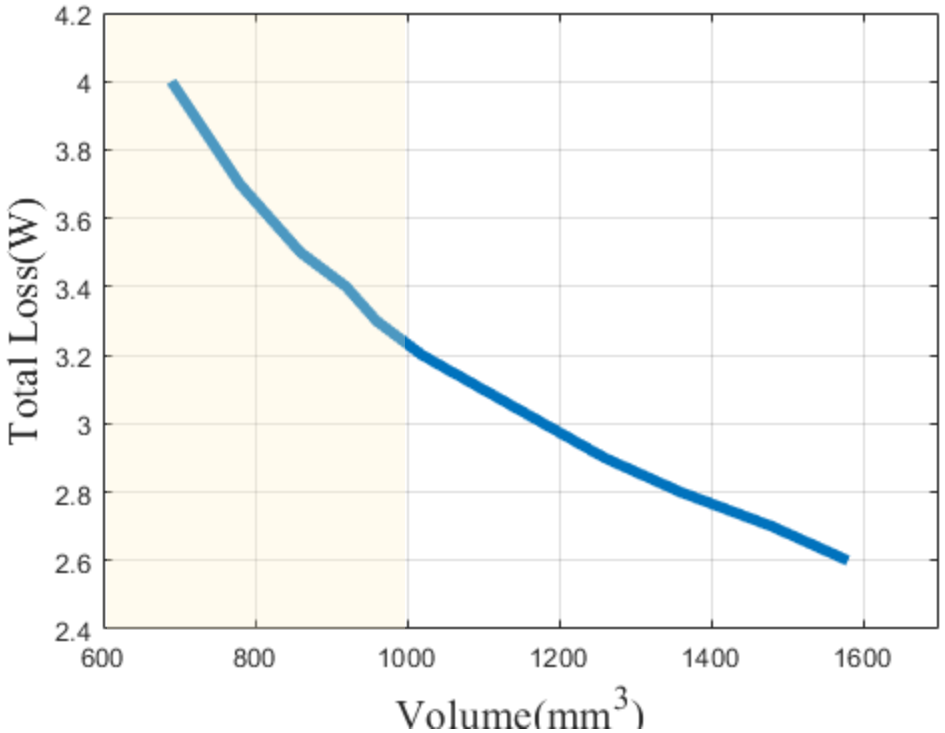


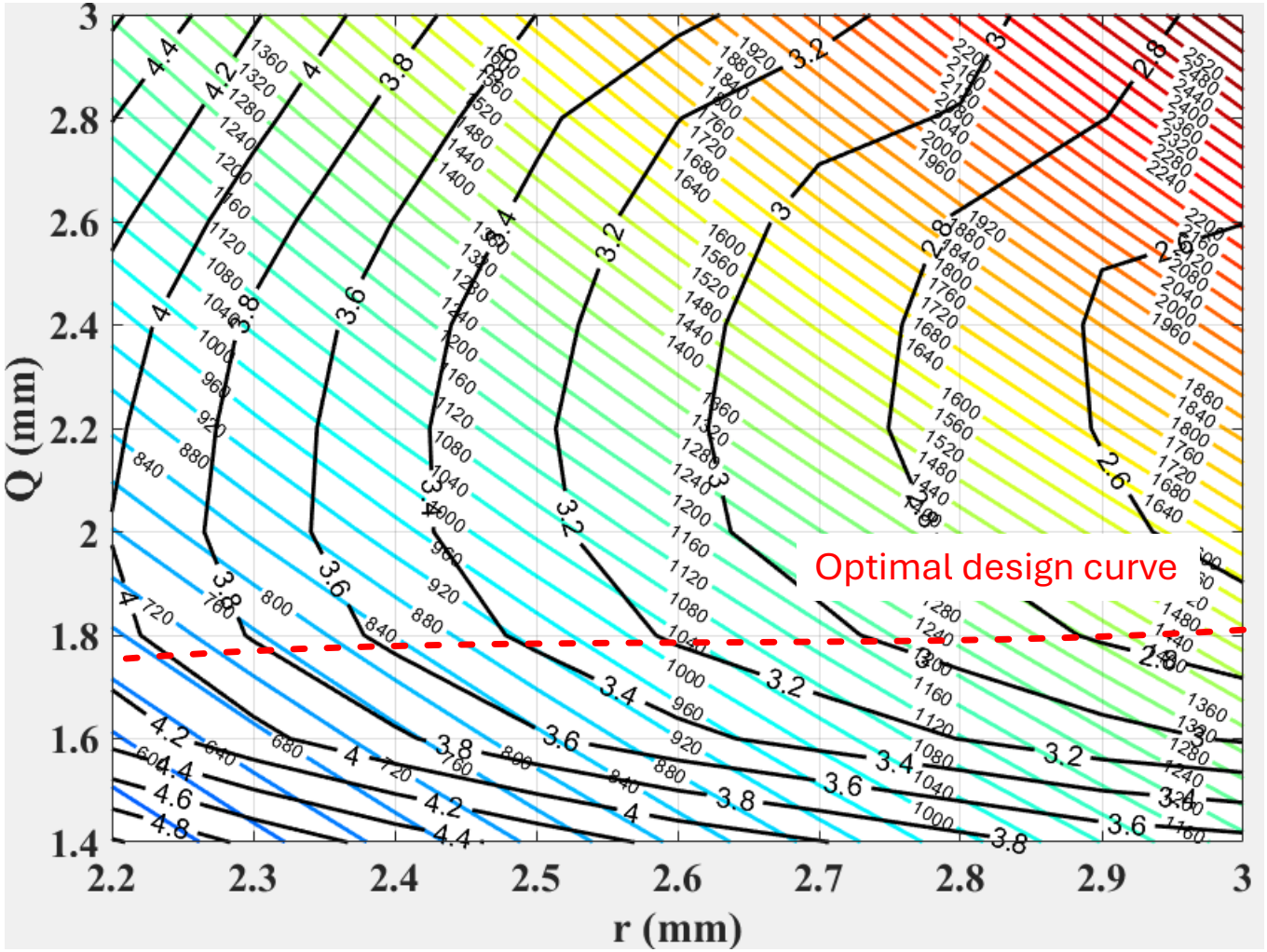
Q = 1.2m ~ 3mm



Transformer Core Design

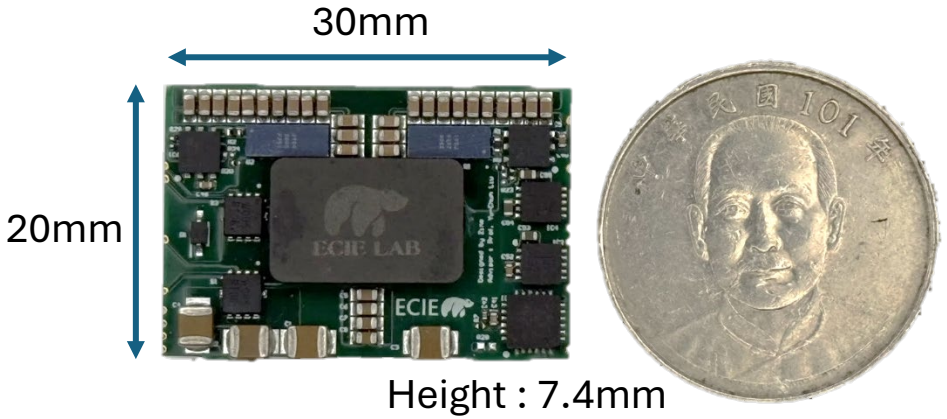
- Plot the optimal total loss curve of the transformer based on the minimum volume for different losses
- Due to power density constraints, a design with a volume less than 1000mm^3 is chosen

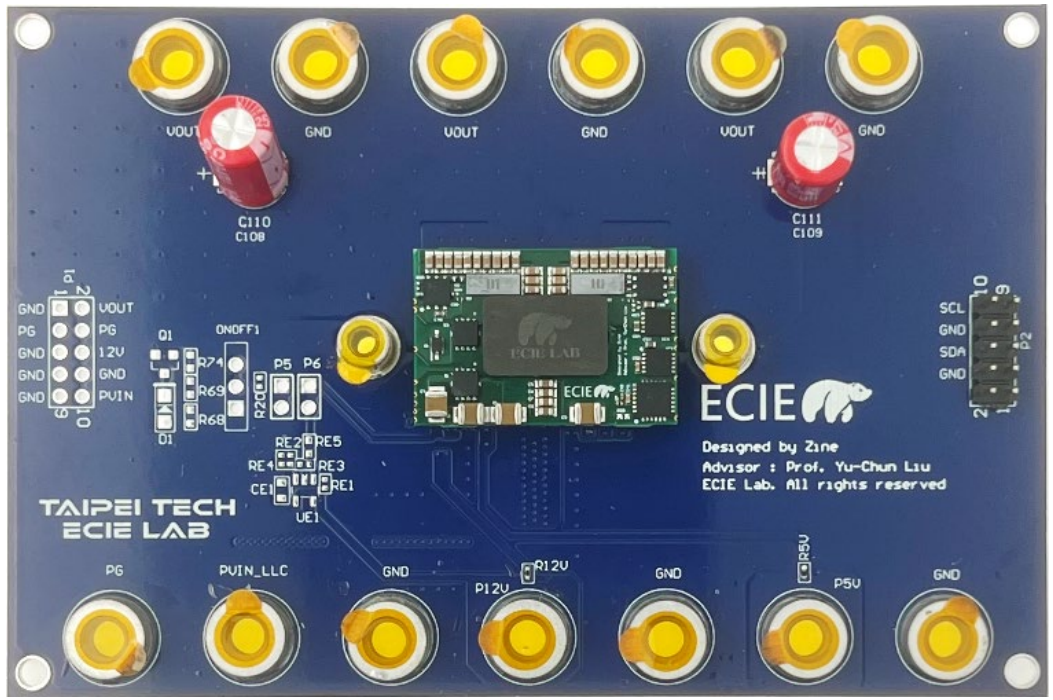




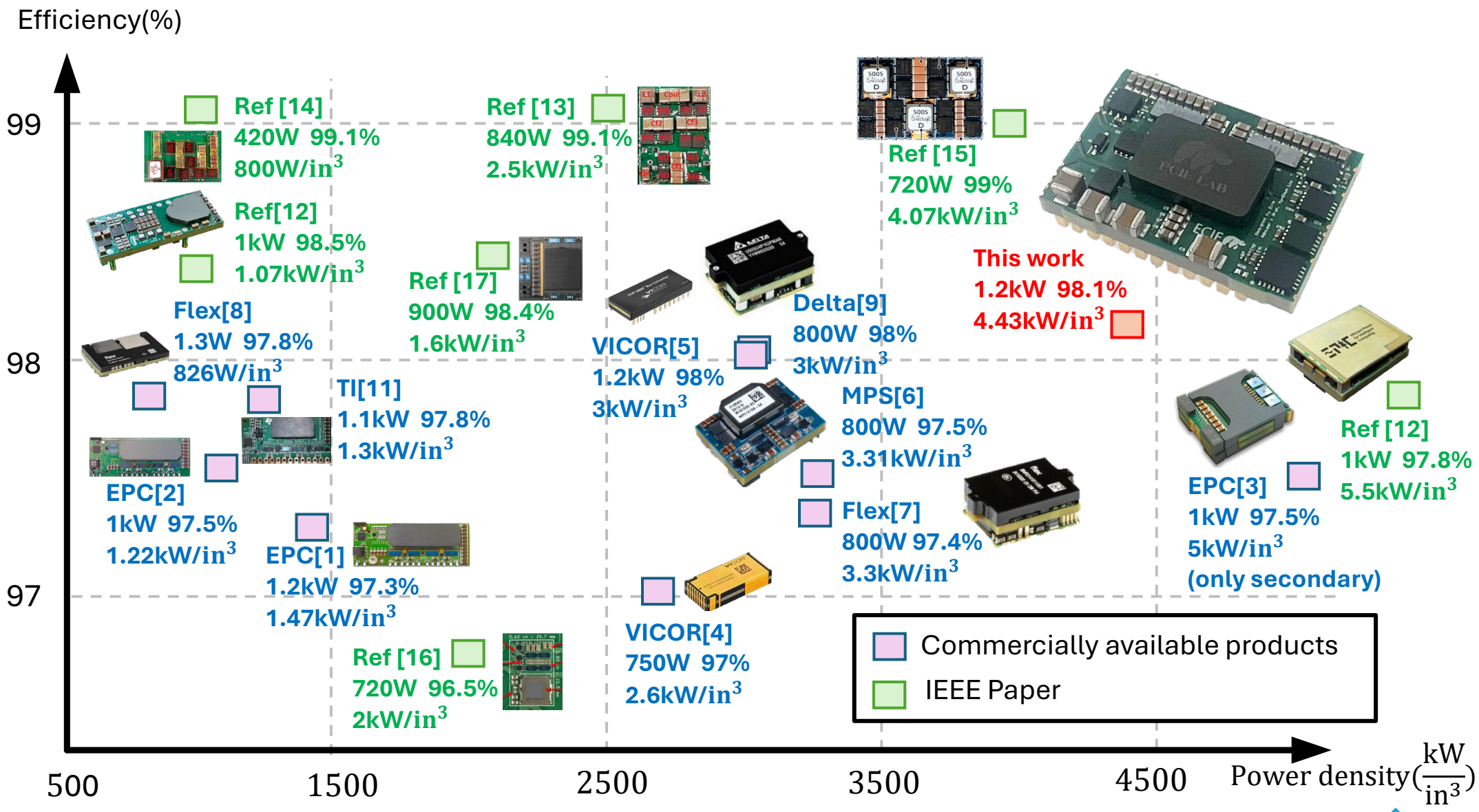
Experimental Verification

Parameters	Specifications
Input Voltage	40-60Vdc
Output Voltage	10-15Vdc
Output Power	1200W
Switching Frequency	1.08MHz
Peak Efficiency	98.11%
Length / Width / Height	30mm/20mm/7.4mm
Power Density	>4430 W/in^3



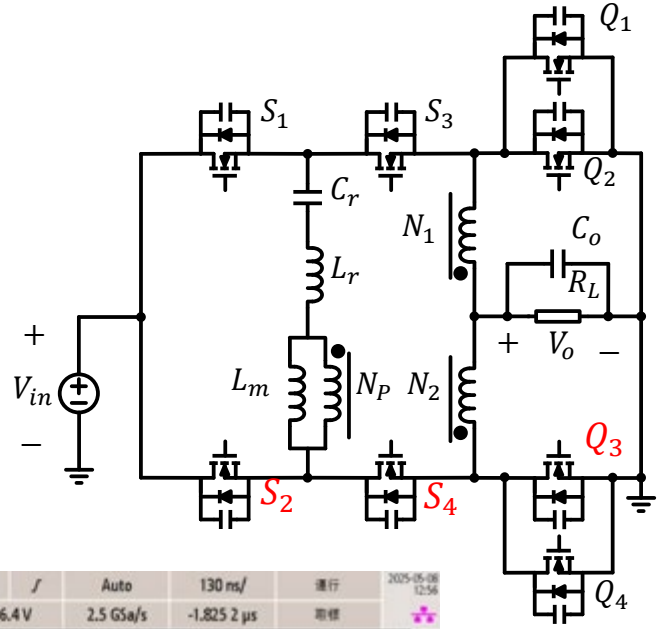


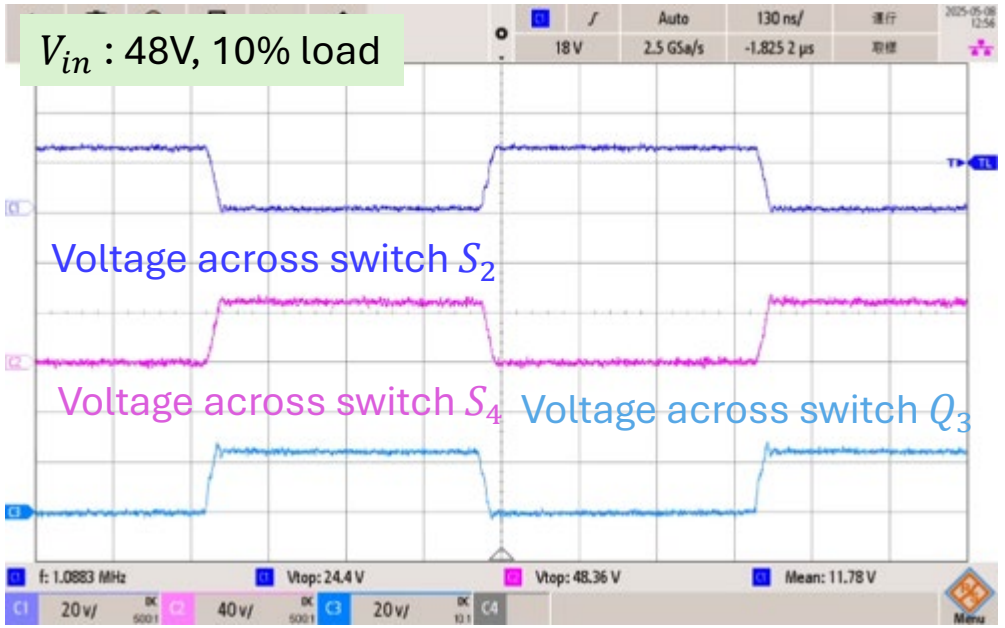
Experimental Verification

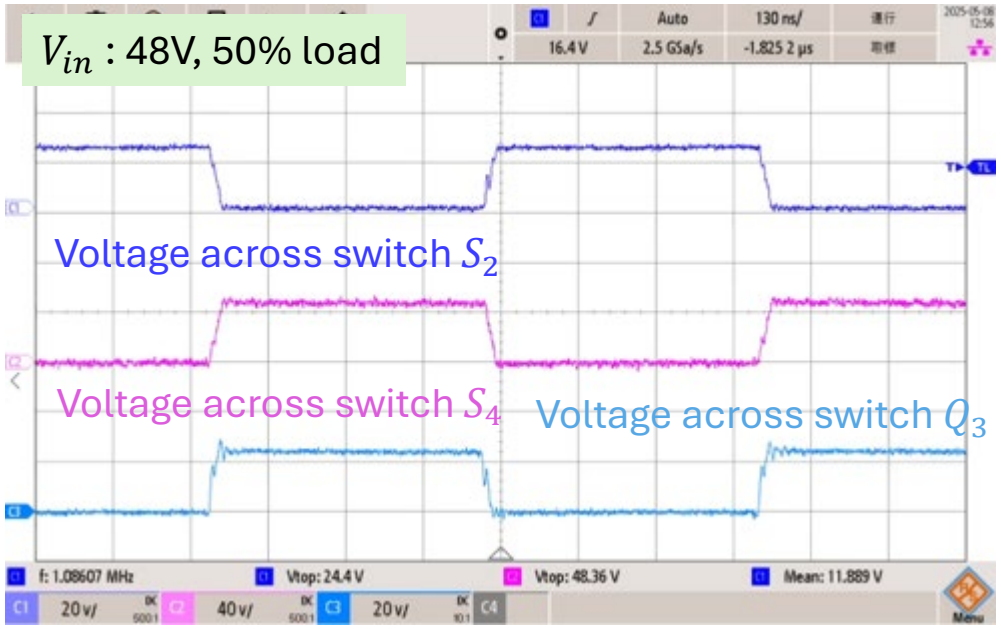


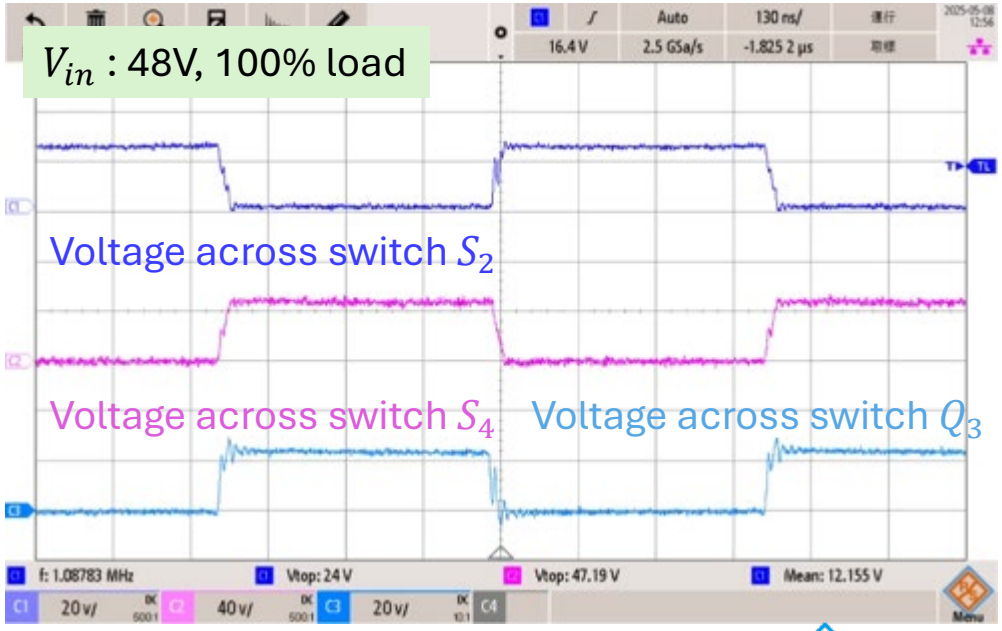
Experimental Verification

- With a 48V input, 30 ns dead time, and 1.08 MHz switching frequency
- ZVS is achieved under all load conditions.





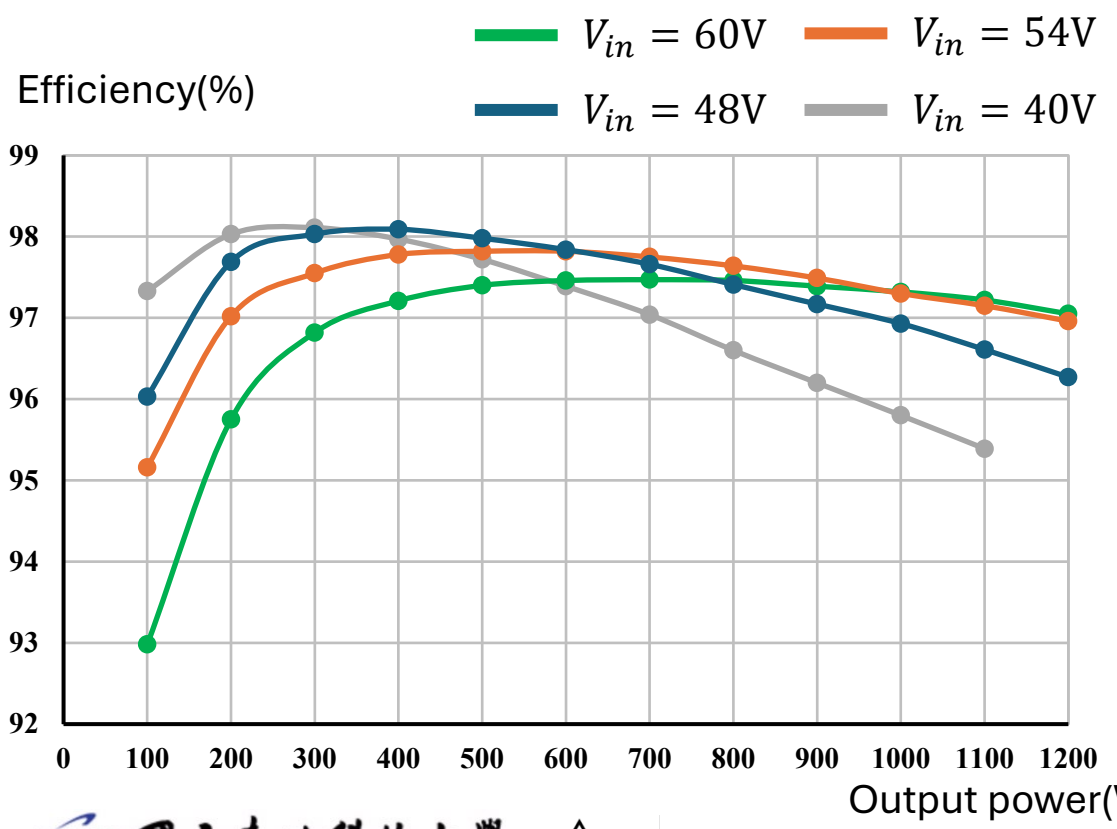


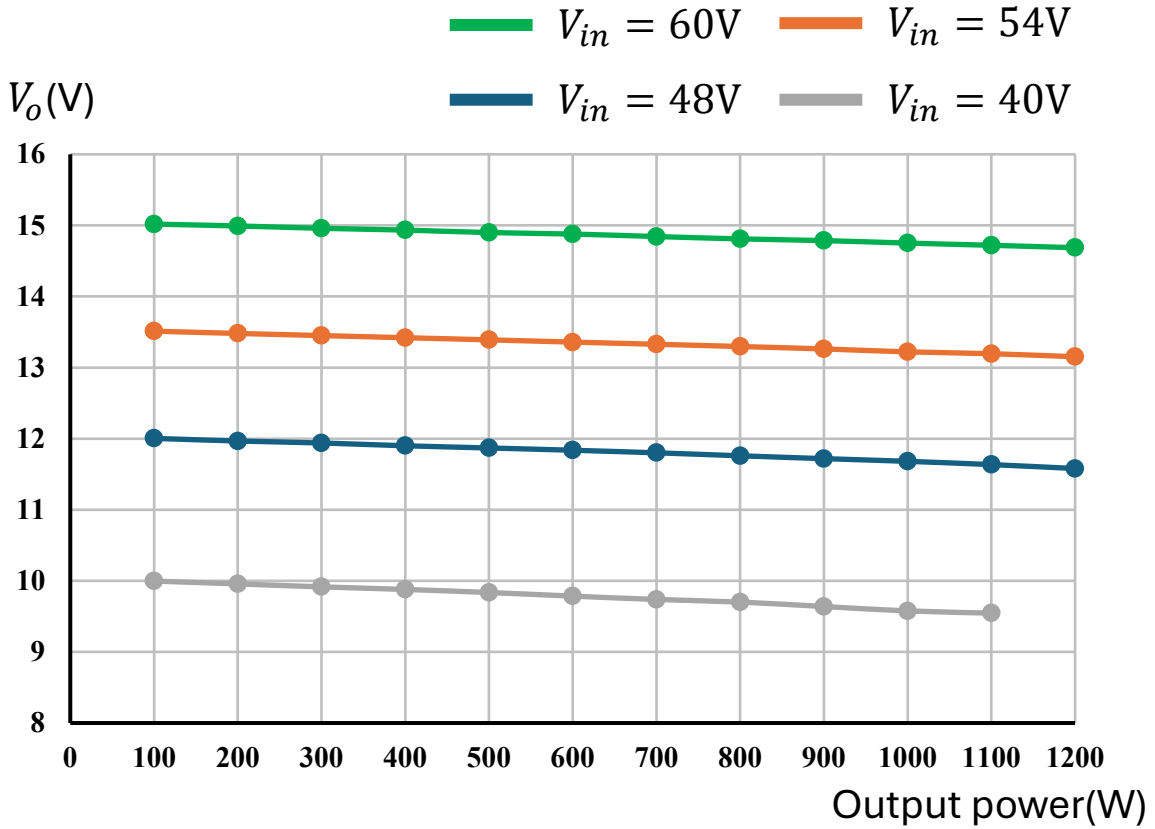


Experimental Verification

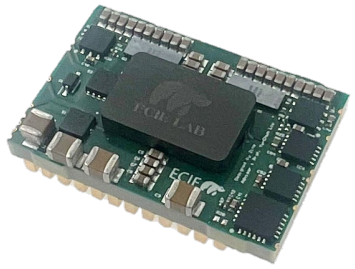
- Due to excessive temperature, the input of **40V** was only tested up to **1100W**.
- The peak efficiency reached **98.11%**.
- The switching frequency was **1.08 MHz**.

V_{in}	40V	48V	54V	60V
Peak Efficiency	98.11%	98.10%	97.82%	97.47%
Full Load Efficiency	95.39%	96.27%	96.96%	97.05%
V_o(10% load)	9.99V	12V	13.51V	15.02V
V_o (100% load)	9.54V	11.58V	13.15V	14.69V

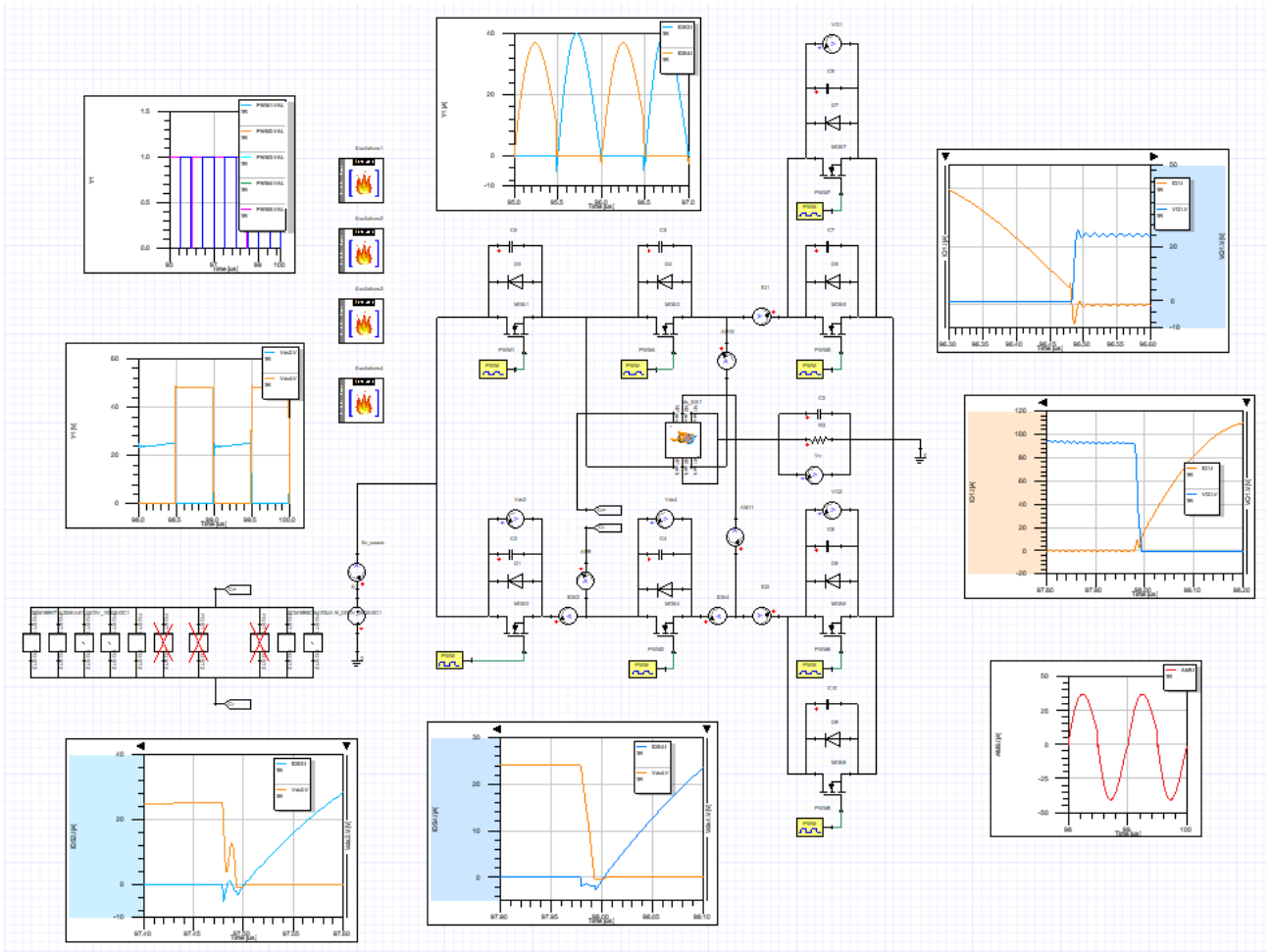




Experimental Verification

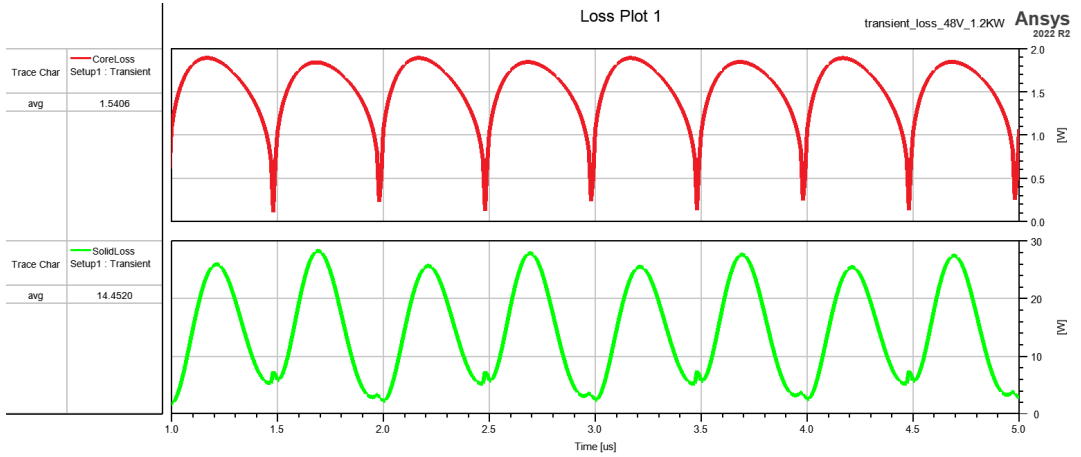


- Due to proximity effects, edge effects, and non-ideal conditions, actual transformer losses are difficult to calculate.
- The designed PCB winding is imported into Maxwell and simulated with Simplorer to estimate transformer losses.



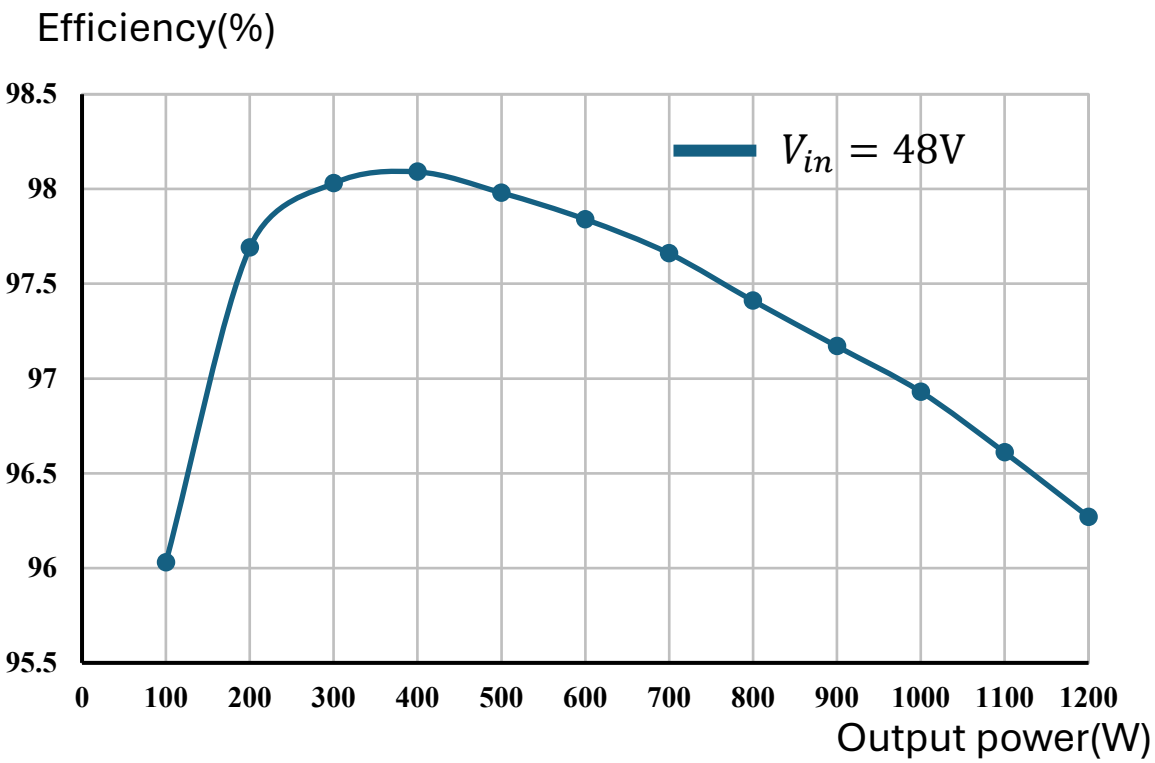
48 V input, 1.2 kW simulation results:

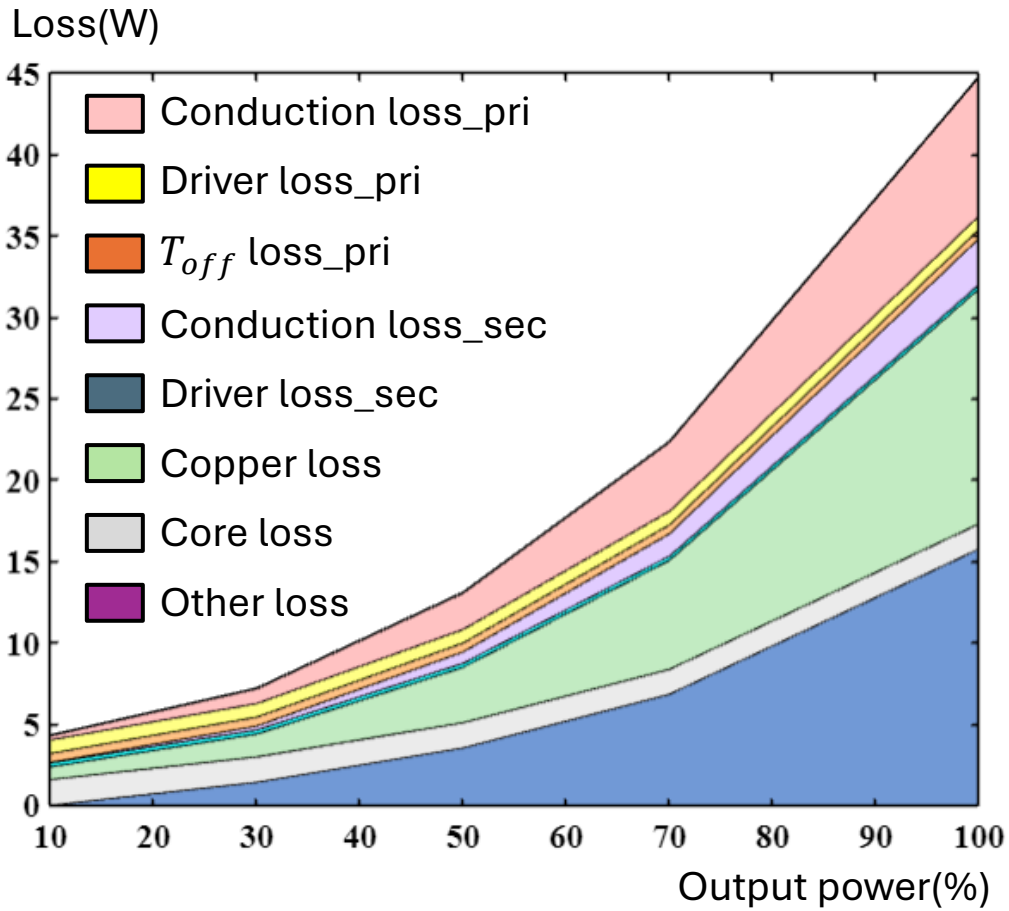
- Copper loss: 14.45 W
- Core loss: 1.54 W



Experimental Verification

- Loss analysis shows that beyond conduction and copper losses, other losses (via, PCB, capacitor, etc.) also exist. Optimizing them can further improve efficiency.
- Smaller primary-side switches (3 mm × 3 mm) result in higher conduction losses compared to the secondary side. Future designs must balance switch size and power loss.





Key Technologies for High Power Density and High Efficiency Converters

Summary of Key Technical Insights

- **Topology Optimization**: Select soft-switching topologies (e.g., ZVS/ZCS) to reduce switching losses
- **Magnetics Integration and Design**: High-frequency operation requires careful core and winding optimization
- **Component Selection**: Utilize wide bandgap devices (GaN/SiC) and low-ESR/ESL capacitors for improved performance
- **Thermal Management**: Higher power density increases thermal stress; early thermal modeling is essential

Importance of Pre-Simulation

- Identifies potential hotspots and EMI issues early in the design stage
- Enables optimization of magnetics, PCB layout, and thermal paths before hardware prototyping
- Reduces the number of design iterations and shortens development cycles
- Supports system-level trade-offs in performance, size, and cost

Conclusion:

Pre-simulation is a critical first step toward achieving high efficiency and reliability in high power density converter designs.

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ECIE LAB

ECIE Lab Demonstration

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Any Questions?