A SOLUTION FOR ACCURATELY MEASURING PCB IMPEDANCE USING A VECTOR NETWORK ANALYZER

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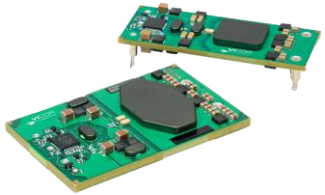
ROHDE&SCHWARZ
Make ideas real

POWER MANAGEMENT FOR SOCS AND RFSOCS
- INDUSTRY TRENDS AND CHALLENGES



GPU

Memory

PCIe

CPU

800V HVDC

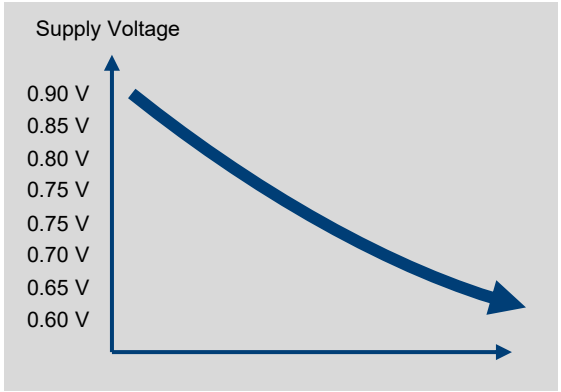
PDU

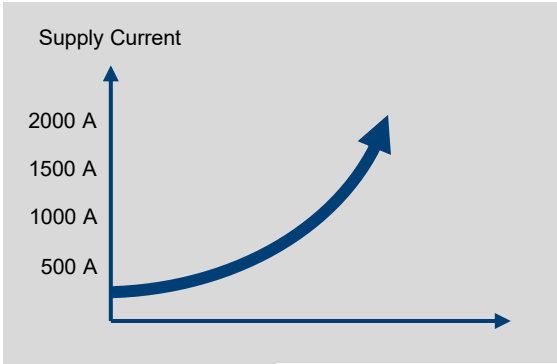
IBC / VR / LDO

Load

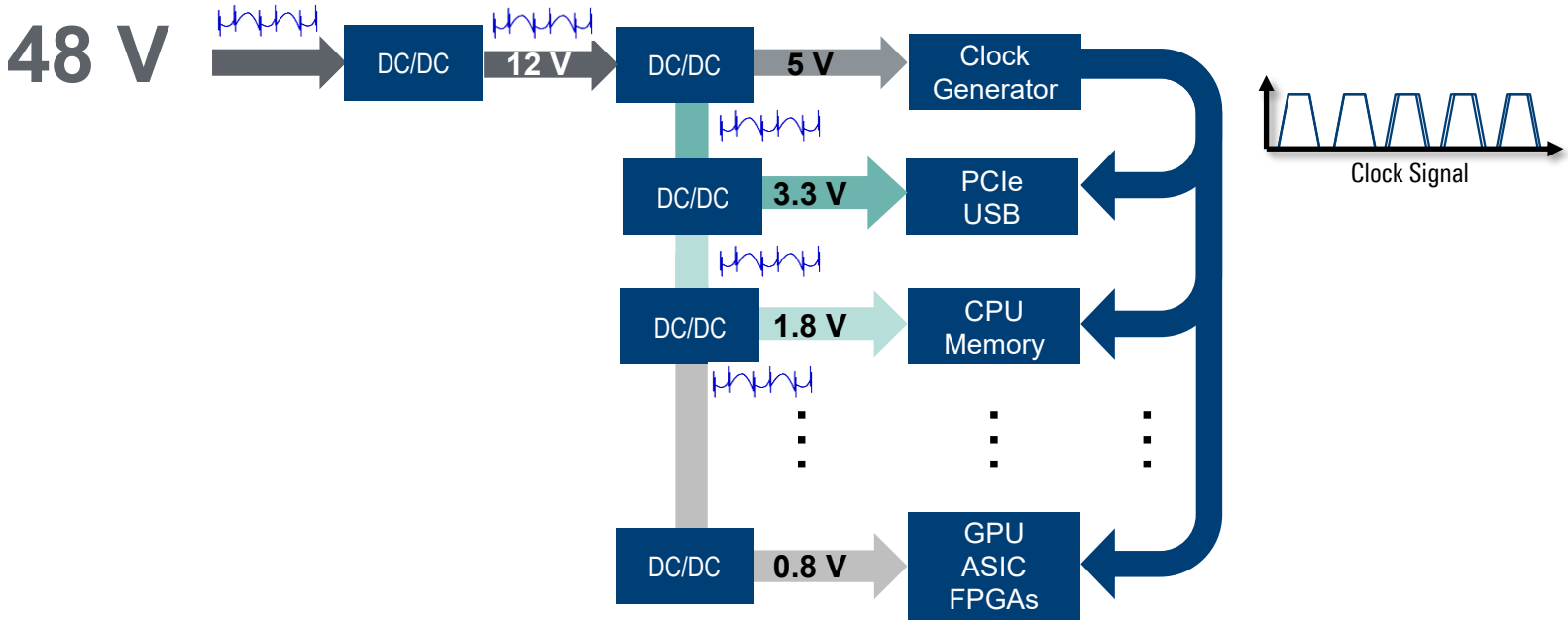
POWER MANAGEMENT FOR SOCS AND RFSOCS - INDUSTRY TRENDS AND CHALLENGES

- ASICs/SoCs require multiple rails for compact design
  - Low-voltage for high efficiency
  - High currents on core power rails
- Increasing use of multi-phase buck converters
  - Precise sequencing for power-up / power-down
  - Fast response on load transients
  - Low ripple / noise





HIGH CURRENT & LOW VOLTAGE
-POWER DELIVERY NETWORK



HIGH CURRENT & LOW VOLTAGE -POWER DELIVERY NETWORK

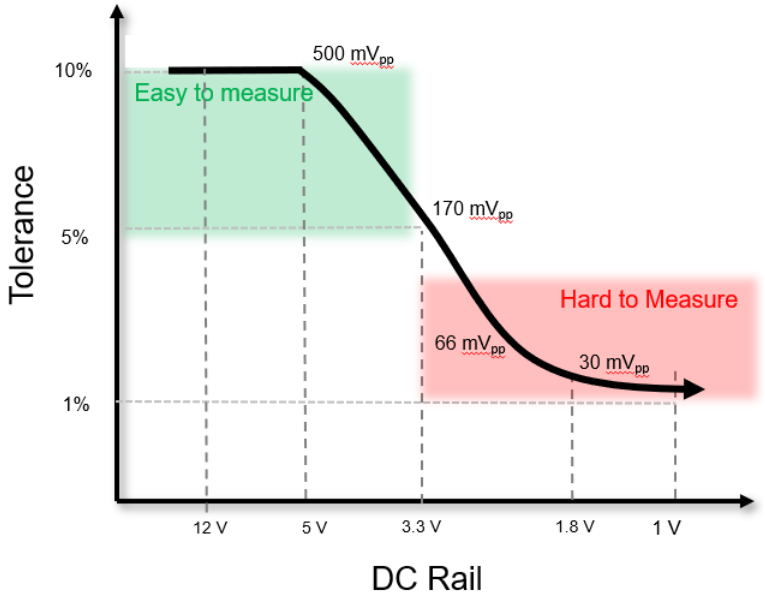
- Lower operating voltages for power reduction
  →Stricter rail tolerances

- Decreasing voltage and tolerance levels:

Rail Value	Tolerance	Need to measure
3.3 V	1%	33 mV_{pp}
1.8 V	2 %	36 mV_{pp}
1.2 V	2 %	24 mV_{pp}
1 V	1 %	10 mV_{pp}

EASY

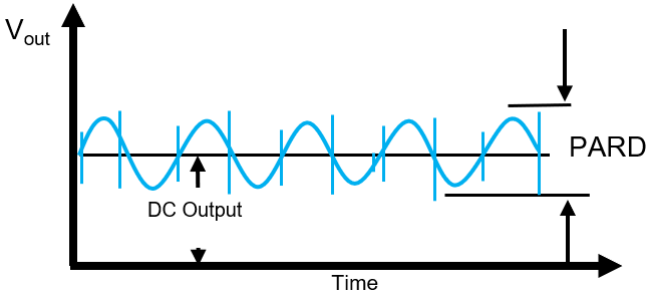
- Larger high-frequency transient current
  →Generate growing power supply noise



MEASUREMENT CHALLENGES - POWER INTEGRITY

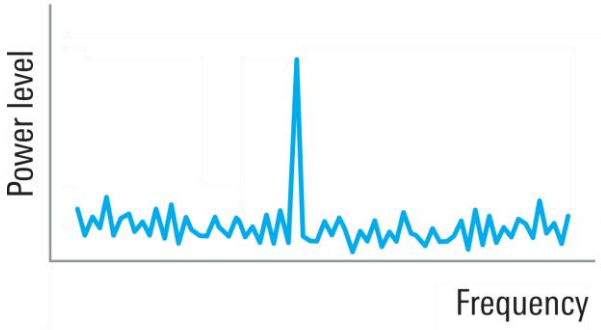
PARD (Periodic and Random Disturbances)

Periodic and random interference voltage fluctuations



Noise spectrum

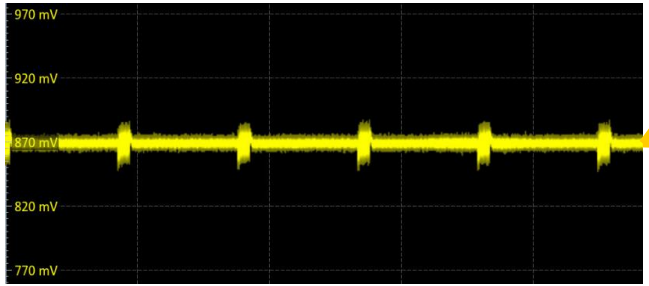
Analyze signal/event correlation in frequency and time domains

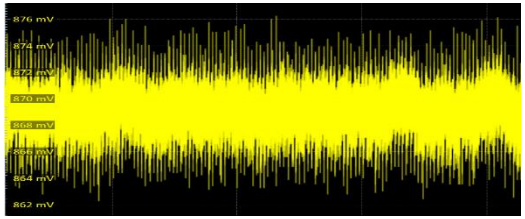


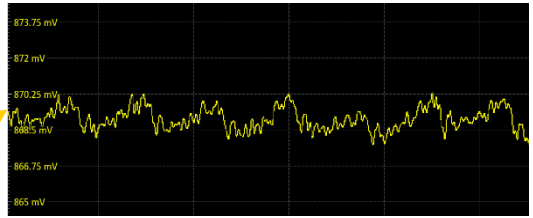
POWER INTEGRITY
-PARD(PERIODIC AND RANDOM DISTURBANCES

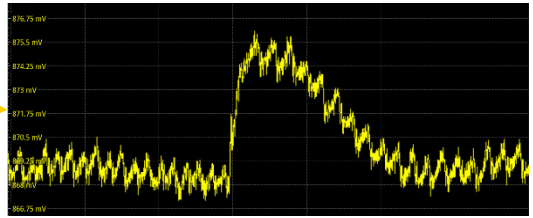
- Measurement challenges with regular techniques
  - Higher Attenuation and Noise Floor
  - Limited Offset and Reduced Resolution

- Optimized method for measuring low voltage
  - Low amplitude noise in the mV range
  - Requires low noise scope and probe
  - Wide DC offset range to center the voltage









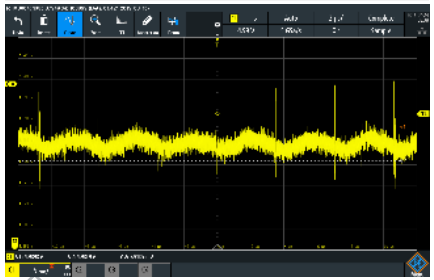
POWER INTEGRITY
-PARD(PERIODIC AND RANDOM DISTURBANCES)

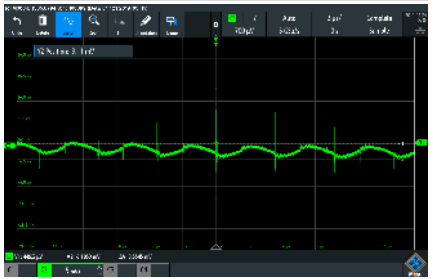
Standard
10:1
passive
probe

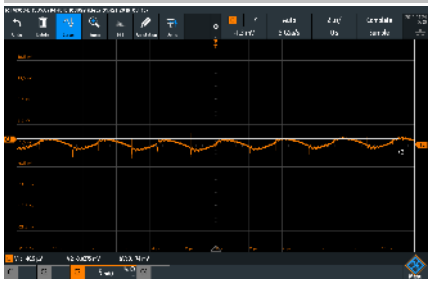
Low BW
1:1
passive
probe

50 Ω cable
(with blocking cap
Or AC coupling)

Specialized
power rail
probe







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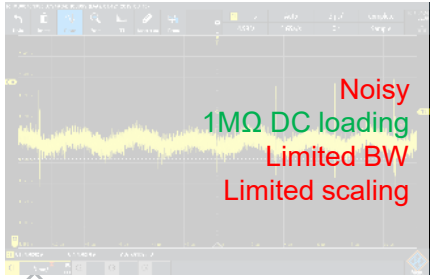
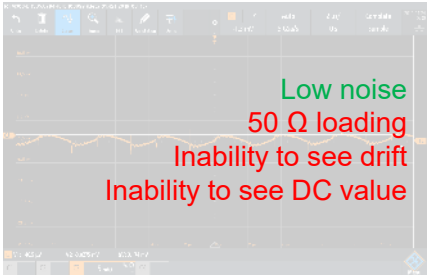
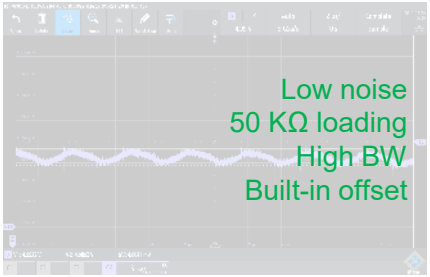
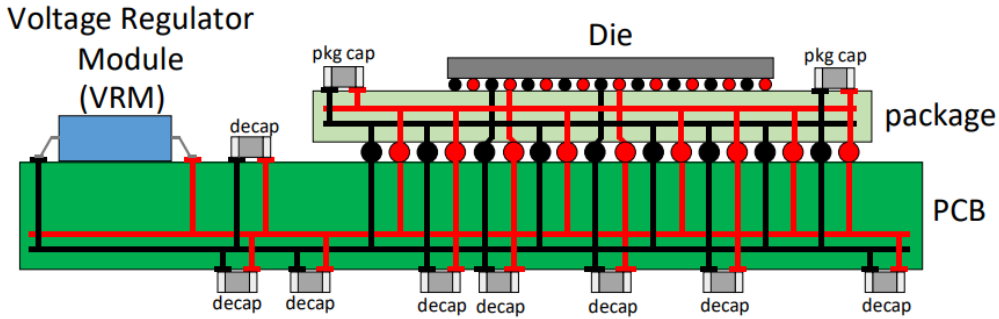
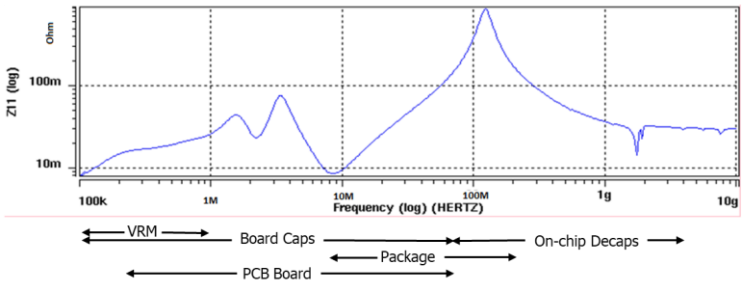


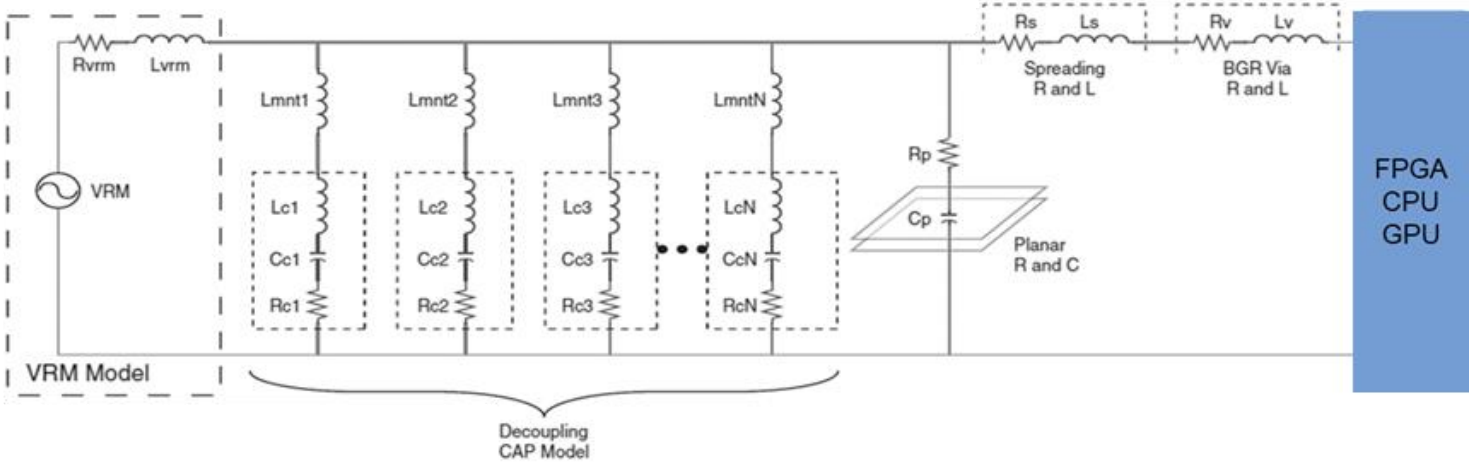




HIGH CURRENT & LOW VOLTAGE
-POWER DELIVERY NETWORK



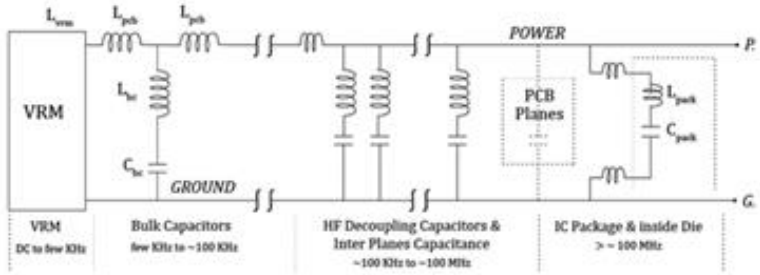




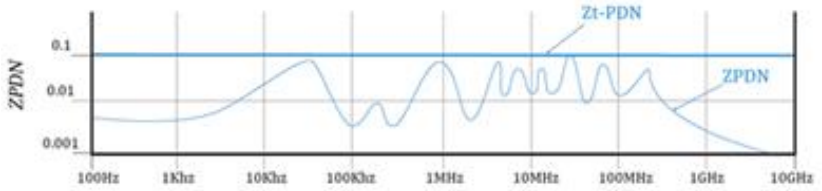
HIGH CURRENT & LOW VOLTAGE -POWER DELIVERY NETWORK

- High current and low voltage loads require low impedance power rails

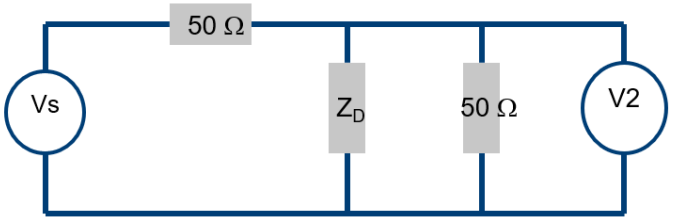
$$\Delta V = Z * \frac{di}{dt}$$



- Critical to reliable operation of high-speed digital circuits
  - Low impedance in the micro-ohm range
  - Flat vs. frequency



- Measure using 2-port shunt-through technique
  - Frequencies from 1 Hz to 100 MHz (up to 1 GHz)
  - VNA (low frequency limit) or oscilloscope



HIGH CURRENT & LOW VOLTAGE
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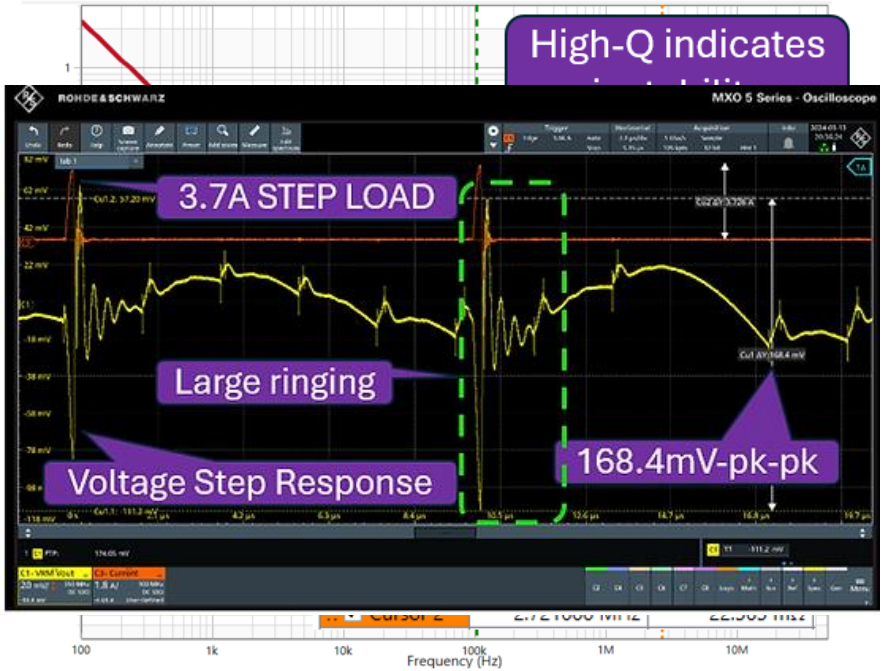
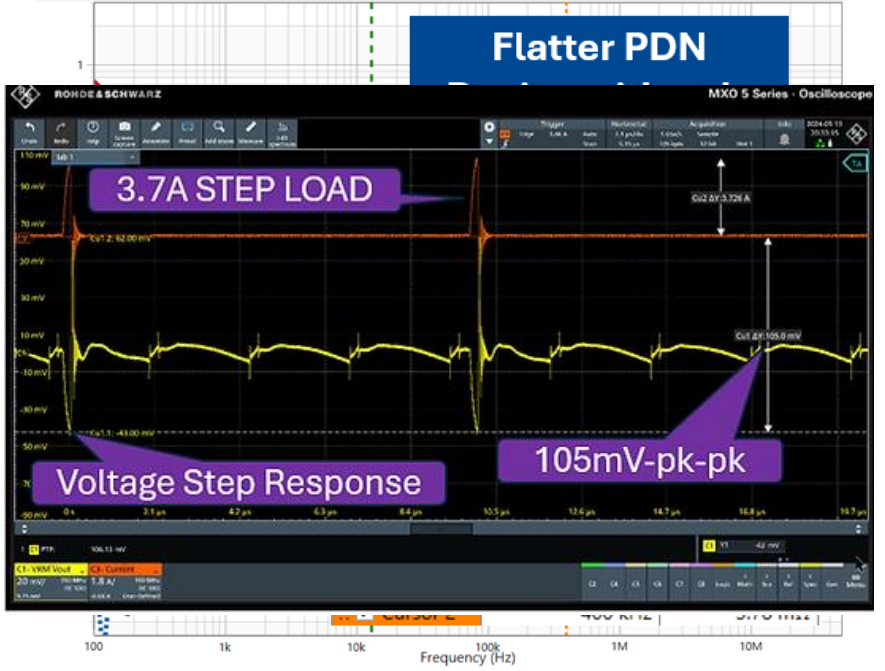
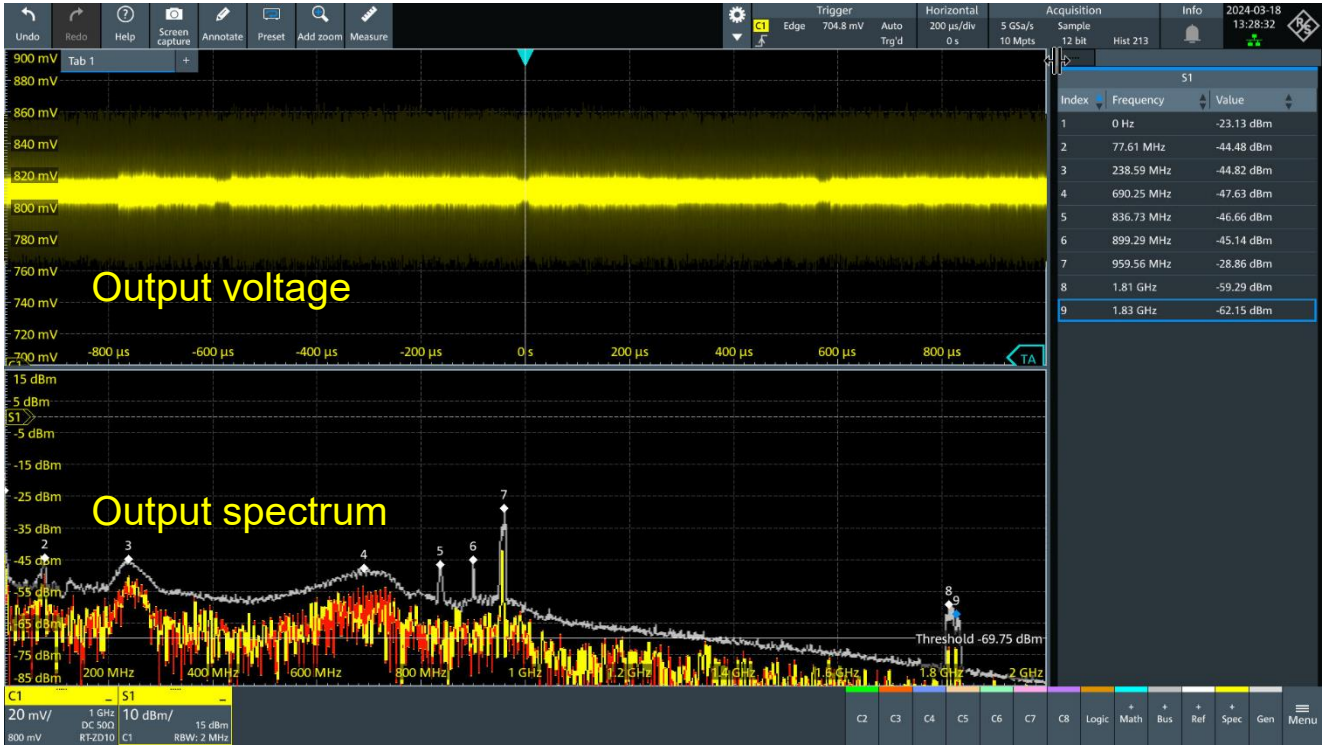




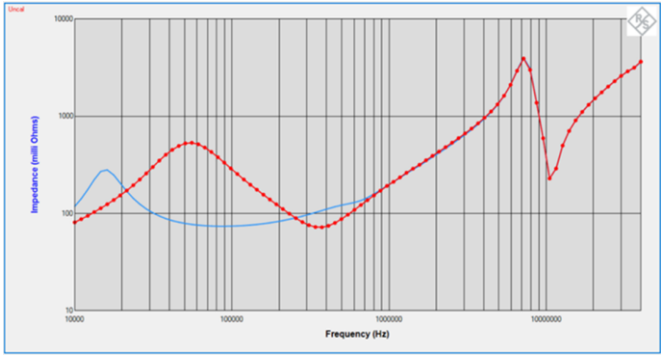
POWER INTEGRITY
-NOISE SPECTRUM



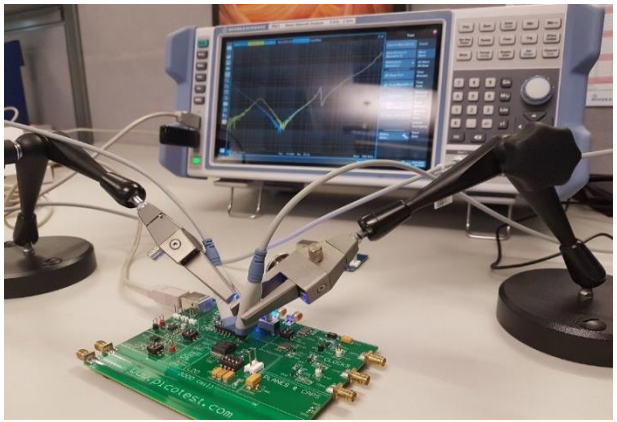
- High FFT update rate
- Synchronized analysis of time and frequency domain
- Independent time and frequency control
- Peak list
- Frequency domain trigger

HIGH CURRENT & LOW VOLTAGE -POWER DELIVERY NETWORK

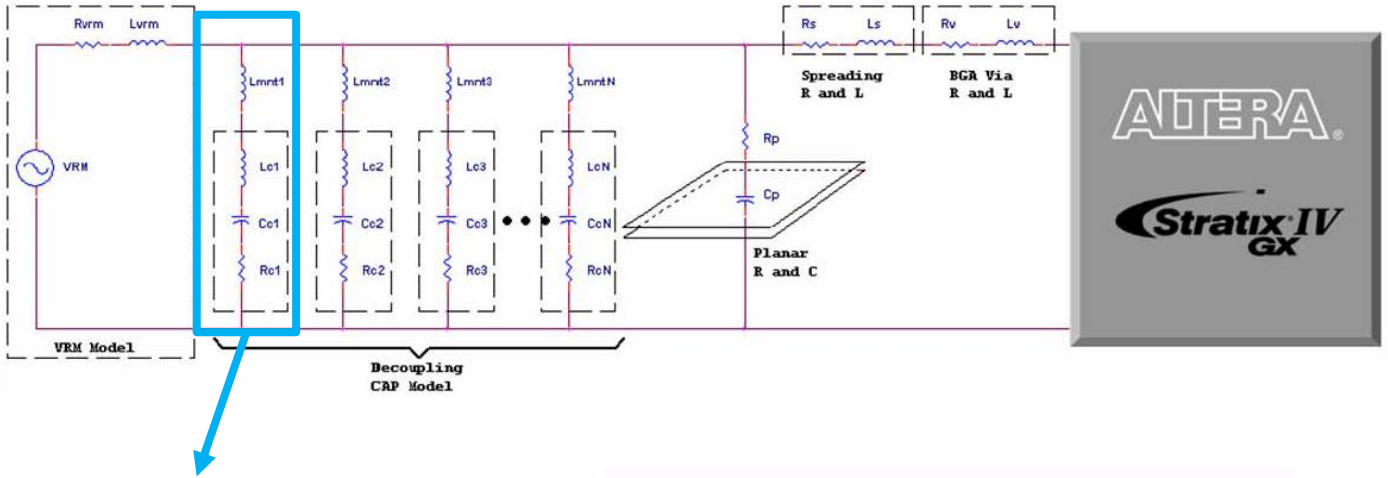
- Measurement of impedance from fractional Hz to 100 MHz using build-in generator
  - Using build-in generator
  - Free software application available

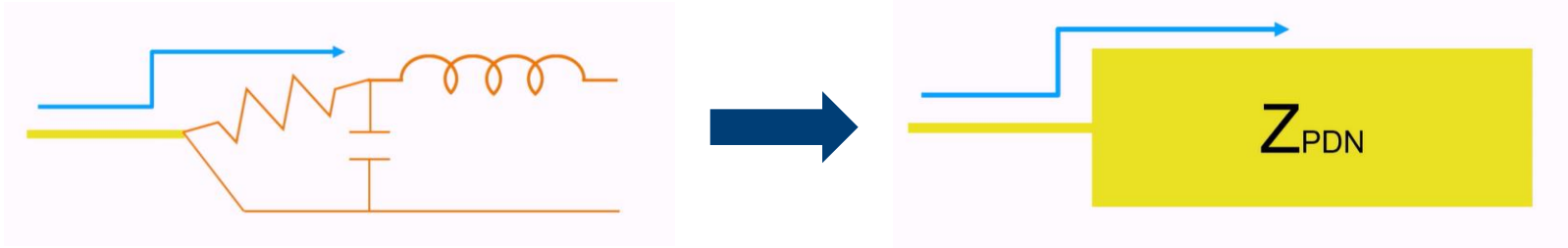


- Combines VNA and oscilloscope applications
  - Covers frequency range down to DC
  - Enables powered measurement
  - Stability measurement (NISM)



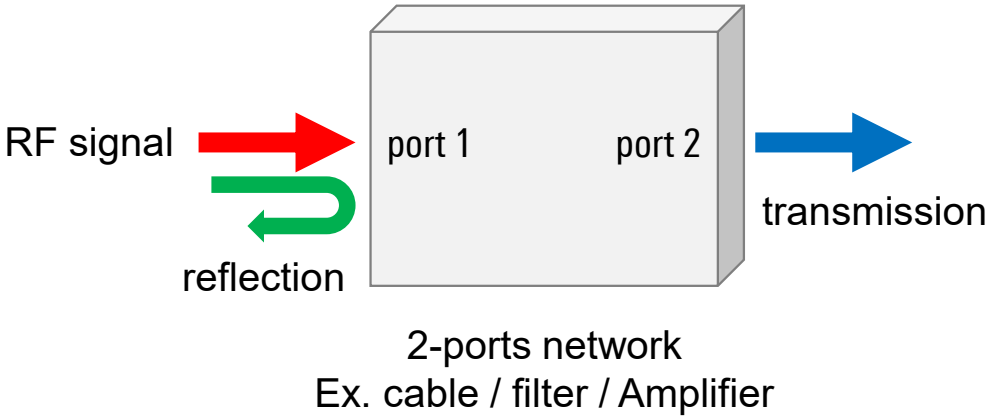
POWER DELIVERY NETWORK (PDN) : IMPEDANCE

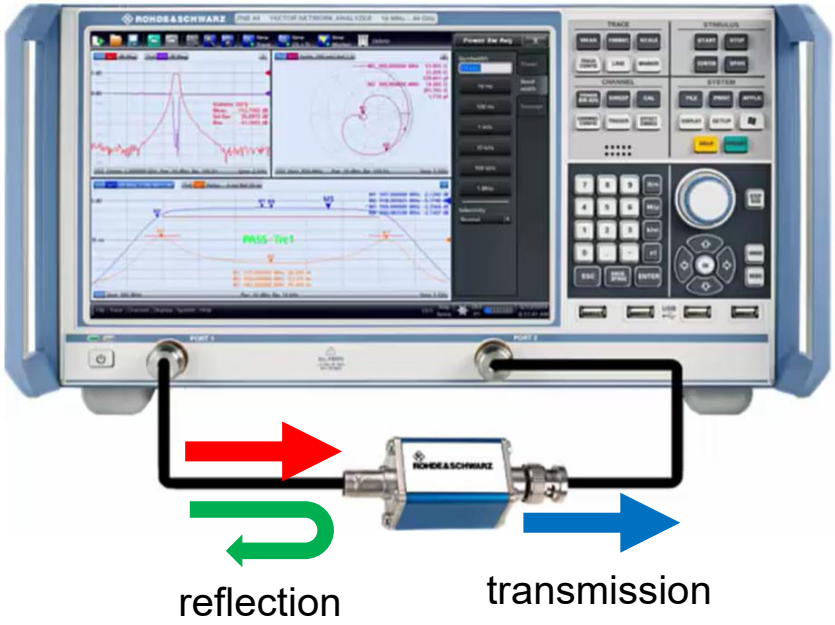




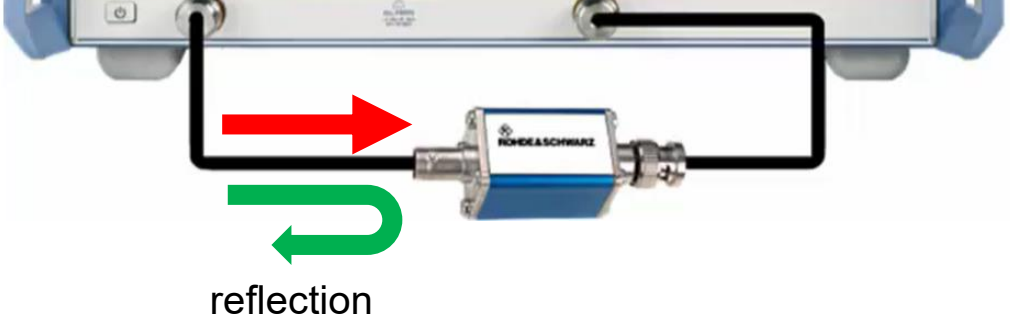
How VNA work?

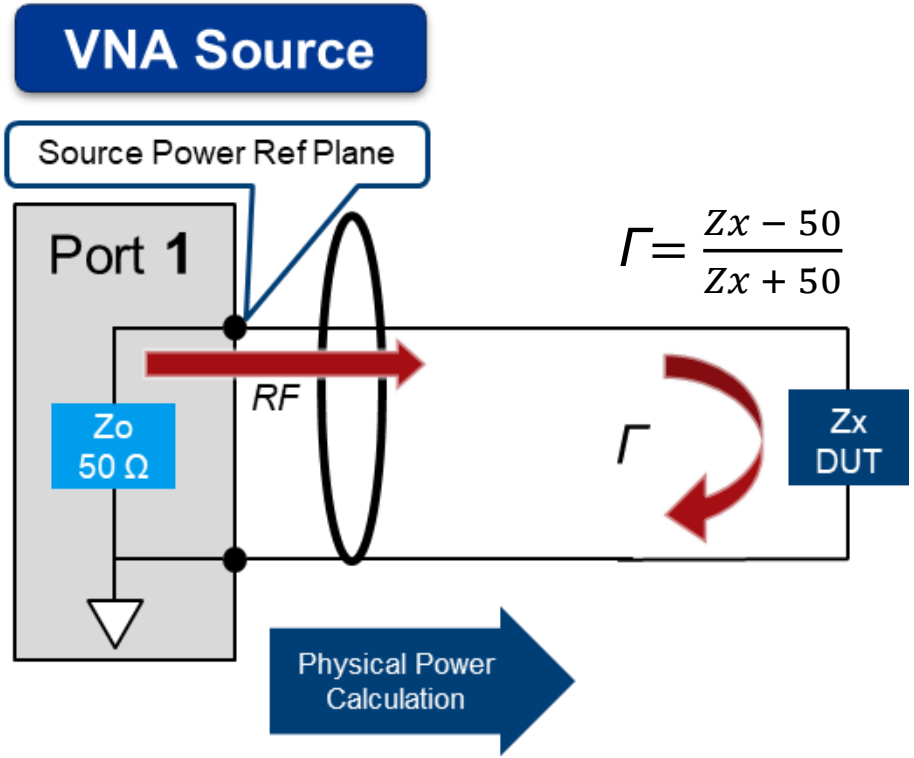
- Signal is injected into a giver port and signals appearing at the connected ports are measured.
- Usually only one signal is injected into one port at one time.
- Usually measured over a range of frequencies.





One Port Reflection





$$\Gamma = \frac{Zx - 50}{Zx + 50}$$

$$\text{Return Loss} = -20\log|\Gamma|$$

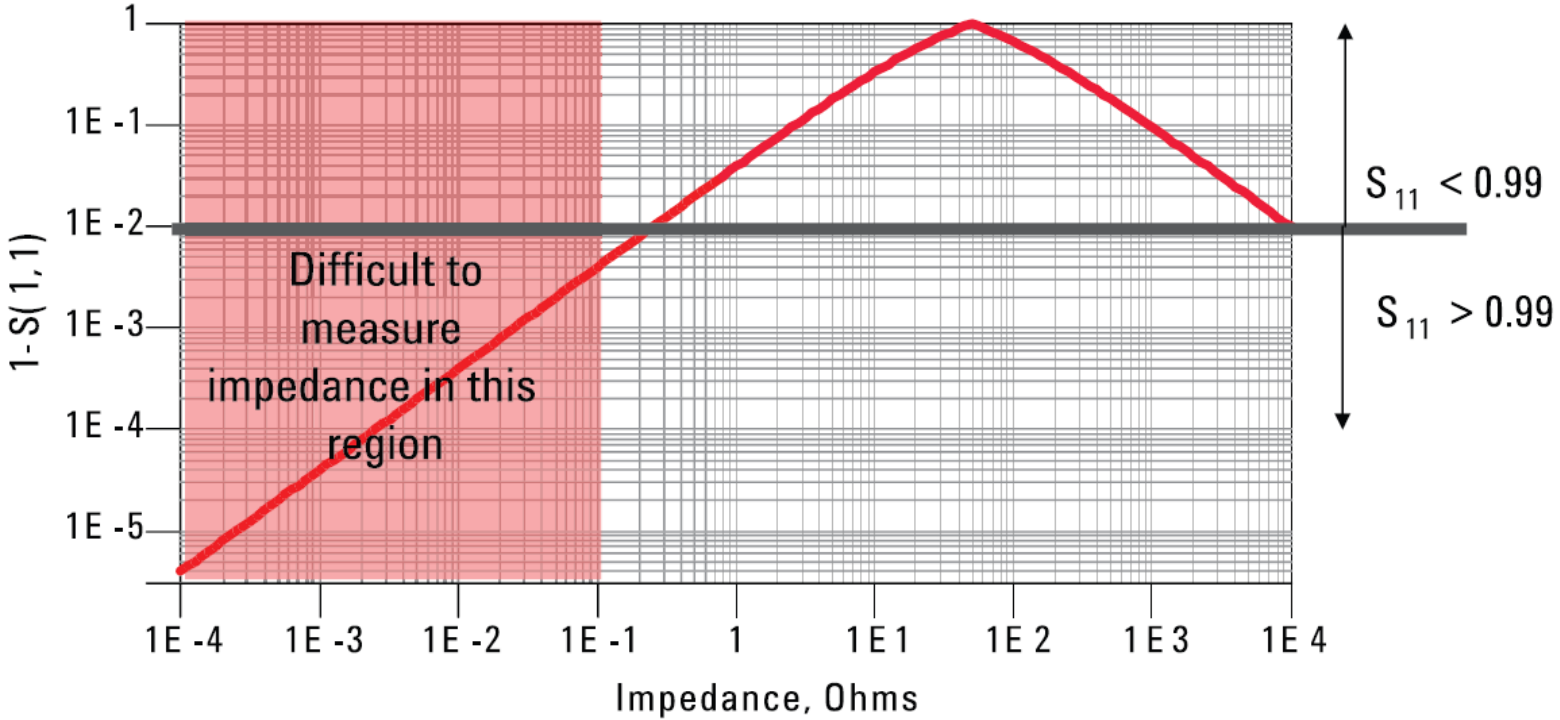
$$\Gamma = \frac{1 - 50}{1 + 50} = -0.96$$

$$RL = 0.35dB$$

$$\Gamma = \frac{0.1 - 50}{0.1 + 50} = -0.996$$

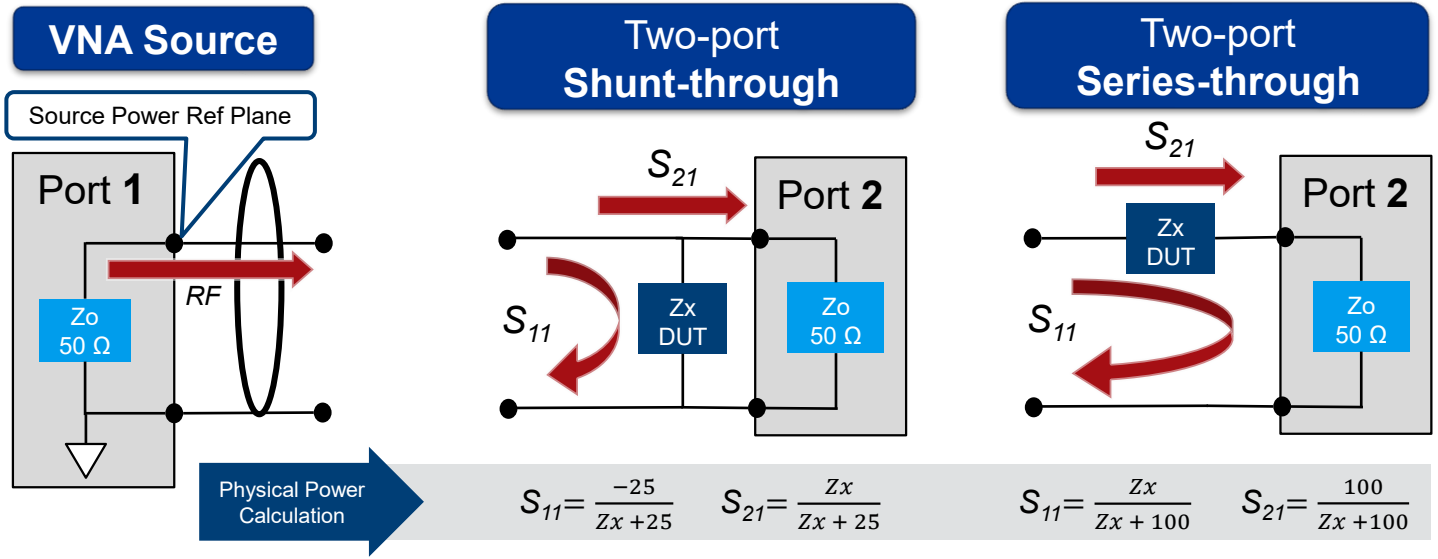
$$RL = 0.035dB$$

CHALLENGE OF ONE PORT REFLECTION METHOD

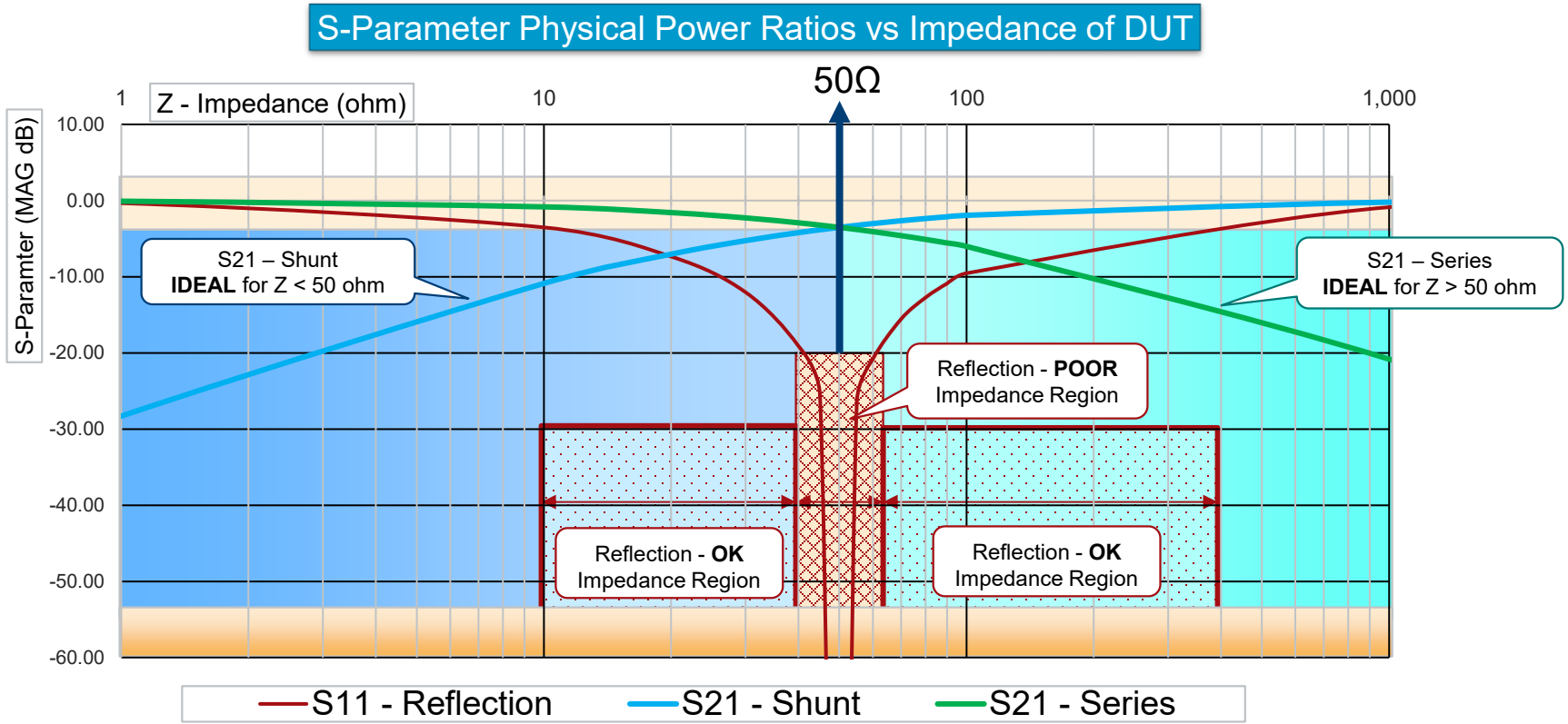


TWO PORT TRANSMISSION

transmission

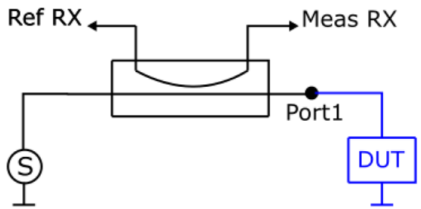


VNA MEASUREMENT PHYSICAL POWER - GUIDE



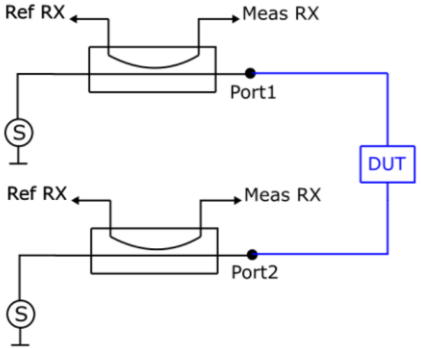
METHODS TO MEASURE IMPEDANCE

Reflection method



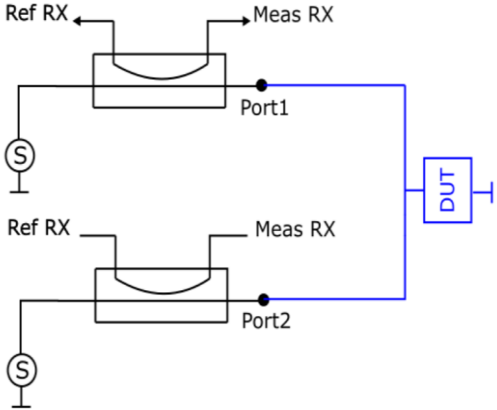
For mid range impedances
~ 2 Ω - 1 k Ω

Series method



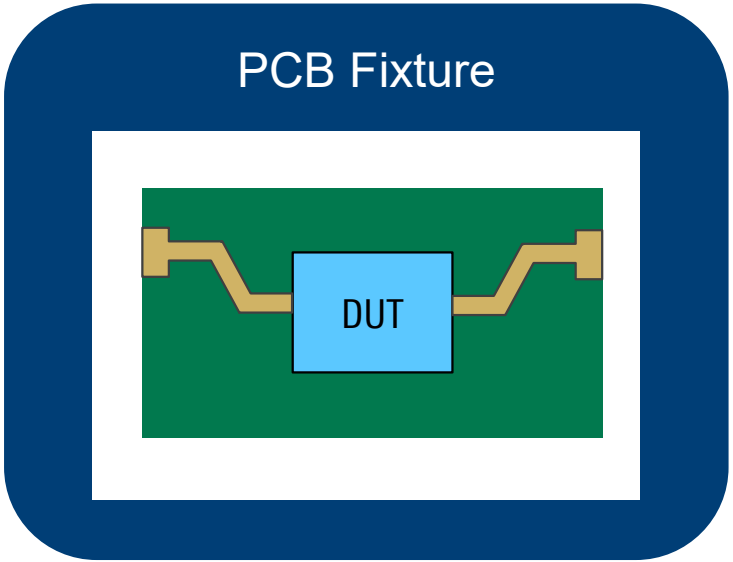
For high range impedances
~ 10 Ω - 1 M Ω

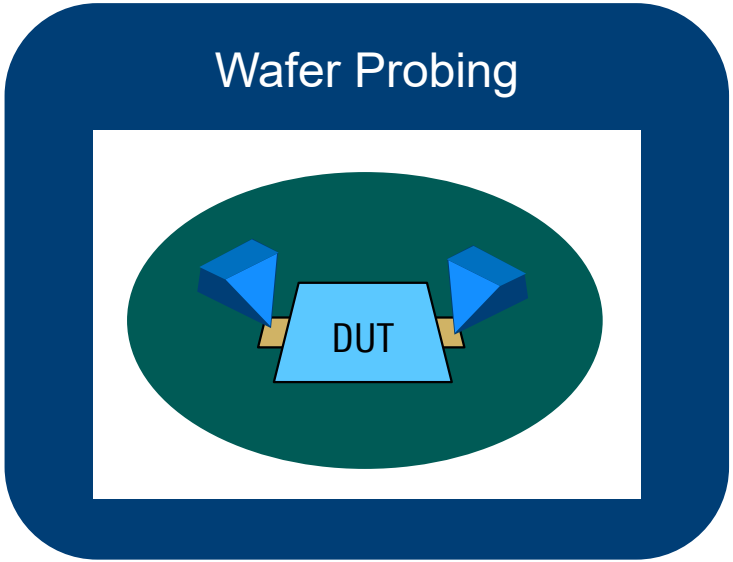
Shunt – through method



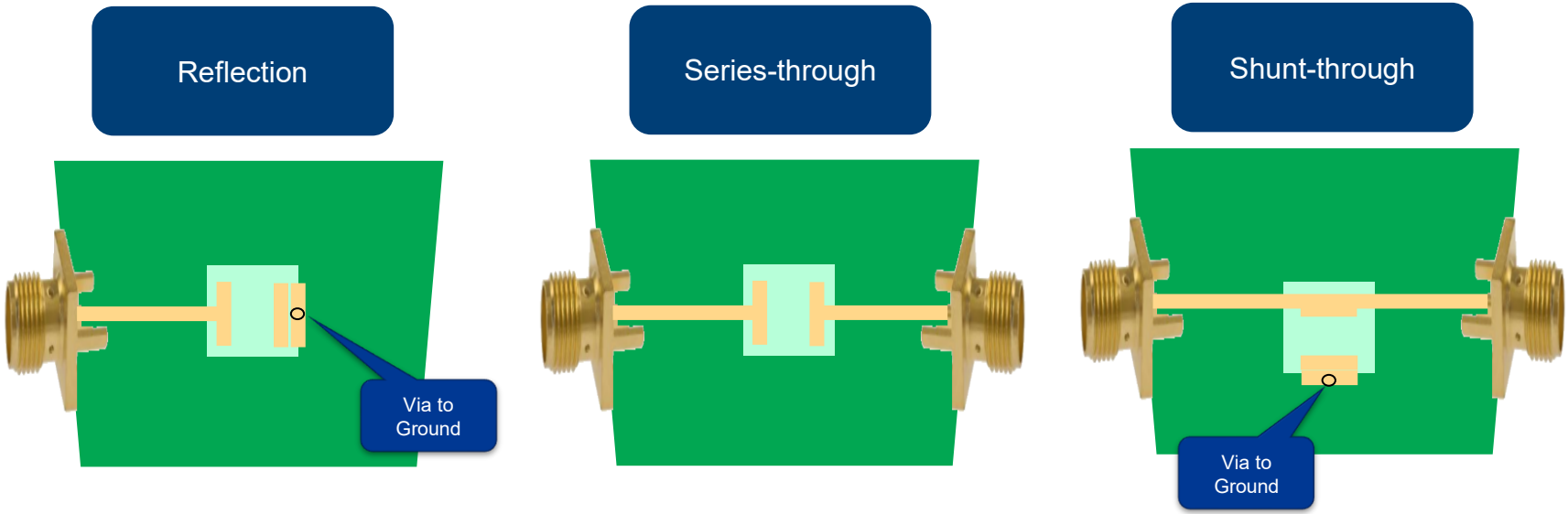
For low range impedances
~ 10 uΩ - 500 Ω

DEALING WITH CONTACT INTERFACE
DUT TEST METHODS

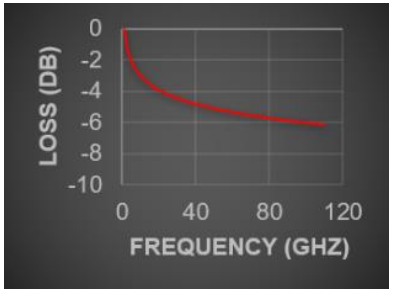




PCB FIXTURE – EXAMPLES



PCB FIXTURE REMOVAL
LENGTH AND PHASE OFFSET PREDICTION



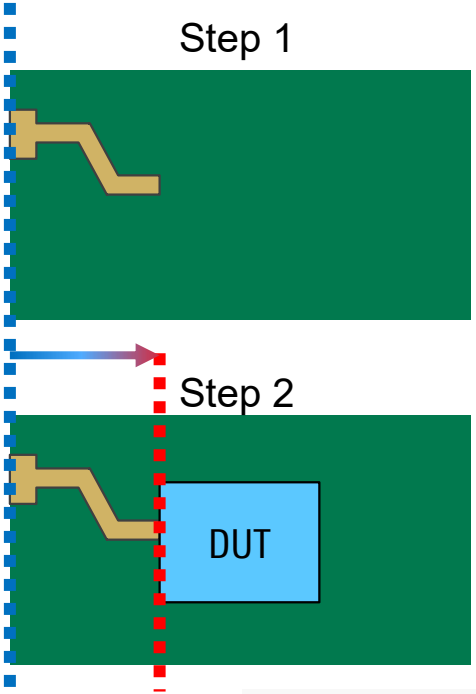
- Prediction using lossy coaxial transmission line model equations for
  - Magnitude:

$$Loss(f) = Loss_{DC} + (Loss(f_1) - Loss_{DC}) \times \sqrt{\frac{f}{f_1}}$$

  - Phase: modeling by delay (slope of phase)

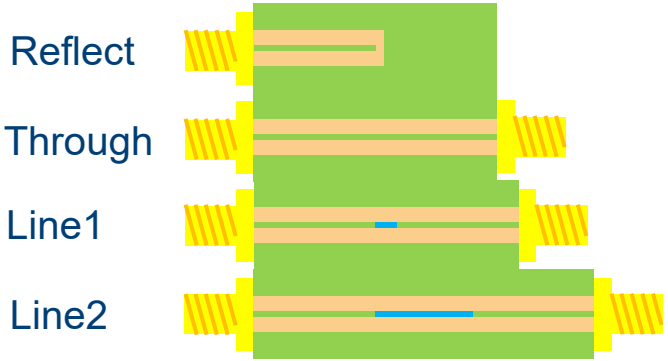
$$\tau_{g\,meas} = -\frac{\Delta\phi_{deg}}{360^{\circ} \cdot \Delta f}$$

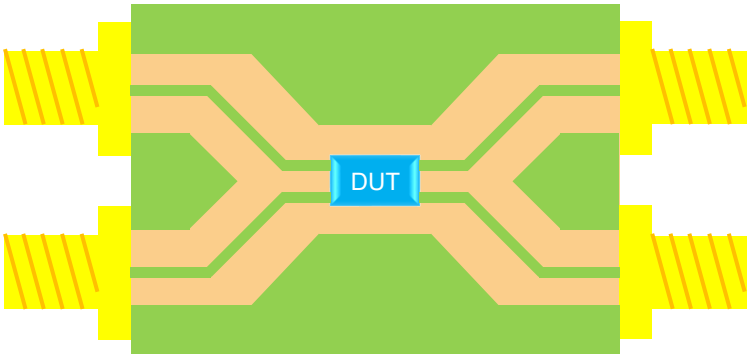
- Disadvantage of length and phase offset
  - Inaccurate for higher frequencies
  - Prediction failure for nonlinear/dispersive transmission line



PCB FIXTURE REMOVAL
TRL CALIBRATION TECHNIQUES

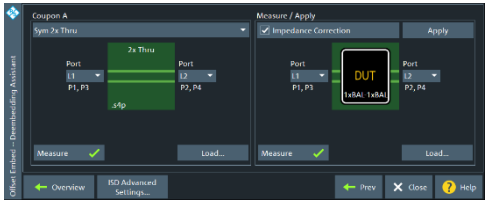
- Measure with reference plan right at the input/output of components or devices

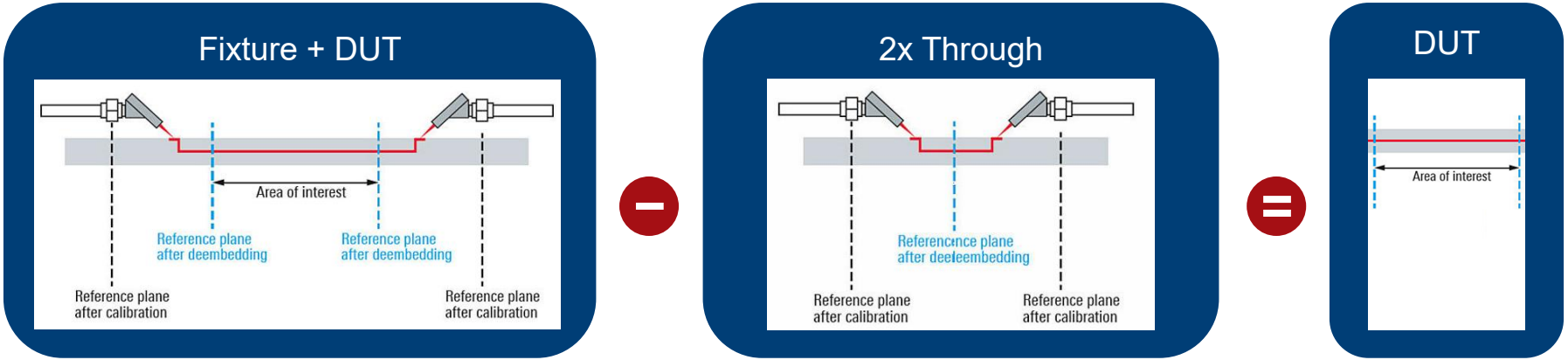




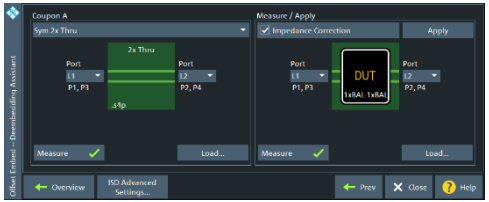
- Disadvantage of TRL calibration method
  - Long calibration time
  - Frequency limited (need several line standards)
  - Need to know TRL standard design concept
  - Calibration not possible for balanced structure

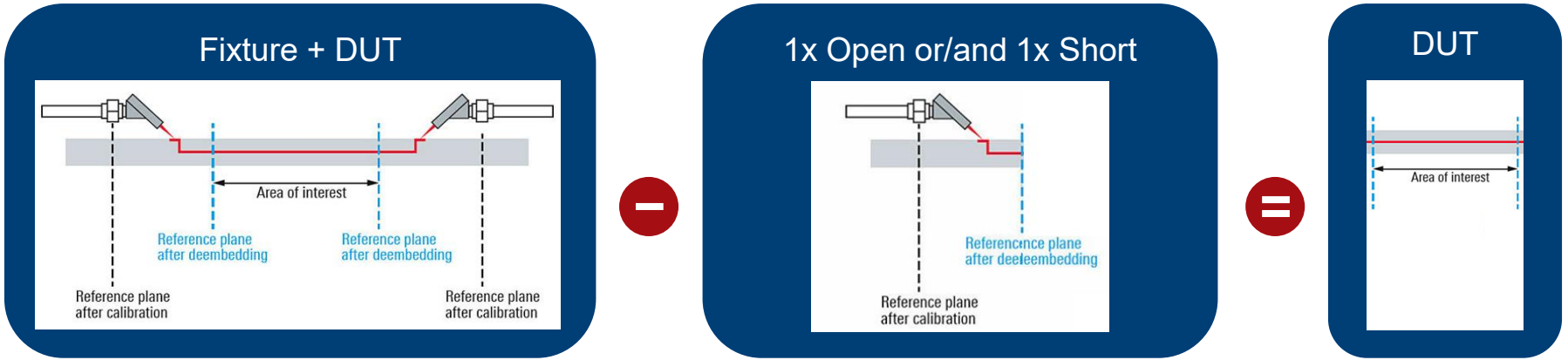
TWO-STEP DE-EMBED TECHNIQUE





TWO-STEP DE-EMBED TECHNIQUE





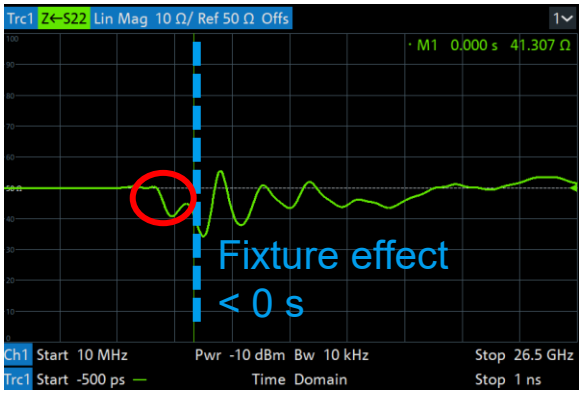
- Industry accepted modeling algorithms
  - K210 EZD: Eazy De-embedding
  - K220 ISD: In-Situ De-embedding
  - K230 SFD: Smart Fixture De-embedding

Method	Offset	TRL	Fixture Model De-embed
Correction (kit)	Easy	Complex	Easy
Speed	Fast	Slow	Fast
Accuracy	Poor	Moderate	Best

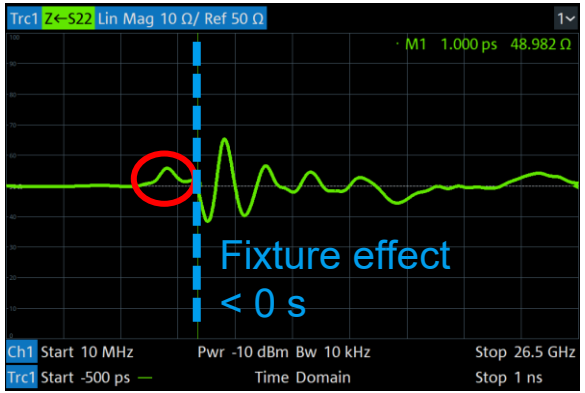
FILTER MEASUREMENT WITH DE-EMBED

TDR MEASUREMENT ACCURACY COMPARISON

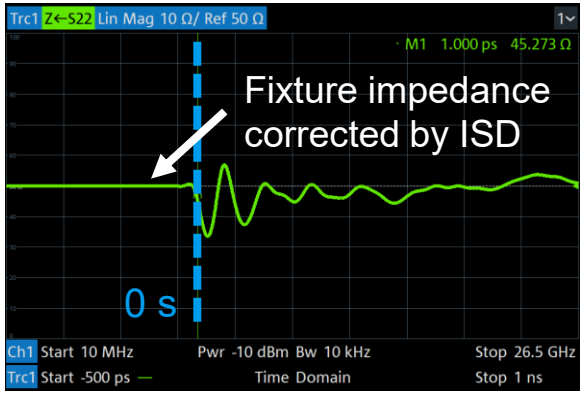
Coax Cal kit + Offset 80ps



TRL Cal Kit



Coax Cal kit + ISD Algorithm

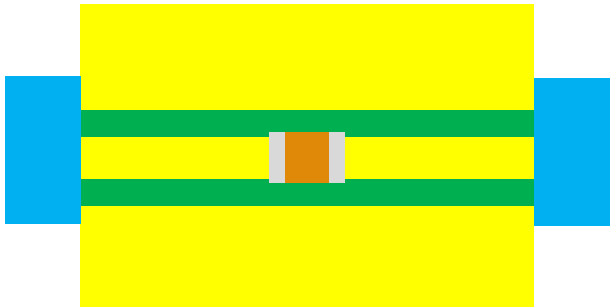


TEST CASE …

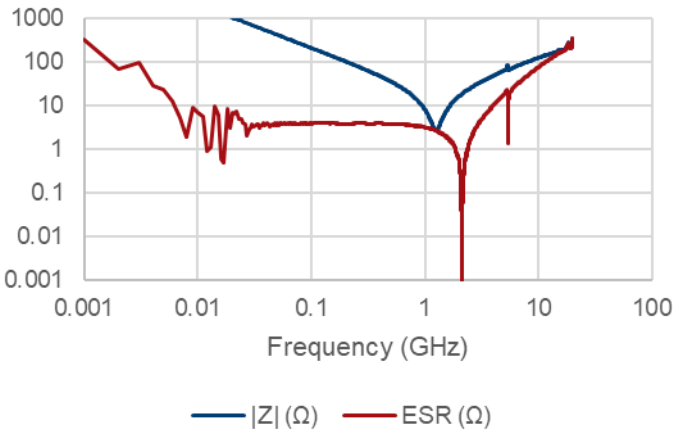
On-board Connector
2.92 mm

THRU

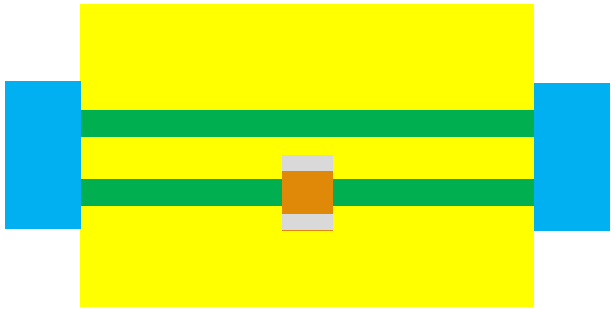
Series



Z



Shunt



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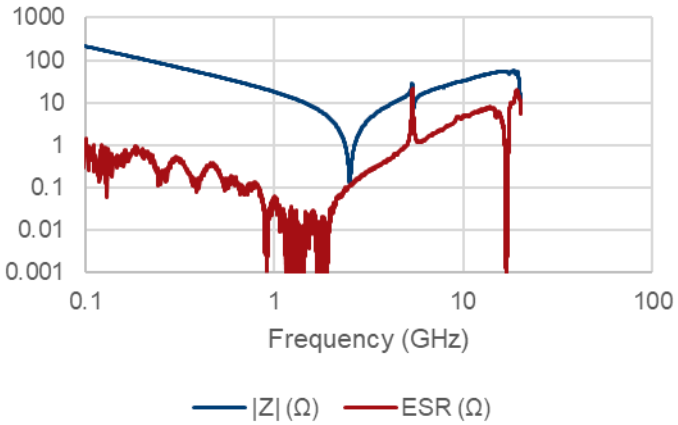
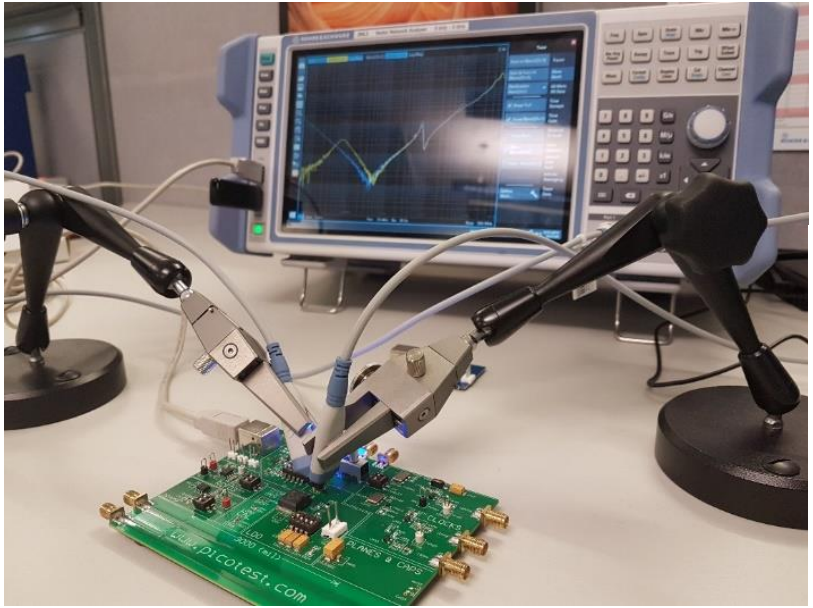
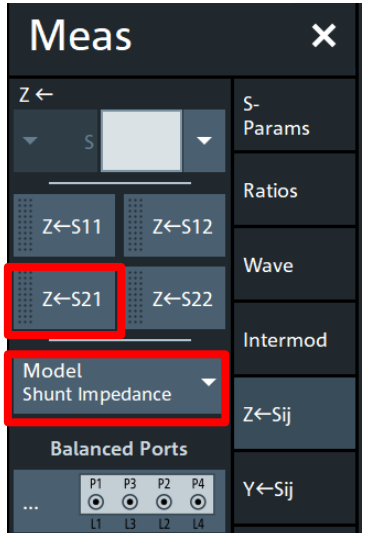
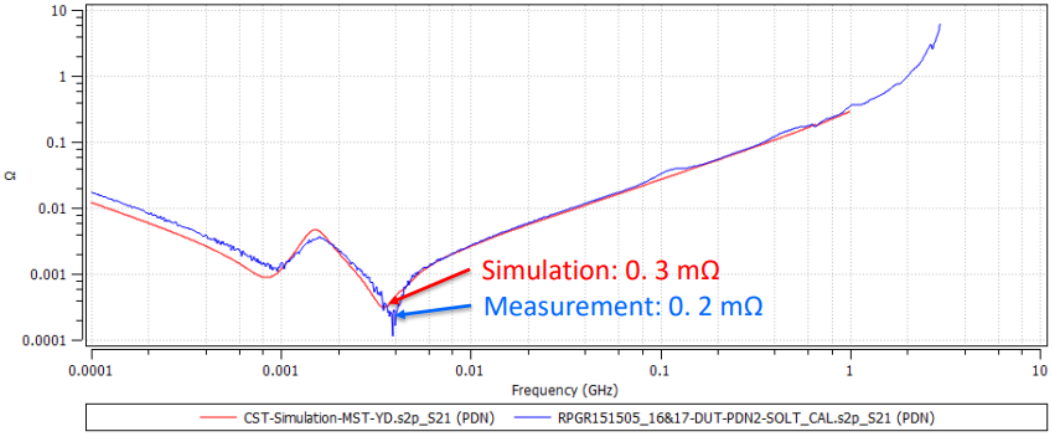


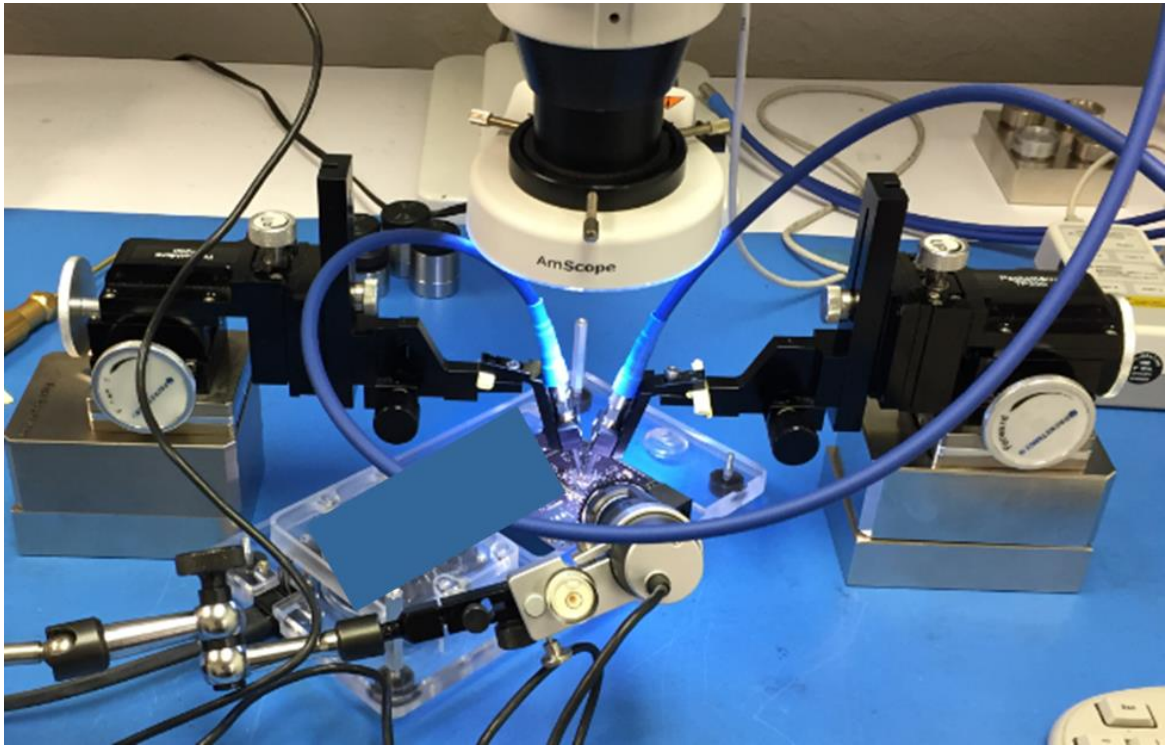
TESTING WITH PROBE

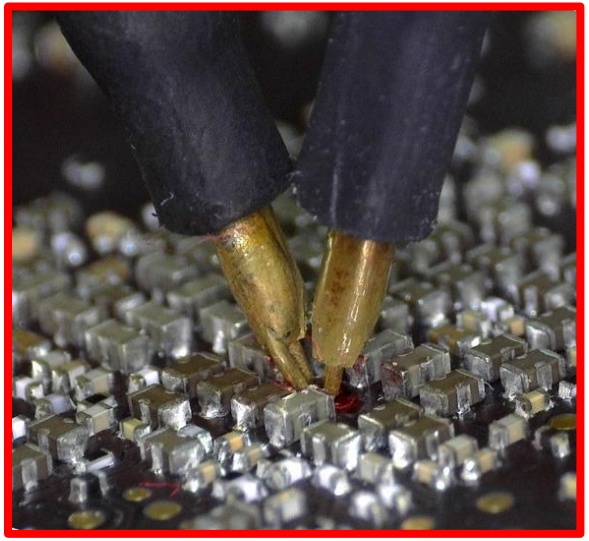






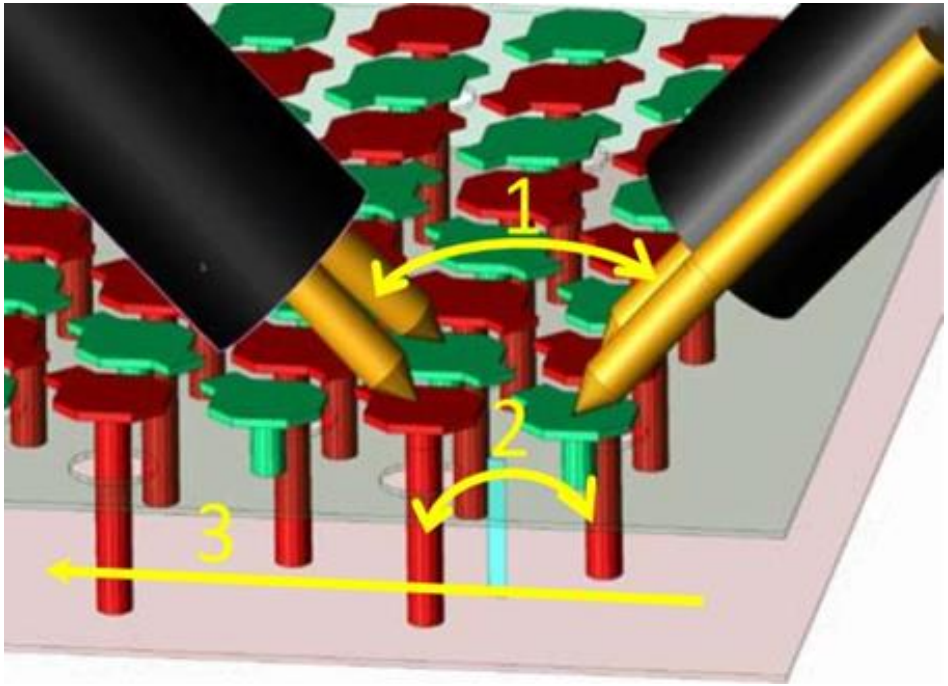
POWER INTEGRITY PROBING





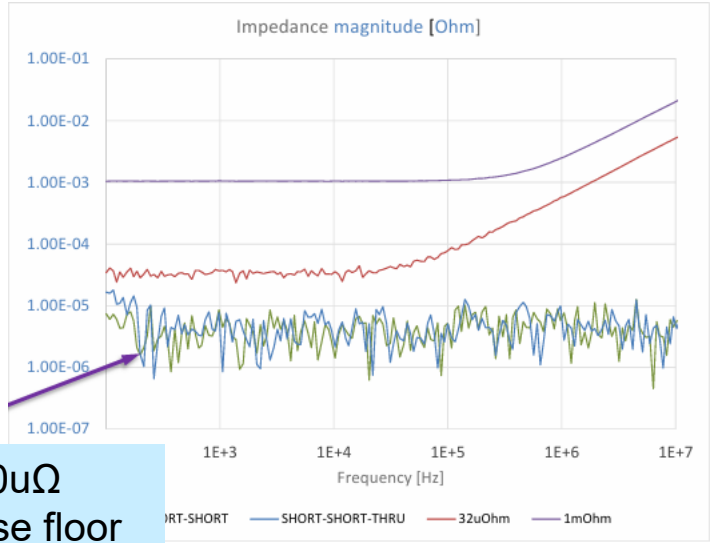
MILLIOHM PDN MEASUREMENTS

Impact of Finite Interconnect Impedance Including Spatial and Domain Comparison of PDN Characterization



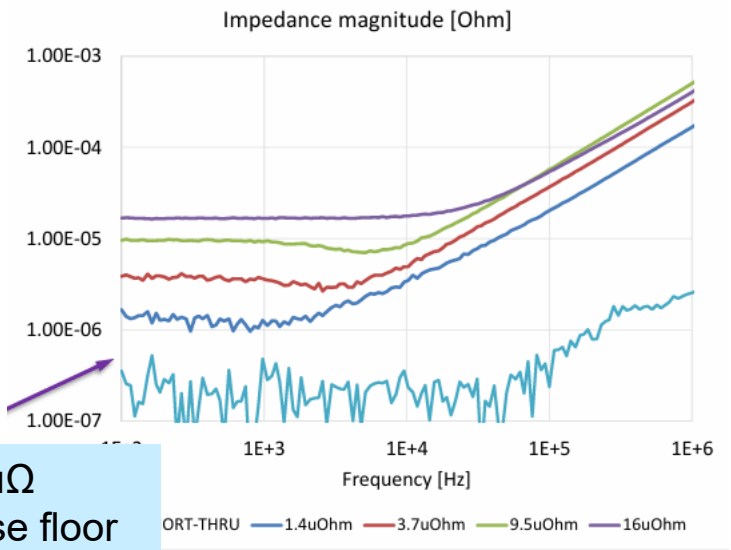
- Analyzing the impact of probe-tip coupling in wafer probe calibrations and measurements.
- Investigating the impact of via coupling within the DUT.
- Understanding the spatial effects associated with large via arrays.

DESIGNCON 2025



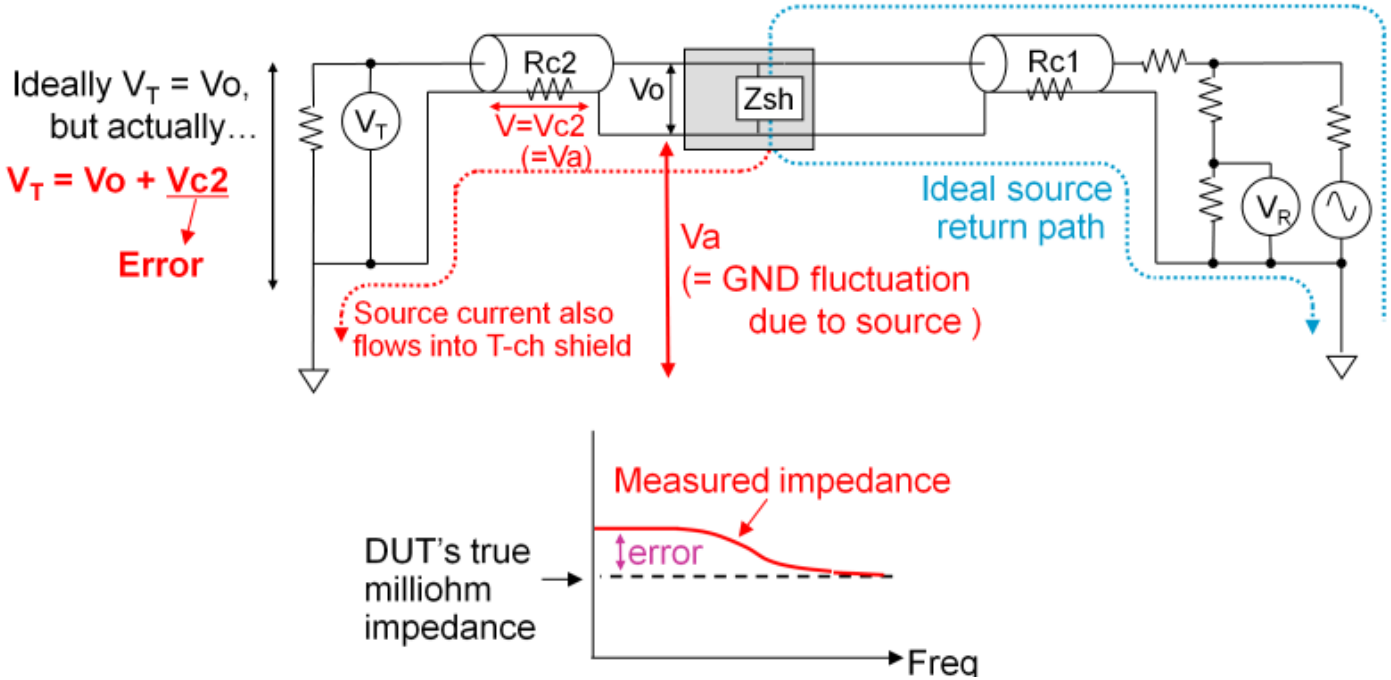
< 10uΩ
Noise floor

Reduce IFBW, power booter on P1, LNA on port2.



< 1uΩ
Noise floor

LOW-FREQ ERRORS CAUSED BY GROUND LOOP

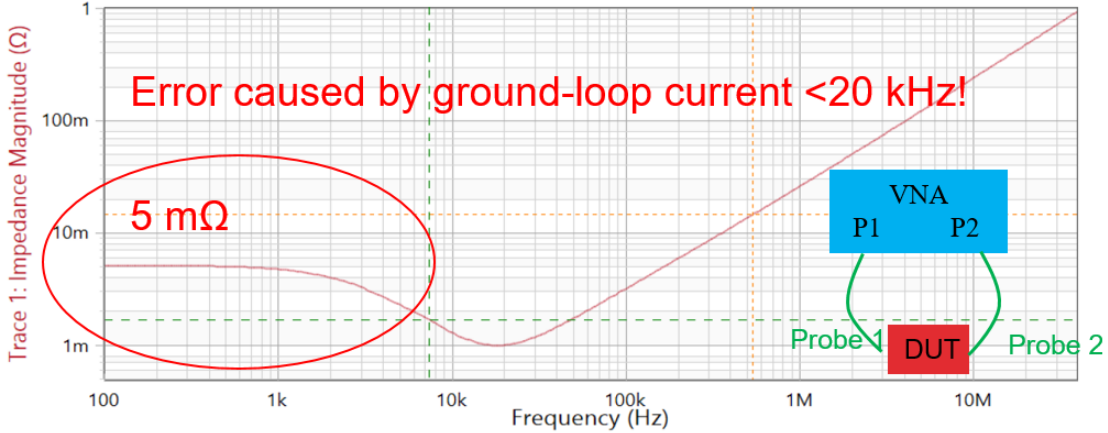


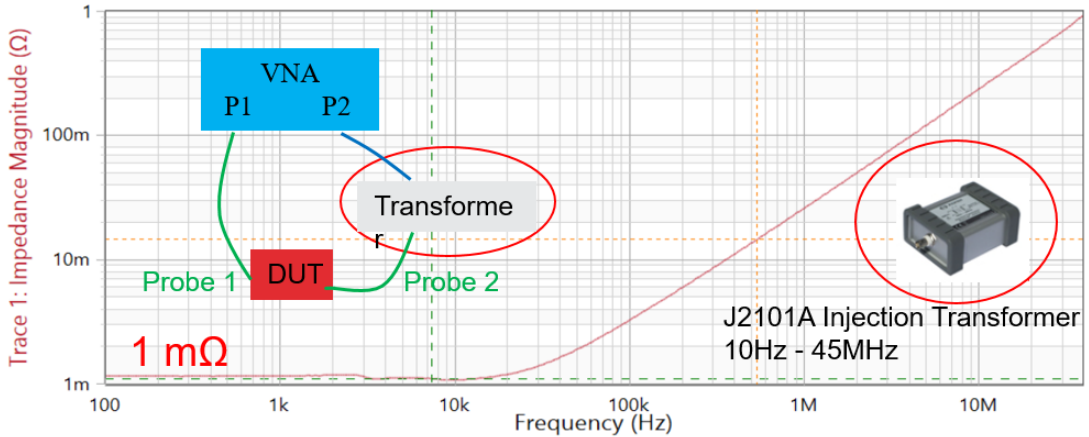
If the DUT's impedance is very small (ZDUT < tens of milliohms)

Source current flows into source-to-receiver cable GND loop.

Measurement errors occur at LF range (<20kHz)

USE TRANSFORMER TO BREAK THE GROUND LOOP





Thanks for your time!

ROHDE&SCHWARZ

Make ideas real